

# COMLINEAR® AD8052LV

## Low Cost, +2.7V to 5.5V, 260MHz Rail-to-Rail Amplifier



### FEATURES

- 260MHz bandwidth
- Fully specified at +2.7V and +5V supplies
- Output voltage range:  
0.036V to 4.953V;  $V_S = +5$ ;  $R_L = 2k\Omega$
- Input voltage range:  
-0.3V to +3.8V;  $V_S = +5$
- 145V/ $\mu$ s slew rate
- 4.2mA supply current per amplifier
- $\pm 55$ mA linear output current
- $\pm 85$ mA short circuit current
- Directly replaces AD8052, AD8042  
and AD8092 in single supply applications
- Pb-free SOIC-8 package

### APPLICATIONS

- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Telecom and optical terminals
- Video driver

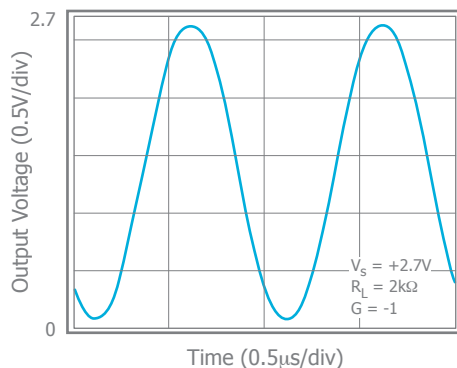
### General Description

The COMLINEAR AD8052LV is a low cost dual, voltage feedback amplifier. This amplifier is designed to operate on +2.7V to +5V, or  $\pm 2.5$ V supplies. The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

The AD8052LV offers superior dynamic performance with a 260MHz small signal bandwidth and 145V/ $\mu$ s slew rate. The combination of low power, high output current drive, and rail-to-rail performance make the AD8052LV well suited for battery-powered communication/computing systems.

The combination of low cost and high performance make the AD8052LV suitable for high volume applications in both consumer and industrial applications such as wireless phones, scanners, and color copiers.

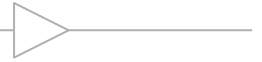
### Output Swing



### Ordering Information

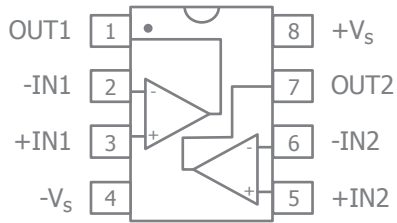
Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
AD8052LVISO8	SOIC-8	Yes	Yes	-40°C to +85°C	Rail
AD8052LVISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
<b>AD8052LVIMP8X*</b>	MSOP-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1. \*Advance Information, contact CADEKA for availability.



## AD8052LV Pin Configuration

SOIC-8, MSOP-8



## AD8052LV Pin Assignments

SOIC-8, MSOP-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	-Vs	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	+Vs	Positive supply



## Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	+6	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V

## Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
8-Lead SOIC		100		°C/W
8-Lead MSOP		TBD		°C/W

Notes:

Package thermal resistance ( $\theta_{JA}$ ), JEDEC standard, multi-layer test boards, still air.

## ESD Protection

Product	SOIC-8	MSOP-8
Human Body Model (HBM)	2.5kV	TBD
Charged Device Model (CDM)	2kV	TBD

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		5.5	V



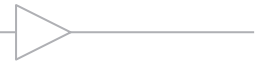
## Electrical Characteristics at 2.7V

$V_S = +2.7V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_S/2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth <sup>(2)</sup>	$G = +1$ , $V_{OUT} = 0.05V_{pp}$		215		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		85		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		36		MHz
GBWP	Gain Bandwidth Product			86		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time <sup>(2)</sup>	$V_{OUT} = 0.2V$ step		3.7		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 1V$ step		40		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		9		%
SR	Slew Rate	2.7V step, $G = -1$		130		V/ $\mu$ s
Distortion/Noise Response						
HD2	2nd Harmonic Distortion <sup>(2)</sup>	1V <sub>pp</sub> , 5MHz		79		dBc
HD3	3rd Harmonic Distortion <sup>(2)</sup>	1V <sub>pp</sub> , 5MHz		82		dBc
		1V <sub>pp</sub> , 5MHz		77		dB
$e_n$	Input Voltage Noise	> 1MHz		16		nV/ $\sqrt$ Hz
$i_n$	Input Current Noise	> 1MHz		1.3		pA/ $\sqrt$ Hz
X <sub>TALK</sub>	Crosstalk <sup>(1)</sup>	10MHz		65		dB
DC Performance						
$V_{IO}$	Input Offset Voltage			-1.6		mV
$dV_{IO}$	Average Drift			10		$\mu$ V/ $^{\circ}$ C
$I_b$	Input Bias Current			3		$\mu$ A
$dI_b$	Average Drift			7		nA/ $^{\circ}$ C
$I_{IO}$	Input Offset Current			0.1		$\mu$ A
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	DC	52	57		dB
$A_{OL}$	Open-Loop Gain			75		dB
$I_S$	Quiescent Current	Per Amplifier		3.9		mA
Input Characteristics						
$R_{IN}$	Input Resistance			4.3		M $\Omega$
$C_{IN}$	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, $V_{cm} = 0V$ to $V_S - 1.5$		87		dB
Output Characteristics						
$V_{OUT}$	Output Voltage Swing	$R_L = 10k\Omega$ to $V_S/2$		0.023 to 2.66		V
		$R_L = 2k\Omega$ to $V_S/2$		0.025 to 2.653		V
		$R_L = 150\Omega$ to $V_S/2$		0.065 to 2.55		V
$I_{OUT}$	Output Current			$\pm$ 55		mA
		-40 $^{\circ}$ C to +85 $^{\circ}$ C		$\pm$ 50		mA
$I_{SC}$	Short-Circuit Output Current			$\pm$ 85		mA
$V_S$	Power Supply Operating Range		2.5	2.7	5.5	V

### Notes:

- 100% tested at 25 $^{\circ}$ C.
- $R_f = 1k\Omega$  was used for optimal performance. (For  $G = +1$ ,  $R_f = 0$ ).



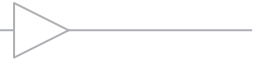
## Electrical Characteristics at 5V

$V_s = 5V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_s/2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth <sup>(2)</sup>	$G = +1$ , $V_{OUT} = 0.05V_{pp}$		260		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		90		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		40		MHz
GBWP	Gain Bandwidth Product			90		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time <sup>(2)</sup>	$V_{OUT} = 0.2V$ step		3.6		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2V$ step		40		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		7		%
SR	Slew Rate	5V step, $G = -1$		145		V/ $\mu$ s
Distortion/Noise Response						
HD2	2nd Harmonic Distortion <sup>(2)</sup>	$2V_{pp}$ , 5MHz		71		dBc
HD3	3rd Harmonic Distortion <sup>(2)</sup>	$2V_{pp}$ , 5MHz		78		dBc
		$2V_{pp}$ , 5MHz		70		dB
DG	Differential Gain	NTSC (3.85MHz), AC-Coupled, $R_L = 150\Omega$		0.06		%
		NTSC (3.85MHz), DC-Coupled, $R_L = 150\Omega$		0.08		%
DP	Differential Phase	NTSC (3.85MHz), AC-Coupled, $R_L = 150\Omega$		0.07		°
		NTSC (3.85MHz), DC-Coupled, $R_L = 150\Omega$		0.06		°
$e_n$	Input Voltage Noise	>1MHz		16		nV/ $\sqrt$ Hz
$i_n$	Input Current Noise	>1MHz		1.3		pA/ $\sqrt$ Hz
$X_{TALK}$	Crosstalk <sup>(2)</sup>	10MHz		62		dB
DC Performance						
$V_{IO}$	Input Offset Voltage <sup>(1)</sup>		-8	1.4	+8	mV
$dV_{IO}$	Average Drift			10		$\mu$ V/ $^{\circ}$ C
$I_b$	Input Bias Current <sup>(1)</sup>		-8	3	+8	$\mu$ A
$dI_b$	Average Drift			7		nA/ $^{\circ}$ C
$I_{IO}$	Input Offset Current <sup>(1)</sup>		-0.8	0.1	+0.8	$\mu$ A
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	DC	52	57		dB
$A_{OL}$	Open-Loop Gain <sup>(1)</sup>		68	78		dB
$I_S$	Quiescent Current <sup>(1)</sup>	Per Amplifier		4.2	5.2	mA
Input Characteristics						
$R_{IN}$	Input Resistance			4.3		M $\Omega$
$C_{IN}$	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio <sup>(1)</sup>	DC, $V_{cm} = 0V$ to $V_s - 1.5$	72	87		dB
Output Characteristics						
$V_{OUT}$	Output Voltage Swing	$R_L = 10k\Omega$ to $V_s/2$		0.027 to 4.97		V
		$R_L = 2k\Omega$ to $V_s/2$		0.036 to 4.953		V
		$R_L = 150\Omega$ to $V_s/2$ <sup>(1)</sup>	0.3	0.12 to 4.8	4.625	V
$I_{OUT}$	Output Current			$\pm 55$		mA
		-40 $^{\circ}$ C to +85 $^{\circ}$ C		$\pm 50$		mA
$I_{SC}$	Short-Circuit Output Current			$\pm 85$		mA
$V_s$	Power Supply Operating Range		2.5	5	5.5	V

### Notes:

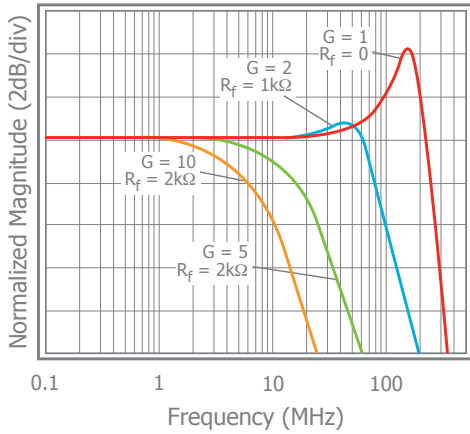
- 100% tested at 25 $^{\circ}$ C.
- $R_f = 1k\Omega$  was used for optimal performance. (For  $G = +1$ ,  $R_f = 0$ ).



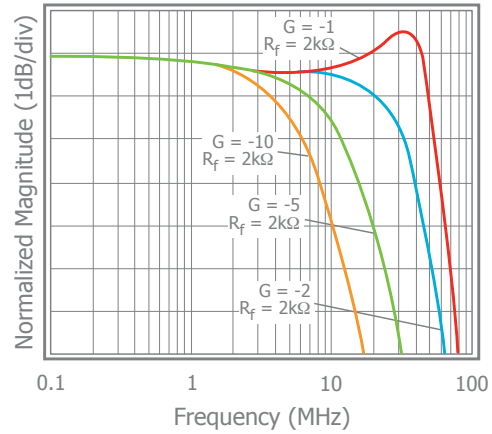
### Typical Performance Characteristics

$V_S = +5V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_S/2$ ; unless otherwise noted.

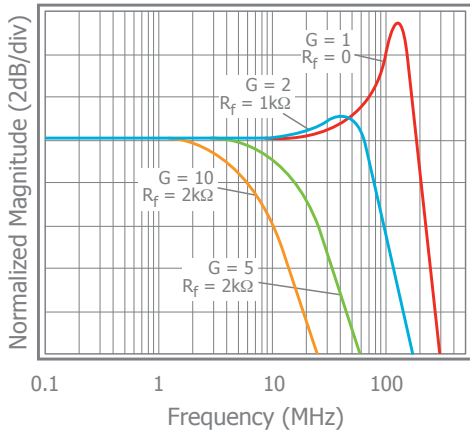
Non-Inverting Frequency Response  $V_S = +5V$



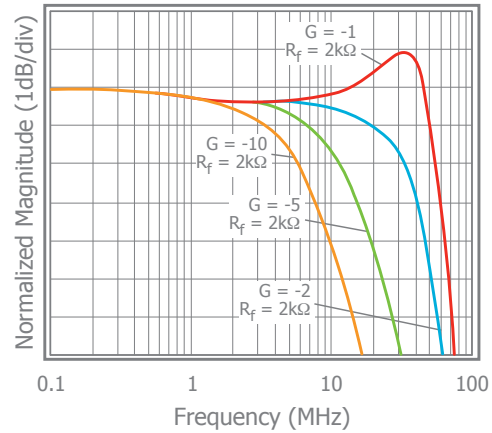
Inverting Frequency Response  $V_S = +5V$



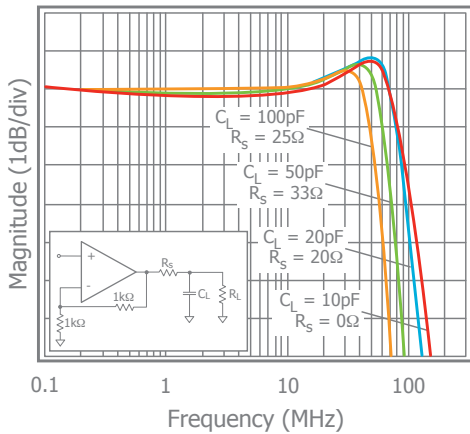
Non-Inverting Frequency Response  $V_S = +2.7V$



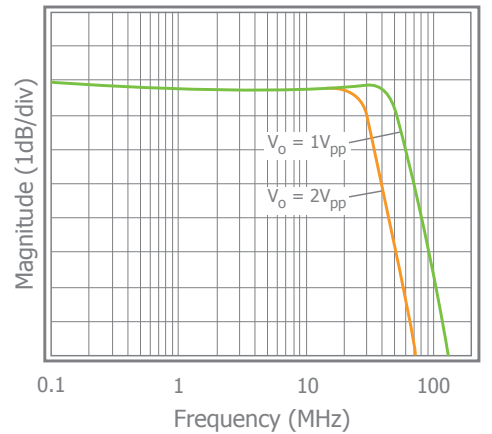
Inverting Frequency Response  $V_S = +2.7V$

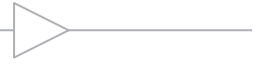


Frequency Response vs.  $C_L$



Large Signal Frequency Response

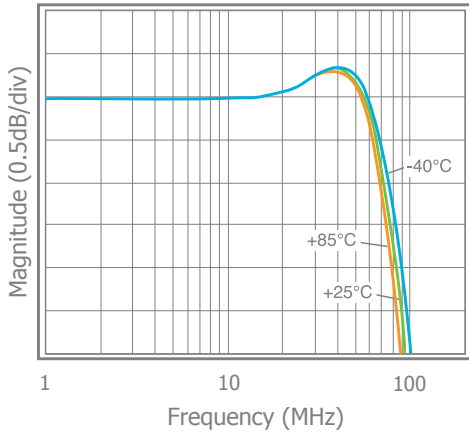




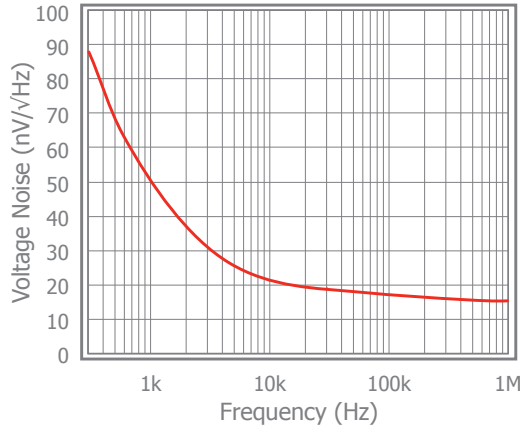
## Typical Performance Characteristics

$V_S = +5V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_S/2$ ; unless otherwise noted.

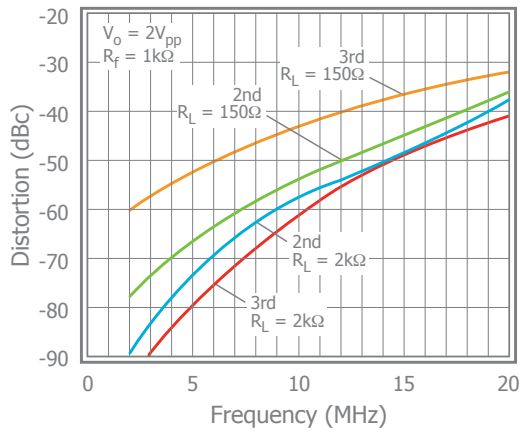
Frequency Response vs. Temperature



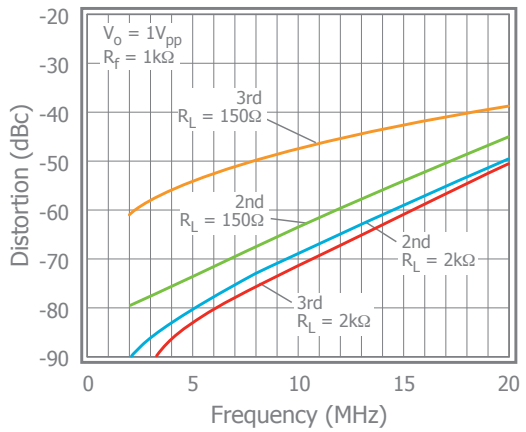
Input Voltage Noise



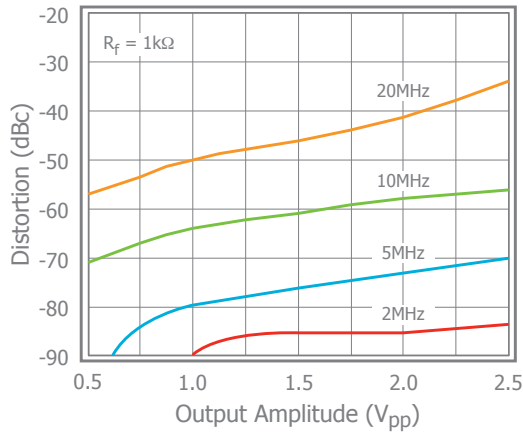
2nd & 3rd Harmonic Distortion;  $V_S = +5V$



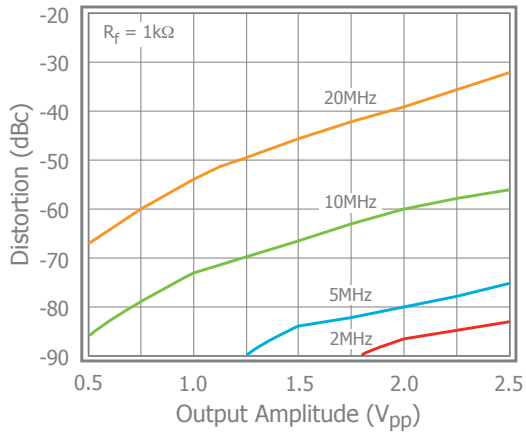
2nd & 3rd Harmonic Distortion;  $V_S = +2.7V$

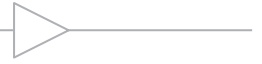


2nd Harmonic Distortion vs.  $V_O$



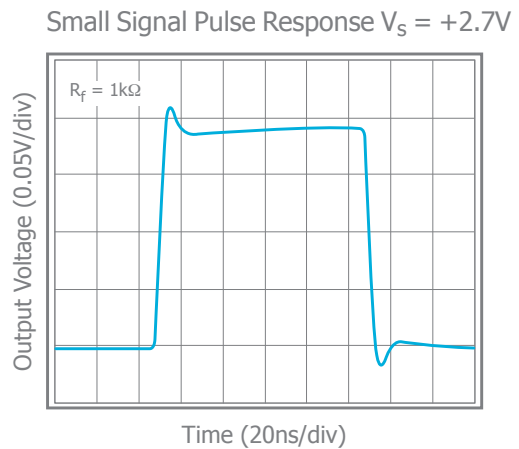
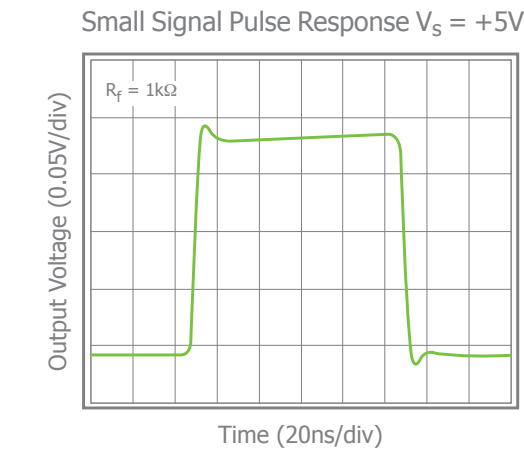
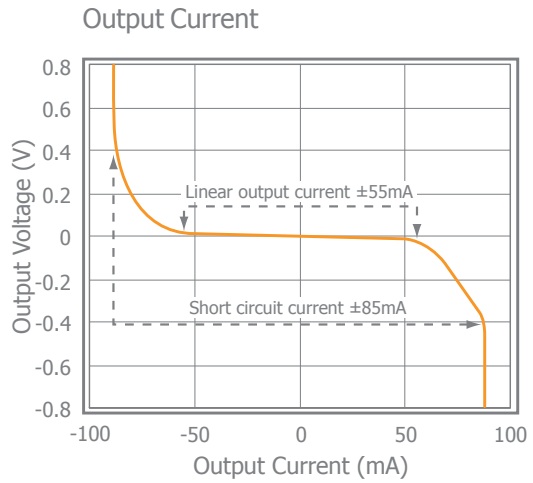
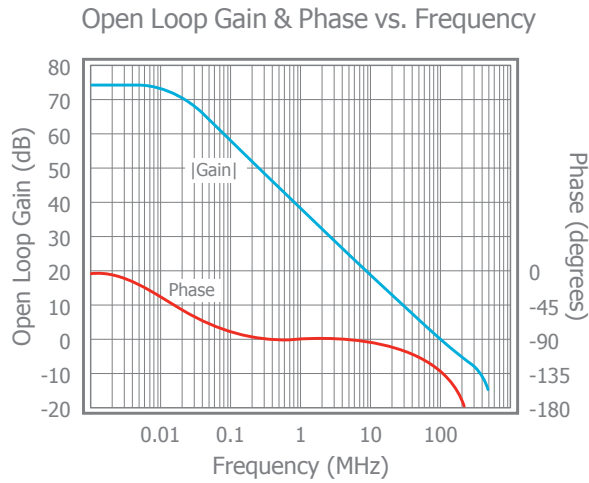
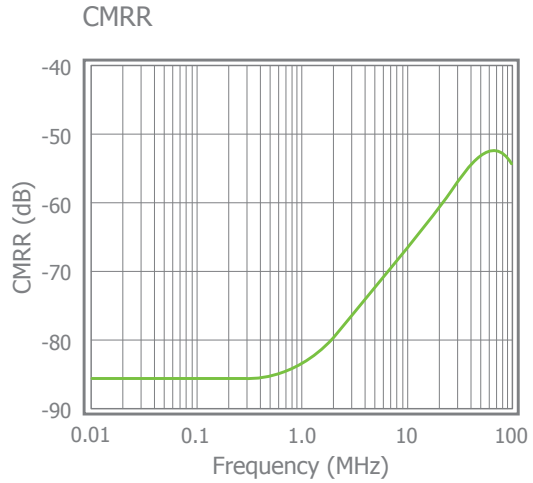
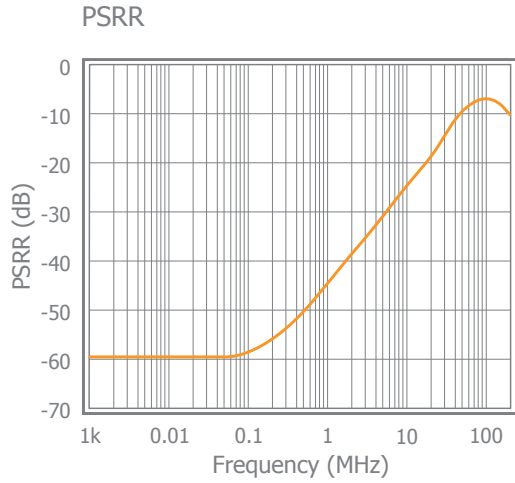
3rd Harmonic Distortion vs.  $V_O$

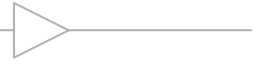




### Typical Performance Characteristics

$V_s = +5V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_s/2$ ; unless otherwise noted.

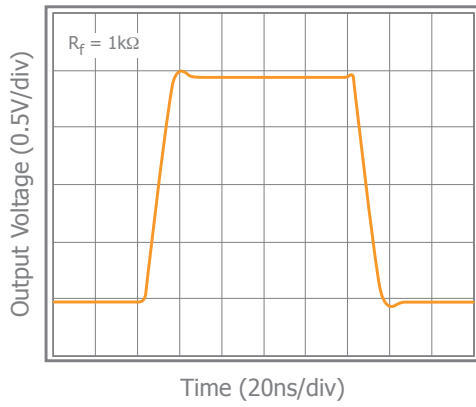




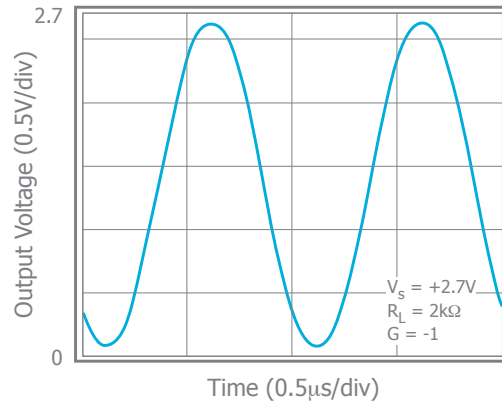
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$V_S = +5V$ ,  $G = 2$ ,  $R_f = 2k\Omega$ ,  $R_L = 2k\Omega$  to  $V_S/2$ ; unless otherwise noted.

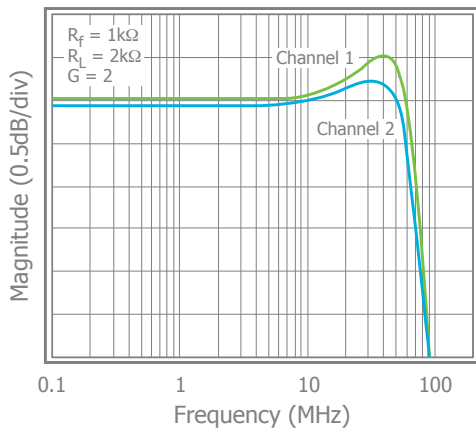
Large Signal Pulse Response  $V_S = +5V$



Output Swing



Channel Matching  $V_S = +5V$





## Application Information

### General Description

The AD8052LV is a single supply, general purpose, voltage-feedback amplifier fabricated on a complementary bipolar process using a patent pending topography. They feature a rail-to-rail output stage and is unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 1.2V below  $V_S$ . Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

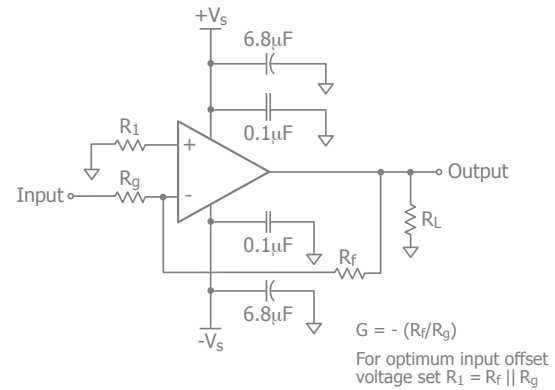


Figure 2. Typical Inverting Gain Circuit

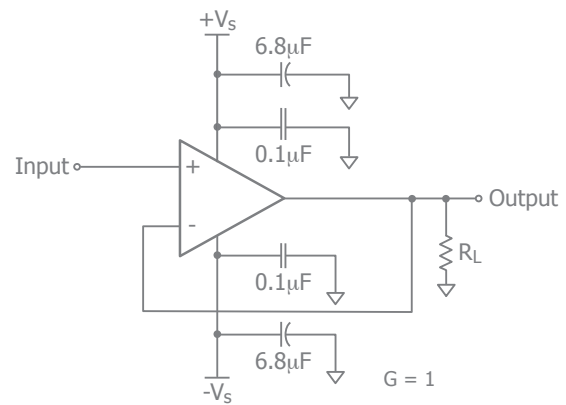


Figure 3. Unity Gain Circuit

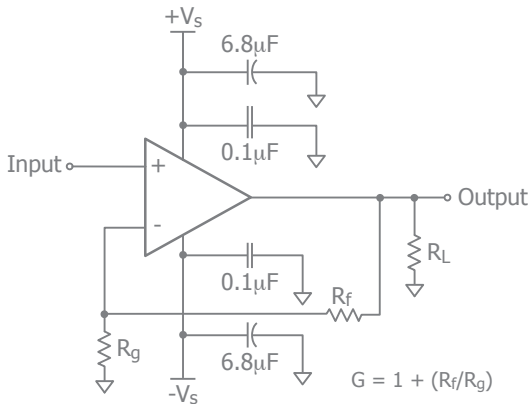


Figure 1. Typical Non-Inverting Gain Circuit

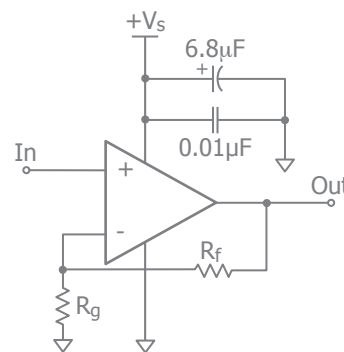


Figure 4. Single Supply Non-Inverting Gain Circuit



At non-inverting gains other than  $G = +1$ , keep  $R_g$  below  $1k\Omega$  to minimize peaking; thus, for optimum response at a gain of  $+2$ , a feedback resistor of  $1k\Omega$  is recommended. Figure 5 illustrates the AD8052LV frequency response with both  $1k\Omega$  and  $2k\Omega$  feedback resistors.

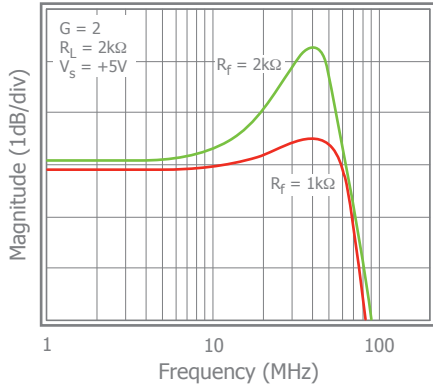


Figure 5: Frequency Response vs.  $R_f$

## Power Dissipation

Power dissipation should not be a factor when operating under the stated  $2k\Omega$  load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of  $150^\circ\text{C}$ . To calculate the junction temperature, the package thermal resistance value  $\Theta_{JA}$  ( $\Theta_{JA}$ ) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{JA} \times P_D)$$

Where  $T_{\text{Ambient}}$  is the temperature of the working environment.

In order to determine  $P_D$ , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}})^2 / R_{\text{load eff}}$$

The effective load resistor ( $R_{\text{load eff}}$ ) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$  in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here,  $P_D$  can be found from

$$P_D = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified  $I_S$  values along with known supply voltage,  $V_{\text{Supply}}$ . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{LOAD}})_{\text{RMS}} = V_{\text{PEAK}} / \sqrt{2}$$

$$(I_{\text{LOAD}})_{\text{RMS}} = (V_{\text{LOAD}})_{\text{RMS}} / R_{\text{load eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{DYNAMIC}} = (V_{S+} - V_{\text{LOAD}})_{\text{RMS}} \times (I_{\text{LOAD}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or  $V_{\text{supply}}/2$ .

The AD8052LV is short circuit protected. However, this may not guarantee that the maximum junction temperature ( $+150^\circ\text{C}$ ) is not exceeded under all conditions. Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

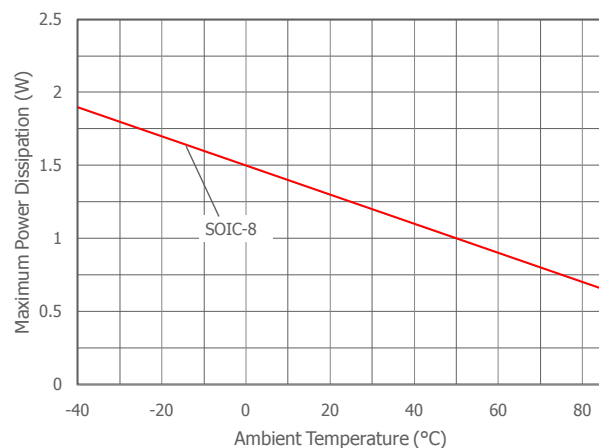


Figure 6. Maximum Power Derating



### Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance,  $R_S$ , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 7.

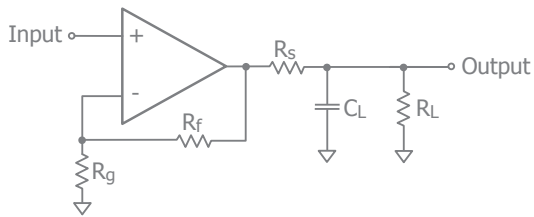


Figure 7. Addition of  $R_S$  for Driving Capacitive Loads

Table 1 provides the recommended  $R_S$  for various capacitive loads. The recommended  $R_S$  values result in approximately <1dB peaking in the frequency response.

$C_L$ (pF)	$R_S$ ( $\Omega$ )	-3dB BW (kHz)
10pF	0	100
20pF	20	94
50pF	33	72
100pF	25	58

Table 1: Recommended  $R_S$  vs.  $C_L$

For a given load capacitance, adjust  $R_S$  to optimize the tradeoff between settling time and bandwidth. In general, reducing  $R_S$  will increase bandwidth at the expense of additional overshoot and ringing.

### Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The AD8052LV will typically recover in less than 20ns from an overdrive condition. Figure 8 shows the AD8052LV in an overdriven condition.

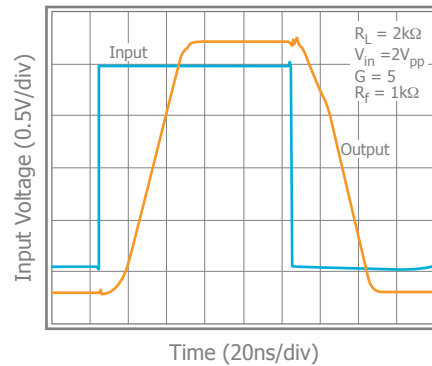


Figure 8. Overdrive Recovery

### Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

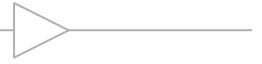
- Include 6.8 $\mu$ F and 0.1 $\mu$ F ceramic capacitors for power supply decoupling
- Place the 6.8 $\mu$ F capacitor within 0.75 inches of the power pin
- Place the 0.1 $\mu$ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

### Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	AD8052LV in SOIC
CEB010	AD8052LV in MSOP



Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-13. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -Vs pin of the amplifier is not directly connected to the ground plane.

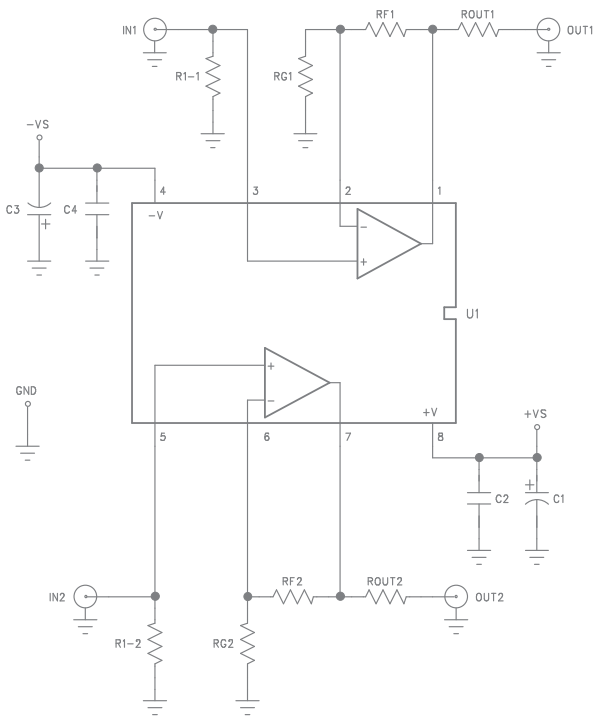


Figure 9. CEB006 & CEB010 Schematic

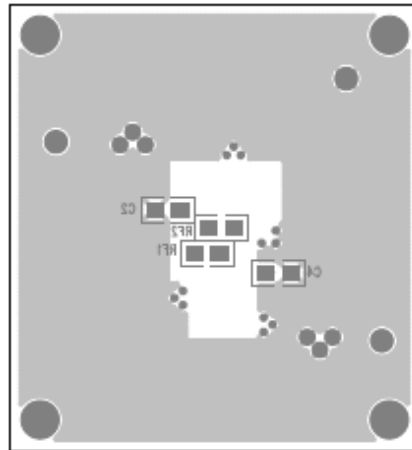


Figure 11. CEB006 Bottom View

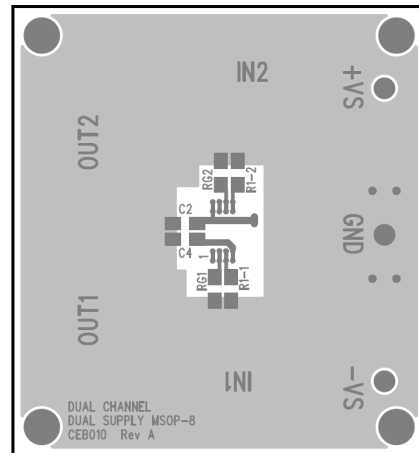


Figure 12. CEB010 Top View

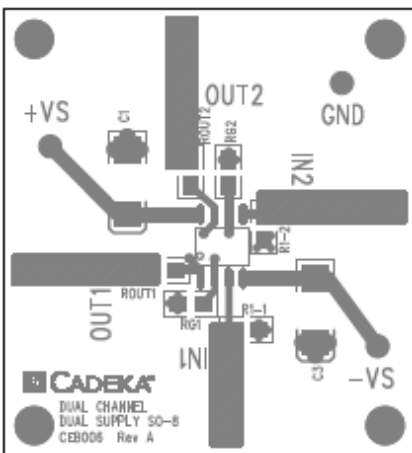


Figure 10. CEB006 Top View

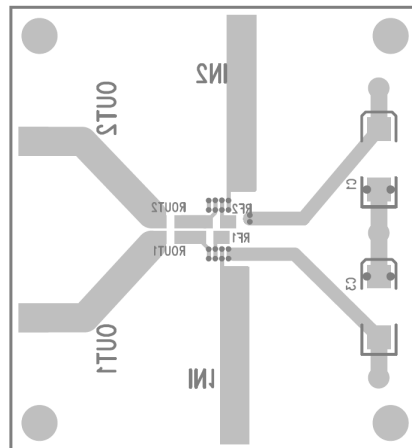
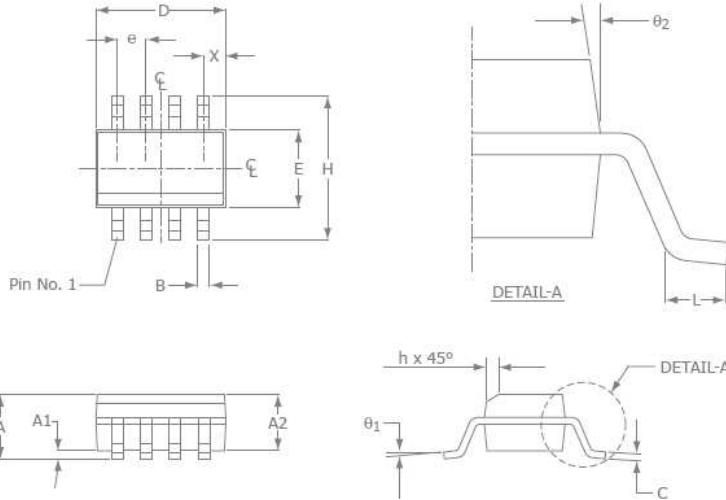


Figure 13. CEB010 Bottom View



## Mechanical Dimensions

### SOIC-8 Package

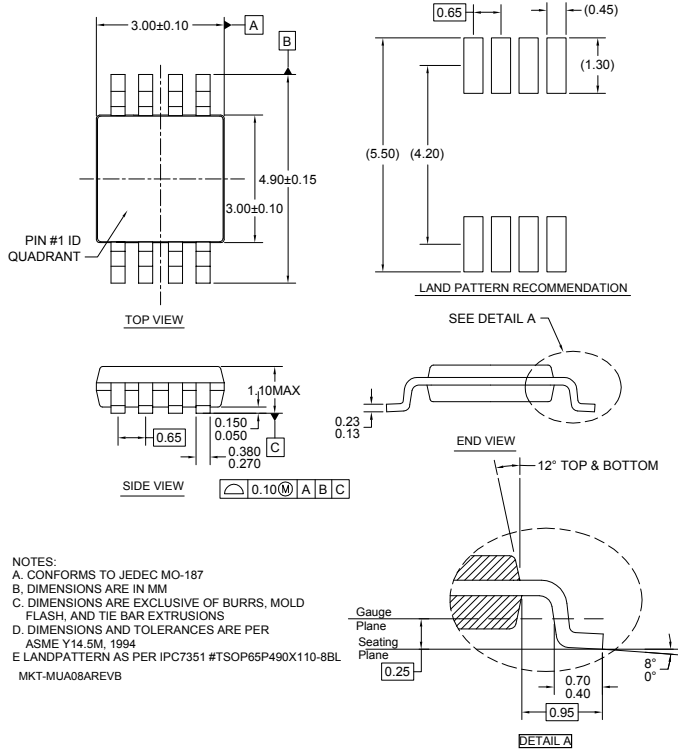


SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
theta <sub>1</sub>	0°	8°
X	0.55 ref	
theta <sub>2</sub>	7° BSC	

**NOTE:**

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

### MSOP-8 Package



NOTES:  
 A. CONFORMS TO JEDEC MO-187  
 B. DIMENSIONS ARE IN MM  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS  
 D. DIMENSIONS AND TOLERANCES ARE PER ASME Y14.5M, 1994  
 E. LANDPATTERN AS PER IPC7351 #TSOP65P490X110-8BLL MKT-MUA08AREVB

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