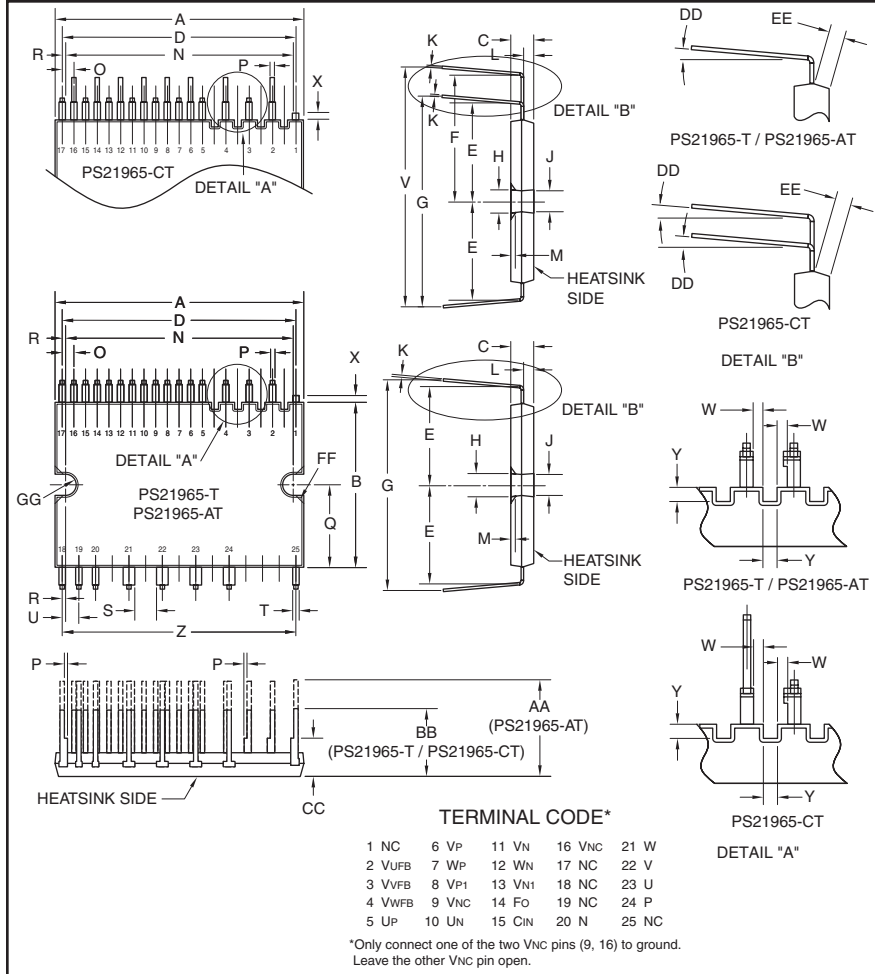


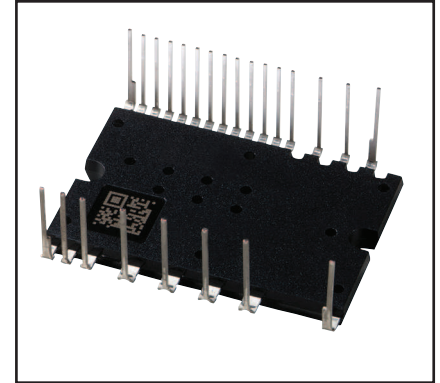
Intellimod™ Module Dual-In-Line Intelligent Power Module 20 Amperes/600 Volts



Outline Drawing and Circuit Diagram

Dimensions	Inches	Millimeters
A	1.50±0.02	38.0±0.5
B	0.94±0.02	24.0±0.5
C	0.14	3.5
D	1.40	35.56
E	0.57±0.02	14.4±0.5
F	0.74±0.02	18.9±0.5
G	1.15±0.02	29.2±0.5
H	0.14	3.5
J	0.13	3.3
K	0.016	0.4
L	0.06±0.02	1.5±0.05
M	0.031	0.8
N	1.39±0.019	35.0±0.3
O	0.07±0.008	1.778±0.2
P	0.02	0.5
Q	0.47	12.0

Dimensions	Inches	Millimeters
R	0.011	0.28
S	0.12	2.8
T	0.024	0.6
U	0.1±0.008	2.54±0.2
V	1.33±0.02	33.7±0.5
W	0.03	0.678
X	0.04	1.0
Y	0.05	1.2
Z	1.40	35.56
AA	0.55±0.02	14.0±0.5
BB	0.37±0.02	9.5±0.5
CC	0.22±0.02	5.5±0.5
DD	0 ~ 5°	0 ~ 5°
EE	0.06 MIN.	1.5 Min.
FF	0.05	1.2
GG	0.063 Rad.	1.6 Rad.



Description:

DIP-IPMs are intelligent power modules that integrate power devices, drivers, and protection circuitry in an ultra compact dual-in-line transfer-mold package for use in driving small three phase motors. Use of 5th generation IGBTs, DIP packaging, and application specific HVICs allow the designer to reduce inverter size and overall design time.

Features:

- Compact Packages
- Single Power Supply
- Integrated HVICs
- Direct Connection to CPU
- Reduced R_{th}

Applications:

- Refrigerators
- Air Conditioners
- Small Servo Motors
- Small Motor Control

Ordering Information:

PS21965-T is a 600V, 20 Ampere short pin DIP Intelligent Power Module.

PS21965-AT – long pin type
PS21965-CT – zigzag pin type

PS21965-T, PS21965-AT, PS21965-CT
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Absolute Maximum Ratings, $T_j = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	PS21965-T, PS21965-AT	
		PS21965-CT	Units
Power Device Junction Temperature*	T_j	-20 to 150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 to 125	$^\circ\text{C}$
Case Operating Temperature (Note 1)	T_C	-20 to 100	$^\circ\text{C}$
Mounting Torque, M3 Mounting Screws	—	6.9	in-lb
Module Weight (Typical)	—	10	Grams
Heatsink Flatness (Note 2)	—	-50 to 100	μm
Self-protection Supply Voltage Limit (Short Circuit Protection Capability)**	$V_{\text{CC(prot.)}}$	400	Volts
Isolation Voltage, AC 1 minute, 60Hz Sinusoidal, Connection Pins to Heatsink Plate	V_{ISO}	1500	Volts

*The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C ($@T_C \leq 100^\circ\text{C}$). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(\text{avg})} \leq 125^\circ\text{C}$ ($@T_C \leq 100^\circ\text{C}$).

** $V_D = 13.5 - 16.5\text{V}$, Inverter Part, $T_j = 125^\circ\text{C}$, Non-repetitive, Less than $2\mu\text{s}$

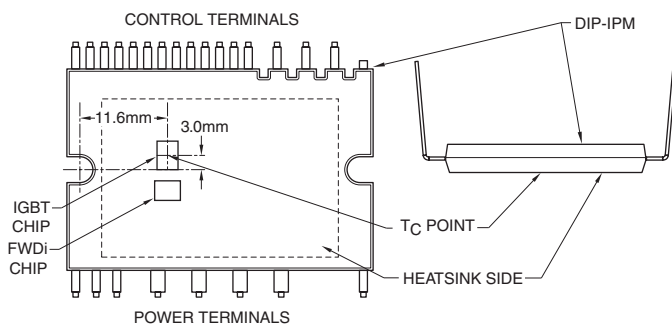
IGBT Inverter Sector

Collector-Emitter Voltage	V_{CES}	600	Volts
Each Collector Current, \pm ($T_C = 25^\circ\text{C}$)	I_C	20	Amperes
Each Peak Collector Current, \pm ($T_C = 25^\circ\text{C}$, Less than 1ms)	I_{CP}	40	Amperes
Supply Voltage (Applied between P - N)	V_{CC}	450	Volts
Supply Voltage, Surge (Applied between P - N)	$V_{\text{CC(surge)}}$	500	Volts
Collector Dissipation ($T_C = 25^\circ\text{C}$, per 1 Chip)	P_C	35.7	Watts

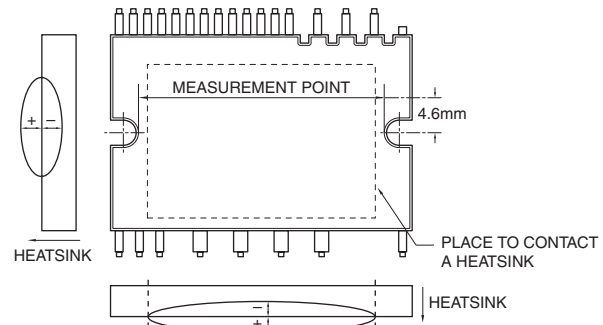
Control Sector

Supply Voltage (Applied between $V_{P1-V_{NC}}$, $V_{N1-V_{NC}}$)	V_D	20	Volts
Supply Voltage (Applied between V_{UFB-U} , V_{VFB-V} , V_{WFB-W})	V_{DB}	20	Volts
Input Voltage (Applied between U_P , V_P , W_P-V_{NC} , U_N , V_N , W_N-V_{NC})	V_{IN}	$-0.5 \sim V_D + 0.5$	Volts
Fault Output Supply Voltage (Applied between F_O-V_{NC})	V_{FO}	$-0.5 \sim V_D + 0.5$	Volts
Fault Output Current (Sink Current at F_O Terminal)	I_{FO}	1	mA
Current Sensing Input Voltage (Applied between $C_{\text{IN}}-V_{NC}$)	V_{SC}	$-0.5 \sim V_D + 0.5$	Volts

Note 1 – T_C Measure Point



Note 2 – Flatness Measurement Position





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Electrical and Mechanical Characteristics, $T_j = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
IGBT Inverter Sector						
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$V_D = V_{DB} = 15\text{V}, I_C = 20\text{A}, V_{IN} = 5\text{V}, T_j = 25^\circ\text{C}$	—	1.70	2.20	Volts
		$V_D = V_{DB} = 15\text{V}, I_C = 20\text{A}, V_{IN} = 5\text{V}, T_j = 125^\circ\text{C}$	—	1.80	2.30	Volts
Diode Forward Voltage	V_{EC}	$-I_C = 20\text{A}, V_{IN} = 0\text{V}$	—	1.90	2.40	Volts
Inductive Load Switching Times	t_{on}		0.70	1.30	1.90	μs
	t_{rr}	$V_{CC} = 300\text{V}, V_D = V_{DB} = 15\text{V},$	—	0.30	—	μs
	$t_{C(on)}$	$I_C = 20\text{A}, T_j = 125^\circ\text{C},$	—	0.50	0.75	μs
	t_{off}	$V_{IN} = 0 \leftrightarrow 5\text{V}, \text{Inductive Load},$	—	1.60	2.20	μs
	$t_{C(off)}$		—	0.40	0.75	μs
Collector Cutoff Current	I_{CES}	$V_{CE} = V_{CES}, T_j = 25^\circ\text{C}$	—	—	1.0	mA
		$V_{CE} = V_{CES}, T_j = 125^\circ\text{C}$	—	—	10	mA

Control Sector

Circuit Current	I_D	$V_{IN} = 5\text{V}$	Total of $V_{P1-V_{NC}}, V_{N1-V_{NC}}$	—	—	2.80	mA
			$V_{UFB-U}, V_{VFB-V}, V_{WFB-W}$	—	—	0.55	mA
		$V_{IN} = 0\text{V}$	Total of $V_{P1-V_{NC}}, V_{N1-V_{NC}}$	—	—	2.80	mA
			$V_{UFB-U}, V_{VFB-V}, V_{WFB-W}$	—	—	0.55	mA
Fault Output Voltage	V_{FOH}	$V_{SC} = 0\text{V}, F_O \text{ Terminal Pull-up to } 5\text{V by } 10\text{k}\Omega$	4.9	—	—	Volts	
	V_{FOL}	$V_{SC} = 1\text{V}, I_{FO} = 1\text{mA}$	—	—	0.95	Volts	
Input Current	I_{IN}	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
Short Circuit Trip Level*	$V_{SC(ref)}$	$V_D = 15\text{V}^*$	0.43	0.48	0.53	Volts	
Over-Temperature Trip Level**	OT_t	$V_D = 15\text{V}, \text{At Temperature of LVIC}$	(100)	(120)	(140)	$^\circ\text{C}$	
Over-Temperature Trip/Reset Level	OT_{rh}	$V_D = 15\text{V}, \text{At Temperature of LVIC}$	—	(10)	—	$^\circ\text{C}$	
Supply Circuit Under-voltage	UV_{DBt}	Trip Level, $T_j \leq 125^\circ\text{C}$	10.0	—	12.0	Volts	
	UV_{DBr}	Reset Level, $T_j \leq 125^\circ\text{C}$	10.5	—	12.5	Volts	
	UV_{Dt}	Trip Level, $T_j \leq 125^\circ\text{C}$	10.3	—	12.5	Volts	
	UV_{Dr}	Reset Level, $T_j \leq 125^\circ\text{C}$	10.8	—	13.0	Volts	
Fault Output Pulse Width***	t_{FO}		20	—	—	μs	
ON Threshold Voltage	$V_{th(on)}$	Applied between	—	2.1	2.6	Volts	
OFF Threshold Voltage	$V_{th(off)}$	$U_P, V_P, W_P-V_{NC},$	0.8	1.3	—	Volts	
ON/OFF Threshold Hysteresis Voltage	$V_{th(hys)}$	U_N, V_N, W_N-V_{NC}	0.35	0.65	—	Volts	

* Short Circuit protection is only for the lower-arms. Please select the external shunt resistance such that the S_C trip level is less than 1.7 times the current rating.

**Over-temperature protection (OT) outputs a fault signal when the LVIC temperature exceeds the OT trip temperature level (OT_t). In that case if the heatsink comes off or becomes loosely fixed, do not reuse the DIP-IPM. (There is a possibility that junction temperature of power chips exceeded maximum T_j (150°C)).

***Fault signal is asserted only for a S_C , a U_V , or an OT failure on the low side. The F_O pulse width is different for each failure mode. For a S_C failure, F_O output is 20 μsec (min). For a U_V or OT failure, F_O output will be asserted as long as the U_V or OT exists or for 20 μsec , whichever is longer.



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Thermal Characteristics

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Junction to Case	$R_{th(j-c)Q}$	Inverter IGBT (Per 1/6 Module)	—	—	2.8	°C/Watt
	$R_{th(j-c)D}$	Inverter FWDi (Per 1/6 Module)	—	—	3.9	°C/Watt

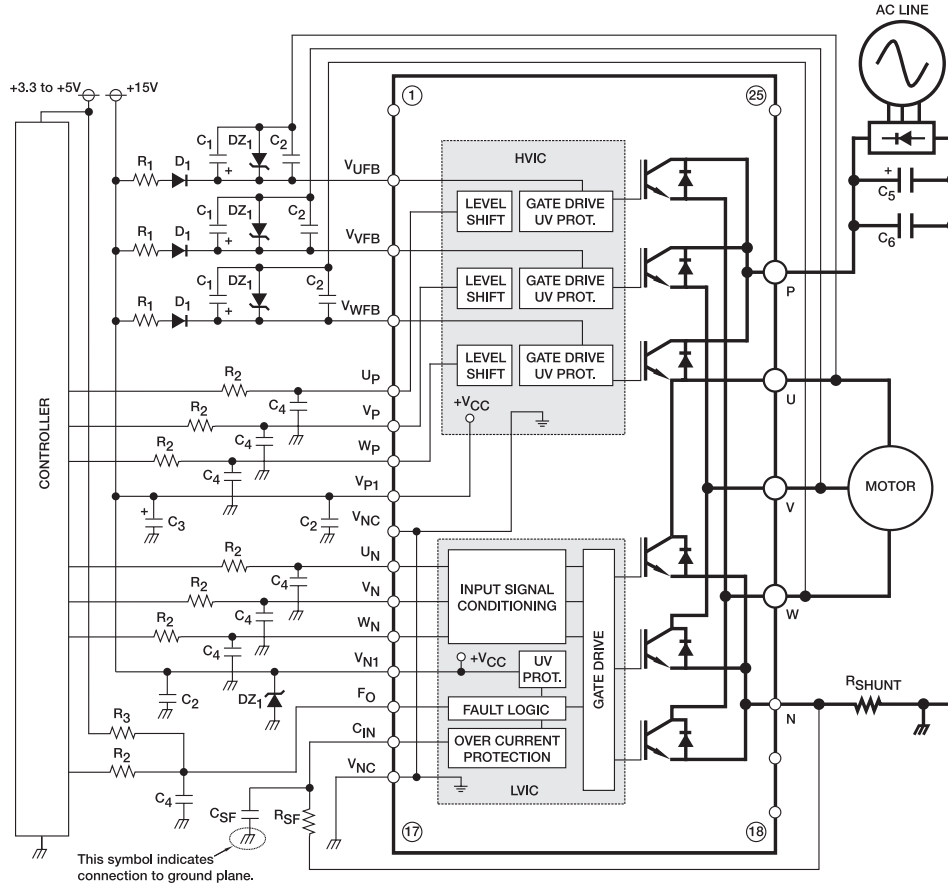
Recommended Conditions for Use

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Applied between P-N Terminals	0	300	400	Volts
Control Supply Voltage	V_D	Applied between V_{P1} - V_{NC} , V_{N1} - V_{NC}	13.5	15.0	16.5	Volts
	V_{DB}	Applied between V_{UFB-U} , V_{VFB-V} , V_{WFB-W}	13.0	15.0	18.5	Volts
Control Supply Variation	dV_D , dV_{DB}		-1	—	1	V/ μ s
Arm Shoot-through Blocking Time	t_{DEAD}	For Each Input Signal, $T_C \leq 100^\circ\text{C}$	1.5	—	—	μ s
Allowable Minimum Input	$P_{WIN(on)}$		0.5	—	—	μ s
Pulse Width*	$P_{WIN(off)}$		0.5	—	—	μ s
V_{NC} Voltage Variation	V_{NC}	Between V_{NC-N} (Including Surge)	-5.0	—	5.0	Volts

*DIP-IPM might not make response or work properly if the input signal pulse width is less than the recommended minimum value.

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Application Circuit



Component Selection:

Dsgn.	Typ. Value	Description
D1	1A, 600V	Boot strap supply diode – Ultra fast recovery
DZ1	24V, 1.0W	Control and boot strap supply over voltage suppression
C1	10-100uF, 50V	Boot strap supply reservoir – Electrolytic, long life, low Impedance, 105°C (Note 5)
C2	0.22-2.0uF, 50V	Local decoupling/High frequency noise filters – Multilayer ceramic (Note 8)
C3	10-100uF, 50V	Control power supply filter – Electrolytic, long life, low Impedance, 105°C
C4	100pF, 50V	Optional Input signal noise filter – Multilayer ceramic (Note 1)
C5	200-2000uF, 450V	Main DC bus filter capacitor – Electrolytic, long life, high ripple current, 105°C
C6	0.1-0.22uF, 450V	Surge voltage suppression capacitor – Polyester/Polypropylene film (Note 9)
CSF	1000pF, 50V	Short circuit detection filter capacitor – Multilayer Ceramic (Note 6, Note 7)
RSF	1.8k ohm	Short circuit detection filter resistor (Note 6, Note 7)
RSHUNT	5-100mohm	Current sensing resistor – Non-inductive, temperature stable, tight tolerance (Note 10)
R1	10 ohm	Boot strap supply inrush limiting resistor (Note 5)
R2	330 ohm	Optional control input noise filter (Note 1, Note 2)
R3	10k ohm	Fault output signal pull-up resistor (Note 3)

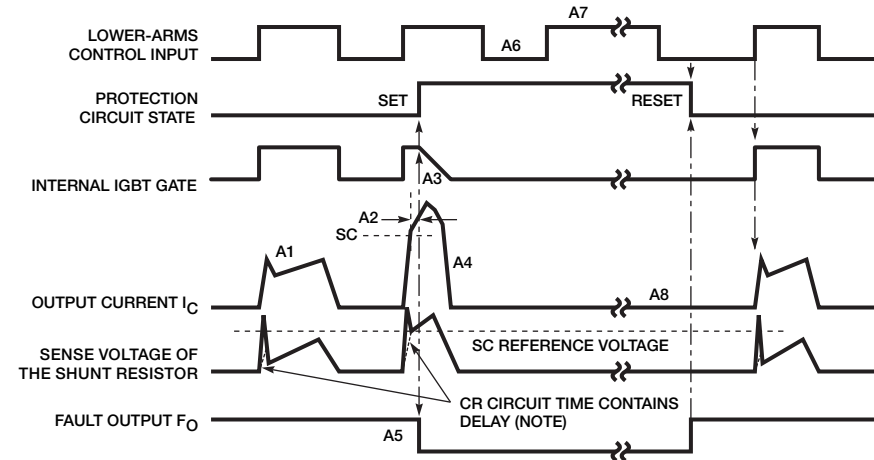
Notes:

- 1) To prevent input signal oscillations minimize wiring length to controller (~2cm). Additional RC filtering (C5 etc.) may be required. If filtering is added be careful to maintain proper dead time and voltage levels. See application notes for details.
- 2) Internal HVIC provides high voltage level shifting allowing direct connection of all six driving signals to the controller.
- 3) FO output is an open collector type. Pull up resistor (R3) should be adjusted to current sink capability of the controller.
- 4) Use only one VNC Pin (either 9 or 16) and leave the other open.
- 5) Boot strap supply component values must be adjusted depending on the PWM frequency and technique.
- 6) Wiring length associated with RSHUNT, RSF, CSF must be minimized to avoid improper operation of the OC function.
- 7) RSF, CSF set over current protection trip time. Recommend time constant is 1.5µs-2.0µs. See application notes.
- 8) Local decoupling/high frequency filter capacitors must be connected as close as possible to the modules pins.
- 9) The length of the DC link wiring between C5, C6, the DIP's P terminal and the shunt must be minimized to prevent excessive transient voltages. In particular C6 should be mounted as close to the DIP as possible.
- 10) Use high quality, tight tolerance current sensing resistor. Connect resistor as close as possible to the DIP's N terminal. Be careful to check for proper power rating. See application notes for calculation of resistance value.

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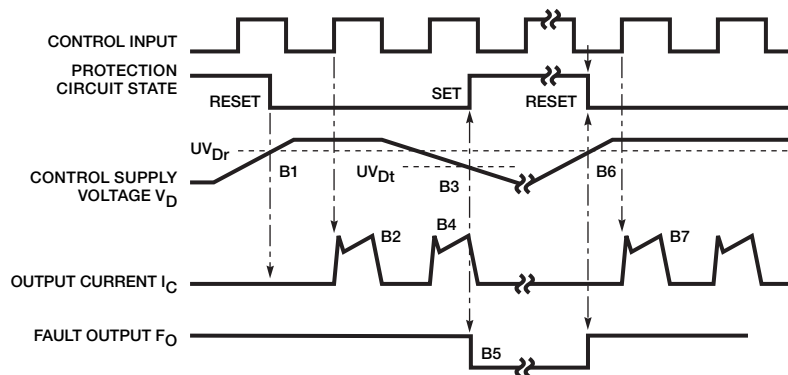
Protection Function Timing Diagrams

Short-Circuit Protection (Lower-arms only with the external shunt resistor and RC filter)



- A1: Normal operation – IGBT turn on and conducting current.
- A2: Short-circuit current detected (SC trigger).
- A3: IGBT gate hard interrupted.
- A4: IGBT turn off.
- A5: F_O output with a fixed pulse width of $t_{FO(min)} = 20\mu s$.
- A6: Input "L" – IGBT off.
- A7: Input "H" – IGBT on is blocked during the F_O output period.
- A8: IGBT stays in off state.

Under-Voltage Protection (Lower-side, UV_D)

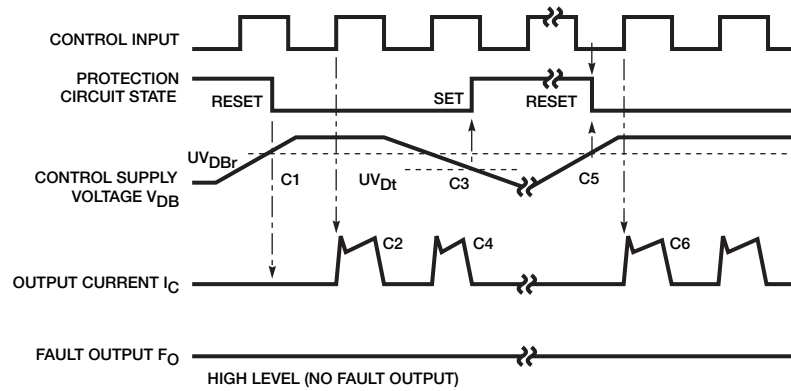


- B1: Control supply voltage rise – After the voltage level reaches UV_{Dr} , the drive circuit begins to work at the rising edge of the next input signal.
- B2: Normal operation – IGBT turn on and conducting current.
- B3: Under-voltage trip (UV_{Dt}).
- B4: IGBT turn off regardless of the control input level.
- B5: F_O output during under-voltage period, however, the minimum pulse width is 20µs.
- B6: Under-voltage reset (UV_{Dr}).
- B7: Normal operation – IGBT turn on and conducting current.

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Protection Function Timing Diagrams

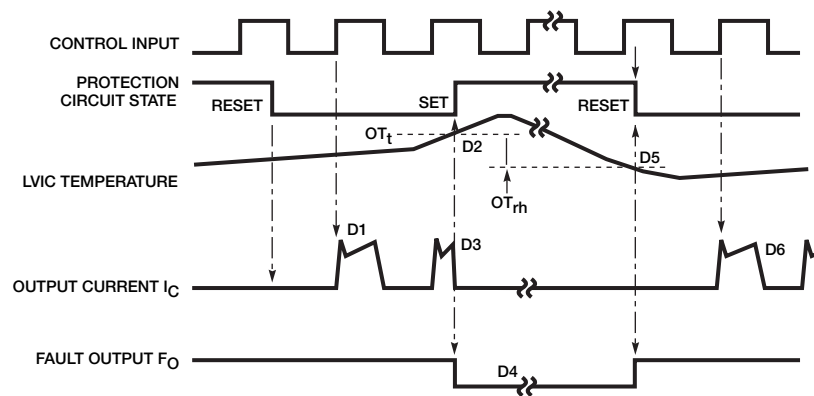
Under-Voltage Protection (Upper-side, UV_{DB})



- C1: Control supply voltage rises – After the voltage level reaches UV_{DBr} , the drive circuit begins to work at the rising edge of the next input signal.
- C2: Normal operation – IGBT turn on and conducting current.
- C3: Under-voltage trip (UV_{DBt}).
- C4: IGBT stays off regardless of the control input level, but there is no F_O signal output.
- C5: Under-voltage reset (UV_{Dr}).
- C6: Normal operation – IGBT turn on and conducting current.

Over-Temperature Protection Timing Diagram

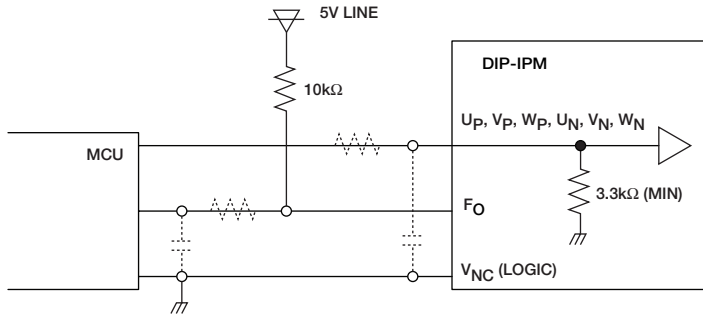
Over-Temperature Protection (Lower -side, OT)



- D1: Normal operation – IGBT ON and carrying current.
- D2: LVIC temperature exceeds over-temperature trip level (OT_t).
- D3: IGBT OFF in spite of control input condition.
- D4: F_O outputs during over-temperature period, however, the minimum pulse is $20\mu s$.
- D5: LVIC temperature falls below over-temperature reset level.
- D6: Circuits start to operate normally when next input is applied.

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Typical Interface Circuit



NOTE: RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. The DIP-IPM input signal section integrates a $3.3k\Omega$ (min) pull-down resistor. Therefore, when using an external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

Wiring Method Around Shunt Resistor

