

■ Features, Benefits and Applications

- Any frequency between 80.000001 and 220 MHz with 6 decimal places of accuracy
- 100% pin-to-pin drop-in replacement to quartz based VCXO
- Frequency stability as low as ± 10 PPM
- Widest pull range options from ± 25 PPM to ± 1600 PPM
- Superior pull range linearity of $\leq 1\%$, 10 times better than quartz
- LVCMOS/LVTTL compatible output
- Three industry-standard packages: 3.2 mm x 2.5 mm (4-pin), 5.0 mm x 3.2 mm (6-pin), 7.0 mm x 5.0 mm (6-pin)
- Ideal for telecom clock synchronization, instrumentation, low bandwidth analog PLL, jitter cleaner, clock recovery, audio, video, FPGA, broadband and networking

■ Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	80.000001	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of Initial tolerance ^[1] at 25 °C, operating temperature, rated supply voltage variation and load variation (15% pF $\pm 10\%$)
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	2.97	3.3	3.63	V	Contact SiTime for any other voltage support between 2.5V and 3.3V
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
		1.71	1.8	1.89	V	
Pull Range ^[2,3]	PR	$\pm 25, \pm 50, \pm 100, \pm 150, \pm 200, \pm 400, \pm 800, \pm 1600$			PPM	
Upper Control Voltage	VC_U	1.7	–	–	V	Vdd = 1.8 V, Voltage at which maximum deviation is guaranteed.
		2.4	–	–	V	Vdd = 2.5 V, Voltage at which maximum deviation is guaranteed.
		2.7	–	–	V	Vdd = 2.8 V, Voltage at which maximum deviation is guaranteed.
		3.2	–	–	V	Vdd = 3.3 V, Voltage at which maximum deviation is guaranteed.
Lower Control Voltage	VC_L	–	–	0.1	V	Voltage at which minimum deviation is guaranteed.
Control Voltage Input Impedance	Z_vin	100	–	–	k Ω	For the voltage control pin
Linearity	Lin	–	0.1	1	%	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage Bandwidth(-3dB)	V_BW	–	8	–	kHz	Contact SiTime for 16 kHz and other high bandwidth options
Current Consumption	Idd	–	34	36	mA	No load condition, f = 100 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	30	33	mA	No load condition, f = 100 MHz, Vdd = 1.8 V
Standby Current	I_std	–	–	70	μ A	All Vdds, ST = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	f \leq 165 MHz, all Vdds.
		40	–	60	%	f > 165 MHz, all Vdds.
Rise/Fall Time	Tr, Tf	–	1.5	2	ns	Vdd = 1.8, 2.5, 2.8 or 3.3 V, 10% - 90% Vdd level
Output Voltage High	VOH	90%	–	–	Vdd	OH = -7 mA, IOL = 7 mA, (Vdd = 3.3 V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8 V)
Input Pull-up Impedance	Z_in	–	100	250	k Ω	For the OE/ST pin if available
Start-up Time	T_start	–	6	10	ms	
OE Enable/Disable Time	T_oe	–	–	150	ns	f = 100 MHz, all Vdds. For other freq, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	–	10	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	1.5	2	ps	f = 156.25 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	2	3	ps	f = 156.25 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.5	1	ps	f = 156.25 MHz, Integration bandwidth = 12kHz to 20MHz, All Vdds
Aging	F_aging	–	–	± 5	PPM	10 years

Notes:

1. Initial tolerance is measure at Vin = Vdd/2
2. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
3. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)
4. All electrical specifications in the above table are measured with 15pF output load. Contact SiTime for higher drive options.

■ Specifications (Cont.)

Pin Description Tables (4-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change

Pin Map	
Pin	Connection
1	VIN
2	GND
3	CLK
4	Vdd

Pin Description Tables (6-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change
Pin #2 Functionality
NC
H or L or Open: No effect on output frequency or other device functions
OE
H or Open ^[5] : specified frequency output
L: output is high impedance
ST
H or Open ^[3] : specified frequency output
L: output is low level (weak pull down). Oscillation stops

Pin Map	
Pin	Connection
1	VIN
2	NC/OE/ \overline{ST}
3	GND
4	CLK
5	NC
6	Vdd

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	-	6000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	°C
Number of Program Writes	-	1	NA
Program Retention over -40 to 125°C, Process, Vdd (0 to 3.65 V)	1,000+	-	years

Environmental Compliance

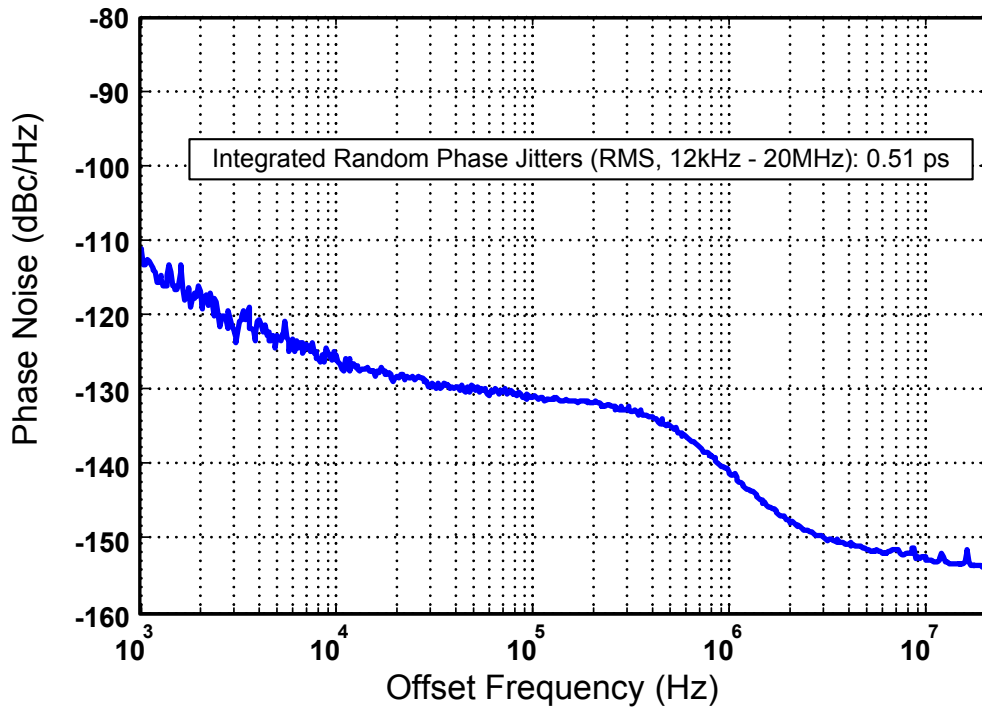
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002; 50kG
Mechanical Vibration	MIL-STD-883F, Method 2007; 70G
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

Notes:

5. A resistor of <100 kΩ between OE/ \overline{ST} pin and VDD is recommended for all voltages.

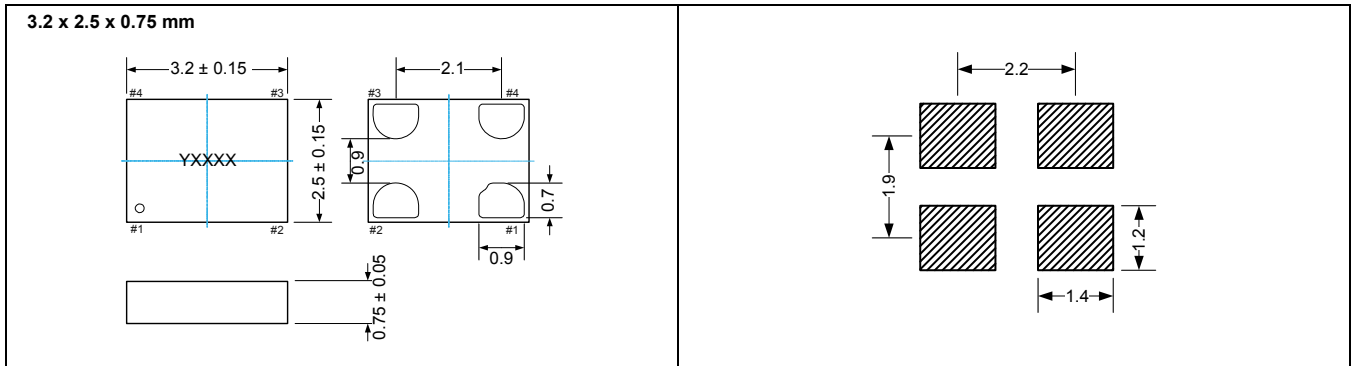
Phase Noise Plot

SiT3809, 100MHz, Pull range ± 100 ppm, 3.3V, LVCMOS output

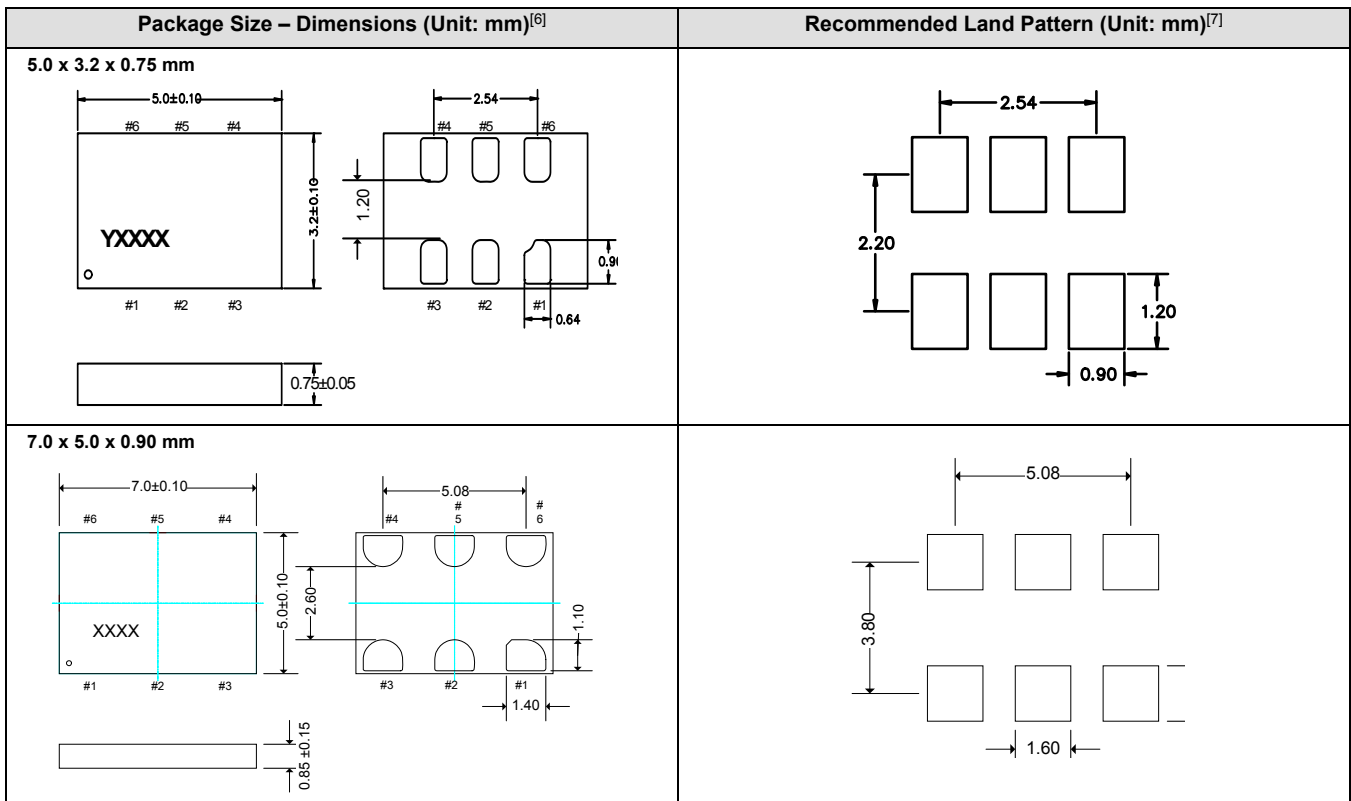


■ Dimensions and Land Patterns

Packages (4-pin device)



Packages (6-pin device)

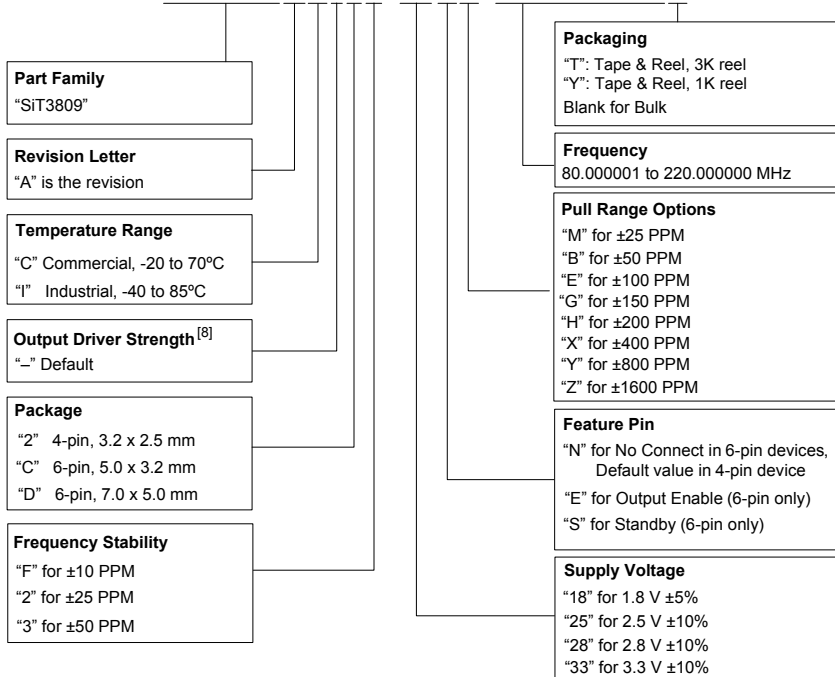


Notes:

6. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
7. A capacitor of value 0.1 μ F between Vdd and GND is recommended.

Part No. Guide - How to Order

SiT3809AC-2F-33EH-108.123456T



APR Definition

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_{stab}) - Aging (F_{aging})

APR Table

Nominal Pull Range	Frequency Stability		
	± 10	± 25	±50
	APR (PPM)		
± 25	± 10	—	—
± 50	± 35	± 20	—
± 100	± 85	± 70	± 45
± 150	± 135	± 120	± 95
± 200	± 185	± 170	± 145
± 400	± 385	± 370	± 345
± 800	± 785	± 770	± 745
± 1600	± 1585	± 1570	± 1545

Note:

8. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.

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