

SiT3821

1-220 MHz High Performance Differential VCXO



Features

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- Widest pull range options: ± 25 , ± 50 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600 PPM
- Superior pull range linearity of $\leq 1\%$, 10 times better than quartz
- 0.6ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 5.0 mm x 3.2 mm and 7.0 mm x 5.0 mm
Contact SiTime for 3.2 mm x 2.5 mm package
- For frequencies higher than 220 MHz, refer to SiT3822 datasheet

Applications

- Ideal for SONET, Video, Instrumentation, Satellite applications
- Telecom, networking, broadband



EXPRESS
SAMPLES



GREEN
SOLUTIONS



QUARTZ
FREE

Electrical Characteristics

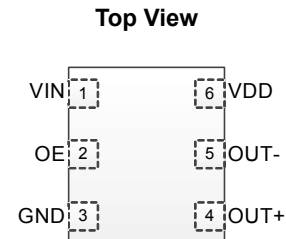
Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common AC Characteristics						
Output Frequency Range	f	1	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power, supply voltage and load change
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	–	10	ms	
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
Pull Range	PR	± 25 , ± 50 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600			PPM	See the last page for Absolute Pull Range, APR table
Upper Control Voltage	VC_U	3.2	–	–	V	Vdd = 3.3V, Voltage at which maximum deviation is guaranteed
		2.4	–	–	V	Vdd = 2.5V, Voltage at which maximum deviation is guaranteed
Lower Control Voltage	VC_L	–	–	0.1	V	Voltage at which maximum deviation is guaranteed
Linearity	Lin	–	–	1	%	
Frequency Change Polarity	–	Positive Slope			–	
Control Voltage Bandwidth (-3dB)	V_BW	–	8	–	kHz	Contact SiTime for 16 kHz or other high bandwidth options
Vin Pin Input Impedance	Z_vin	100	–	–	k Ω	Pin 1
First Year Aging		-2	–	+2	PPM	25°C
10-year Aging		-5	–	+5	PPM	25°C
LVPECL, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	μ A	OE = Low
Maximum Output Current	I-driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

Electrical Characteristics

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS, DC, and AC Characteristics						
Supply Voltage	V _{dd}	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	I _{dd}	–	47	55	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Current	I _{OE}	–	–	35	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	–	1	μA	OE = Low
Differential Output Voltage	V _{OD}	200	350	500	mV	See Figure 4
V _{OD} Magnitude Change	ΔV _{OD}	–	–	50	mV	See Figure 4
Offset Voltage	V _{OS}	1.125	1.2	1.375	V	See Figure 4
V _{OS} Magnitude Change	ΔV _{OS}	–	–	50	mV	See Figure 4
Rise/Fall Time	T _r , T _f	–	495	600	ps	20% to 80%
OE Enable/Disable Time	T _{oe}	–	–	115	ns	f = 220 MHz - For other frequencies, T _{oe} = 100ns + 3 period
RMS Period Jitter	T _{jitt}	–	1.2	1.7	ps	f = 100 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, V _{DD} = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, V _{DD} = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V _{dds}

Pin Description

Pin	Map	Functionality	
1	VIN	Input	Control Voltage
2	OE	Input	H or Open: specified frequency output L: output is high impedance
3	GND	Power	V _{DD} Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage



Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
V _{DD}	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Termination Diagrams

LVPECL:

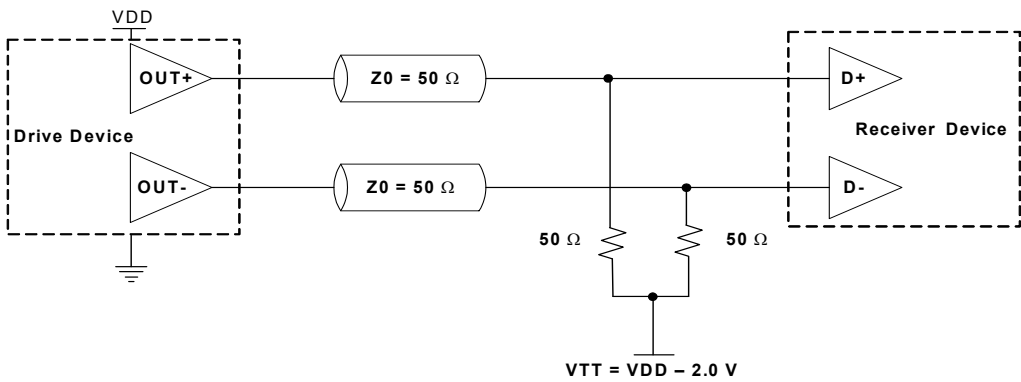


Figure 1. LVPECL Typical Termination

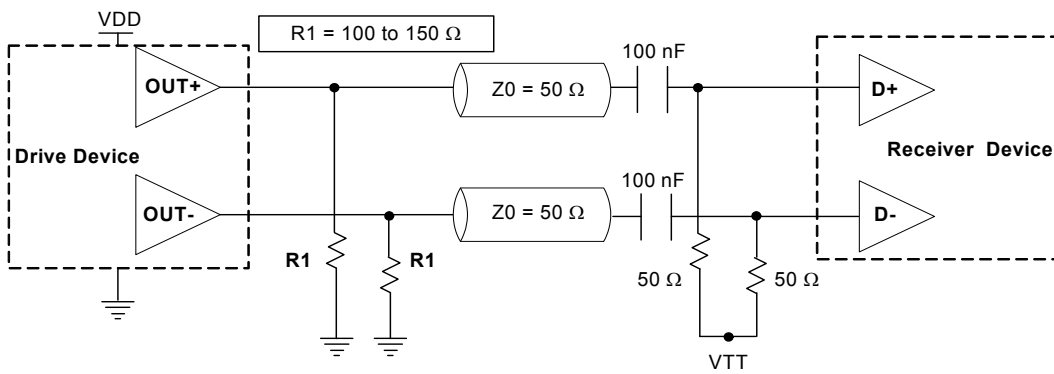


Figure 2. LVPECL AC Coupled Termination

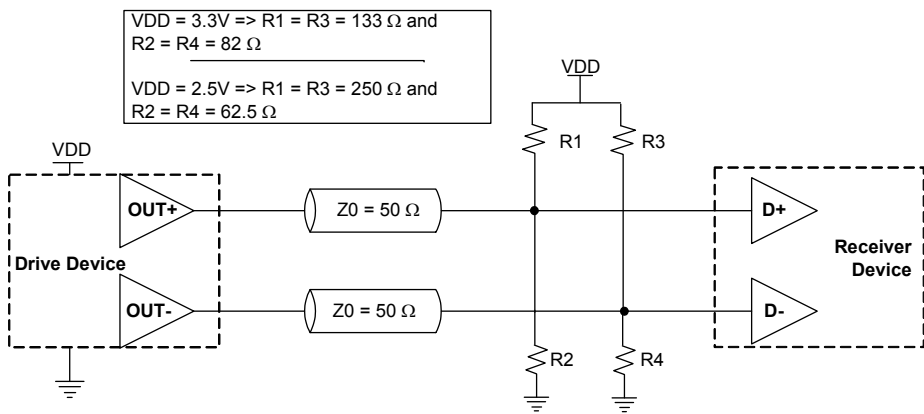


Figure 3. LVPECL with Thevenin Typical Termination

LVDS:

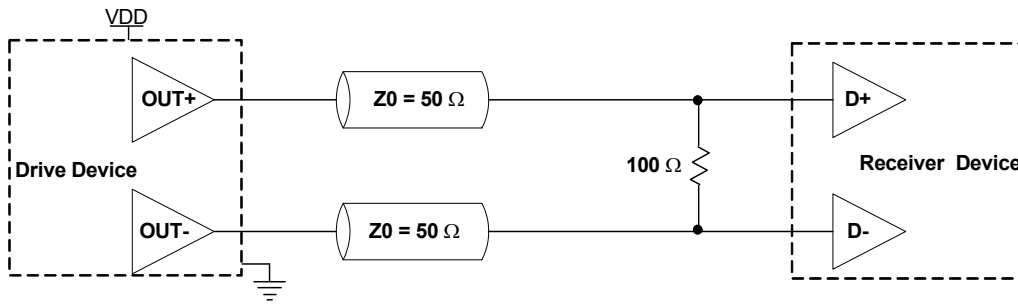
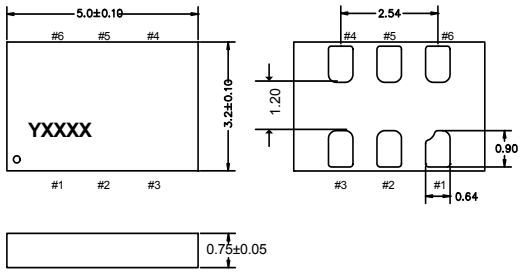
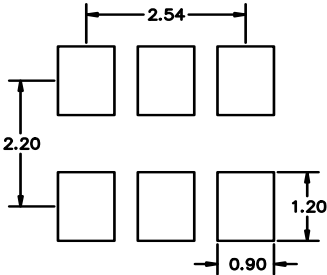
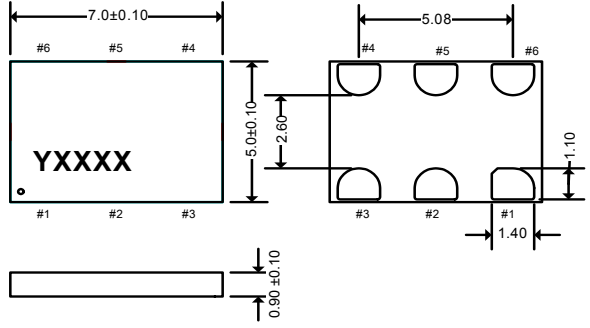
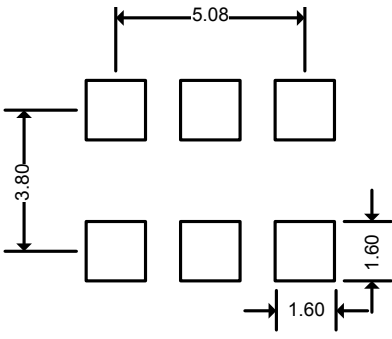


Figure 4. LVDS Single Termination (Load Terminated)

SiT3821

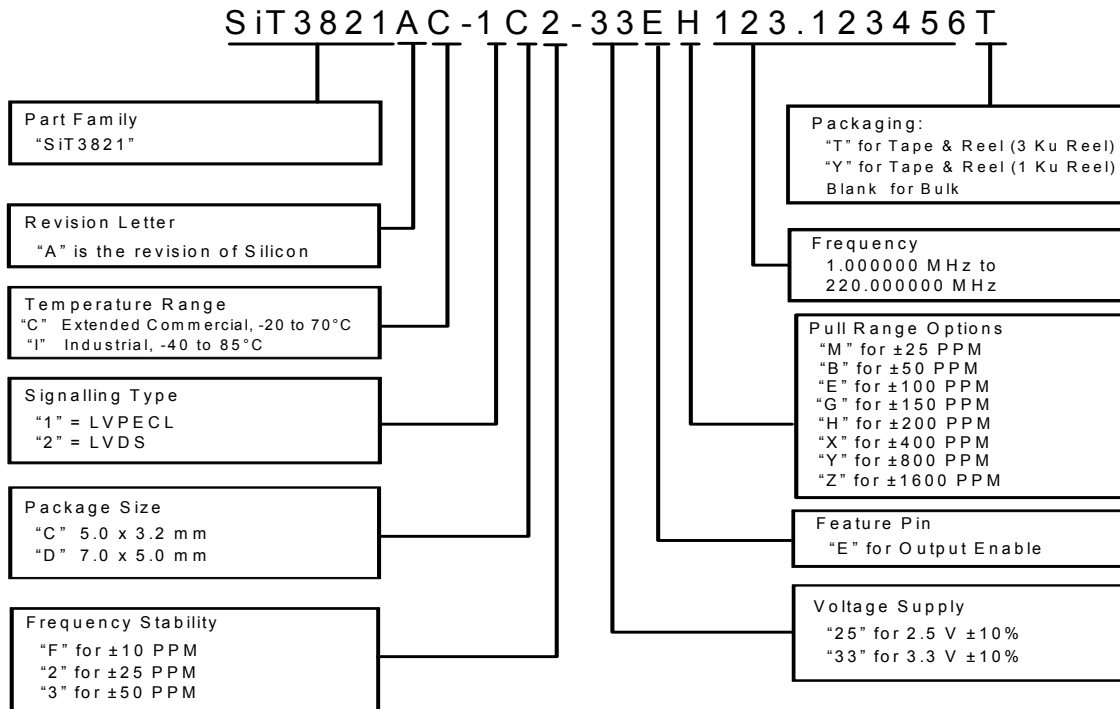
1-220 MHz High Performance Differential VCXO

Dimensions and Patterns

Package Size – Dimensions (Unit: mm) ^[1]	Recommended Land Pattern (Unit: mm) ^[2]
<p>5.0 x 3.2 x 0.75 mm</p>  <p>Top view shows a rectangular package with dimensions 5.0±0.10 mm by 3.2±0.10 mm. Pin locations are marked #1 to #6. The top marking 'YXXXX' is shown. A side view shows a height of 0.75±0.05 mm. The recommended land pattern shows a 2x3 grid of pads with a pitch of 2.54 mm and a pad width of 0.90 mm.</p>	 <p>The recommended land pattern for the 5.0 x 3.2 x 0.75 mm package shows a 2x3 grid of pads. The pitch between pads is 2.54 mm. The pad width is 0.90 mm. The distance from the left edge to the first pad is 2.20 mm. The distance from the bottom edge to the first pad is 1.20 mm.</p>
<p>7.0 x 5.0 x 0.90 mm</p>  <p>Top view shows a rectangular package with dimensions 7.0±0.10 mm by 5.0±0.10 mm. Pin locations are marked #1 to #6. The top marking 'YXXXX' is shown. A side view shows a height of 0.90±0.10 mm. The recommended land pattern shows a 2x3 grid of pads with a pitch of 5.08 mm and a pad width of 1.60 mm.</p>	 <p>The recommended land pattern for the 7.0 x 5.0 x 0.90 mm package shows a 2x3 grid of pads. The pitch between pads is 5.08 mm. The pad width is 1.60 mm. The distance from the left edge to the first pad is 3.80 mm. The distance from the bottom edge to the first pad is 1.60 mm.</p>

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1 μF between Vdd and GND is recommended.

Ordering Information



APR Definition

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

APR Table

Nominal Pull Range	Frequency Stability		
	± 10	± 25	± 50
	APR (PPM)		
± 25	± 10	—	—
± 50	± 35	± 20	—
± 100	± 85	± 70	± 45
± 150	± 135	± 120	± 95
± 200	± 185	± 170	± 145
± 400	± 385	± 370	± 345
± 800	± 785	± 770	± 745
± 1600	± 1585	± 1570	± 1545

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