

S6000 Family

The Stretch® S6000 family of software configurable processors is designed to handle compute-intensive video, imaging, and wireless applications. The architecture, based on the Xtensa® LX Processor, provides the compute power needed for digital signal and application layer processing. The processor core contains a second-generation Instruction Set Extension Fabric (ISEF), which is used to optimize the instruction set for specific applications in real time. An integrated Programmable Accelerator is optimized for algorithms commonly used in audio, video, and wireless applications. Both the S6100 and the S6105 contain an integrated Processor Array (PA) interface to provide glueless chip to chip communication for board level scalability. The S6106 and S6107 are designed without a PA interface, and are optimized for single-chip applications where low power consumption and a small physical footprint are design requirements.

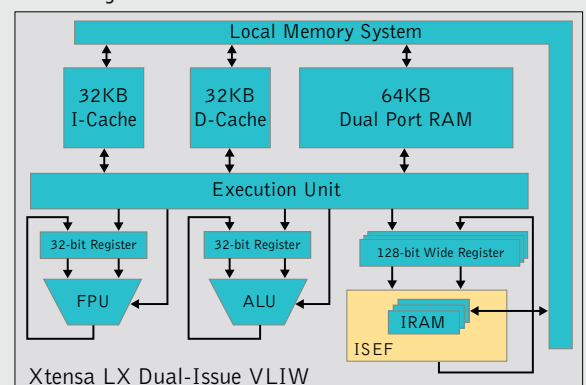
Key Features

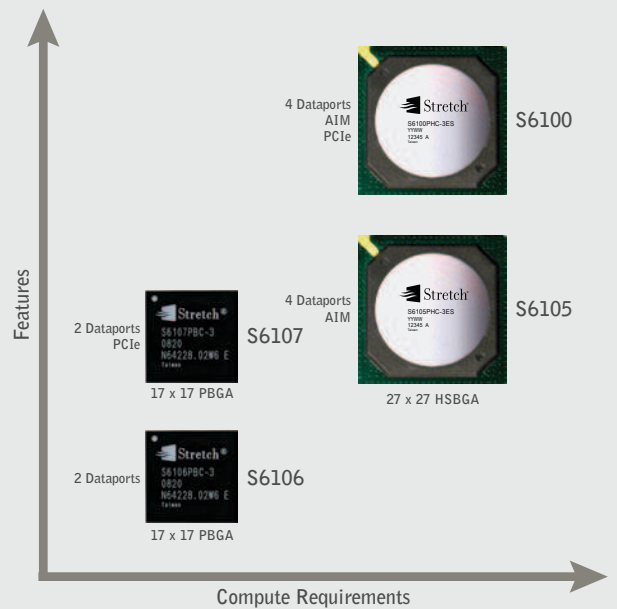
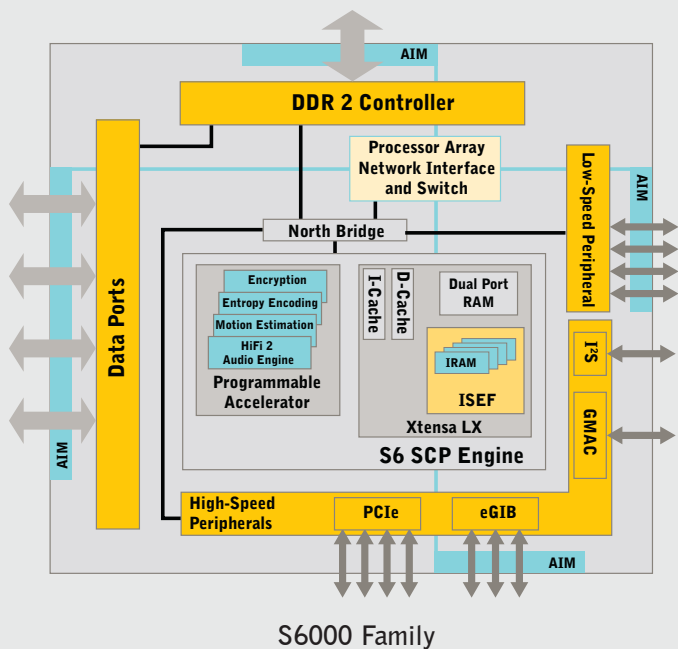
- S6 Software Configurable Processor
 - › Second-generation Instruction Set Extension Fabric (ISEF)
 - S6100 and S6105 – 345MHz operation
 - S6106 and S6107 – 167MHz operation
 - 64KB ISEF embedded RAM (IRAM)
 - Direct DMA
 - Fully pipelined and interlocked
 - › Dual issue VLIW with 16-, 24-, and 64-bit instructions
 - › Single-precision floating point operations
- Programmable Accelerator
 - › Optimized for audio, video, and wireless
- Peripherals
 - › S6100 and S6105 – Four 10-bit Data Ports
 - › S6106 and S6107 – Two 10-bit Data Ports
 - › All Data Ports support multiple modes, including
 - Video SD (BT 656) and HD (BT 1120)—interleaved or progressive
 - Flow-controlled FIFO mode—8/10 bit or 16/20 bit
 - Raw data—8/10 bit
 - Streaming mode
 - › One PCIe port supporting
 - x1 and x4 on S6100
 - x1 on S6107)
 - › S6100 and S6105 – One 16/32-bit DDR2 333–667 SDRAM port
 - › S6106 and S6107 – One 16-bit DDR2 333–500 SDRAM port
 - › One 10/100/1000 Ethernet MAC port
 - › One Enhanced Generic Interface Bus (eGIB)
 - › Two programmable serial ports
 - Two-wire Interface (TWI)
 - Serial Peripheral Interface (SPI)
 - › Two I²S audio ports
 - › Two UART ports with IrDA
 - › General Purpose I/O (GPIO) and Interrupts
 - › One standard test port supporting JTAG IEEE 1149.1

S6000 FAMILY ADVANTAGES

- › Dramatically boosts system performance in compute-intensive applications by:
 - › Customizing the S6 Software Configurable Processor (S6SCP) instruction set
 - › Leveraging the pre-optimized applications for the Programmable Accelerator
- › S6100 and S6105 provide board-level scalability via the Processor Array
- › S6106 and S6107 provide breakthrough performance with low power and small physical footprint
- › Provides high-performance I/Os and flexible video/data ports for highly integrated system design

S6 Software Configurable Processor





S6000 Family Features vs. Application Compute Requirements

The S6 SCP Engine

The S6000 family of processors is powered by the Stretch S6 SCP Engine, which incorporates the popular Tensilica® Xtensa LX dual issue VLIW processor core and the powerful second-generation Stretch Instruction Set Extension Fabric (ISEF). The ISEF is a software configurable compute fabric that contains 64KB of embedded RAM (IRAM). Using the ISEF, system designers extend the processor instruction set and define new instructions using only their C/C++ code. As a result, developers get the performance of custom hardware with C/C++ development simplicity—achieving unprecedented performance, easy and rapid development, and significant cost savings. Stretch’s S6 SCP Engine unlocks the two major RISC bottlenecks to provide an unparalleled level of performance:

Granularity of computations—Unlike typical RISC processors’ ALUs that perform low level operations such as shift, add, and multiply, the ISEF can execute thousands of operations as a single instruction.

Data bandwidth—The S6 SCP Engine uses 32 128-bit wide registers to feed data to the ISEF. A DMA controller also allows data to be transferred to and from the IRAM in the background with zero processor overhead.

Package

- S6100 and S6105 – HSBGA — 27mm x 27mm
- S6106 and S6107 – PBGA — 17mm x 17mm

Stretch Inc.

1322 Orleans Dr.
 Sunnyvale, CA 94089
 tel 408.543.2700 • fax 408.747.5736
 www.stretchinc.com

Stretch Advantage

How This is Achieved

High Compute Performance	Second generation ISEF with embedded IRAM delivers highly accelerated performance through Instruction Extensions
Board Level Scalability	The Processor Array, standard on the S6100 and S6105, provides a glueless, high-speed interface for creating arrays of processors to satisfy the compute requirements of the most demanding applications
Low System Cost	A rich I/O set with high-speed data ports ensures seamless connectivity with system elements such as image sensors, video encoders, and digital-to-analog converters for radio applications
Design Flexibility	Developers use C/C++ to program the processor and configure the ISEF with custom instructions. Configurability enables application flexibility, allowing developers to respond to emerging standards, add new features, and support new algorithms with no redesign
Low Power Consumption	The S6106 and S6107 are optimized for low power consumption in single chip applications. Power consumption is dramatically reduced by exploiting the application acceleration capability of the ISEF

All information contained in this document is subject to change without notice. For more information, visit our web site at www.stretchinc.com
 © 2009, Stretch Inc. All rights reserved. Stretch, the Stretch logo and Extending the Possibilities are registered trademarks of Stretch Inc.