



150mA Ultra-Low Dropout Adjustable and Fixed Regulators

Features

- Stable with 2.2uF Low ESR Ceramic Capacitor
- Voltage Reference Accuracy of 2%
- Wide Operating Range: 2.5V ~ 14V
- Quiescent Current 5uA in Shutdown
- Current Limit and Thermal Shutdown
- Logic Input Enable Pin
- RoHS-compliant, Halogen-free SOT-23-5 Package

Description

The APU8852-3 is an efficient linear voltage regulator with better than 2% initial voltage accuracy, very low dropout voltage and very low ground current designed especially for hand-held, battery powered applications. Other features of the device are TTL compatible enable/shutdown control input, current limiting and thermal shutdown.

The APU8852-3 is available in both fixed and adjustable output voltage versions in a small SOT-23 5-pin package.

Applications

- Laptop, Notebook and Palmtop computers
- Battery Powered Equipments
- PCMCIA Vcc and Vpp Regulator
- Consumer Electronics
- High Efficiency Linear Power Supplies

Typical Application

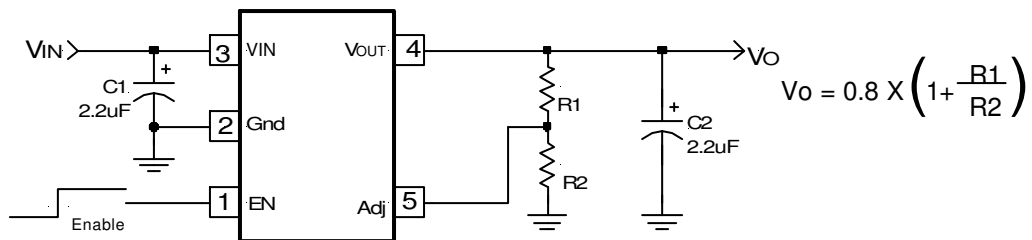


Figure 1 - Typical application of the APU8852-3 adjustable voltage regulator.

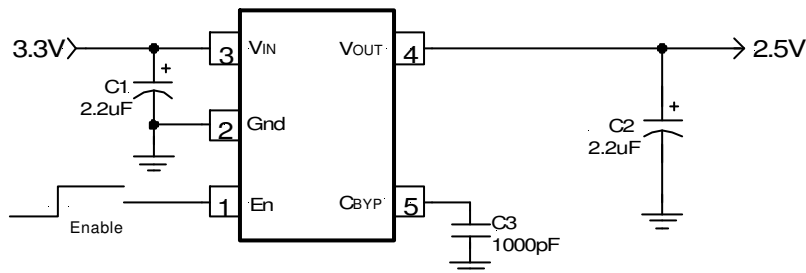


Figure 2 - Typical application of the APU8852-25-3 fixed voltage regulator.

Ordering information

T _J (°C)	5-PIN SOT-23-5	OUTPUT VOLTAGE
0 To 125	APU8852Y5-HF-3TR	Adj
0 To 125	APU8852Y5-18-HF-3TR	1.8V
0 To 125	APU8852Y5-25-HF-3TR	2.5V
0 To 125	APU8852Y5-28-HF-3TR	2.8V
0 To 125	APU8852Y5-30-HF-3TR	3.0V
0 To 125	APU8852Y5-33-HF-3TR	3.3V

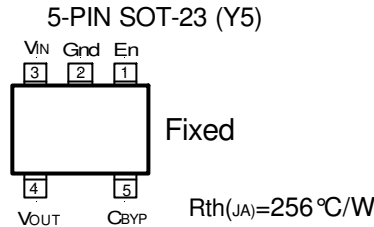
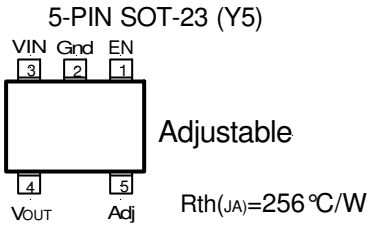
Products in 5-pin SOT-23-5 are shipped on tape and reel, 3000 pieces per reel. The device is rated MSL3 for moisture sensitivity, and the reel is shipped sealed inside a moisture barrier bag.



Absolute Maximum Ratings

Input Voltage (V_{IN})	16V
Enable Input Voltage	16V
Storage Temperature Range	-65°C to 150°C
Operating Junction Temperature Range	0°C to 150°C

Pin Configuration



Electrical Specifications

Unless otherwise specified, these specifications apply over $C_{IN}=C_O=2.2\mu\text{F}$, $I_O=100\mu\text{A}$, $V_{IN(MIN)}=2.5\text{V}$ (for adjustable devices), $V_{IN}=V_O + 1\text{V}$ (for fixed voltage devices), $V_{OUT}=V_{FB}$ (for adjustable version only), $C_{BYP}=470\text{pF}$ (for fixed voltage devices), $V_{EN}=2\text{V}$ and $T_A=25^{\circ}\text{C}$. Typical values refer to $T_A=25^{\circ}\text{C}$. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_O		-2		2	%
Line Regulation	ΔV_I	$V_O + 1\text{V} < V_{IN} < 14\text{V}$		0.1		%/V
Load Regulation (Note 1)	ΔV_L	$1\text{mA} < I_O < 100\text{mA}$		1.5		%
Dropout Voltage (Note 2)	$\Delta V_{I(O)}$	$I_O=100\mu\text{A}$		10		mV
		$I_O=50\text{mA}$		50		
		$I_O=100\text{mA}$		120		
Ground Current (Note 3)	I_Q	$V_{EN}=2\text{V}$, $I_O=100\mu\text{A}$		120		μA
Minimum Load Current	I_{Min}			5		mA
Ground Current-SD Activated	$I_{Q(SD)}$	$V_{EN}=0\text{V}$ to 0.8V or Open		5		μA
Current Limit	I_{CL}	$V_O=0\text{V}$	150			mA
Thermal Regulation	ΔV_P	$V_{IN}=10\text{V}$, $I_O=150\text{mA}$, 10ms Pulse		0.05		%/W
Adjust Pin Current	I_{ADJ}	$V_{IN}=2.5\text{V}$, $V_O=V_{ADJ}$		0.1		μA
Enable Pin Input LO Voltage	$V_{EN(L)}$	Regulator OFF			0.8	V
Enable Pin Input HI Voltage	$V_{EN(H)}$	Regulator ON	2.0			V
Enable Pin Input LO Current		$V_{EN(L)}=0\text{V}$ to 0.8V		0.01		μA
Enable Pin Input HI Current		$V_{EN(H)}=2\text{V}$ to V_{IN}		20		μA



Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT} . It is measured when the output voltage drops 1% below its nominal value.

Note 3: Ground current is the regulator quiescent current plus the pass transistor current. The total current from the supply is the sum of the load current plus the ground pin current.

Pin Descriptions

PIN #	PIN SYMBOL	PIN DESCRIPTION
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to ensure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be higher than V_{OUT} by at least the amount of the dropout voltage and some margin in order for the device to regulate properly.
2	Gnd	Ground pin. This pin must be connected to the lowest potential in the system and all other pins must be at higher potential with respect to this pin.
1	En	Enable pin. A low signal or left open on this pin shuts down the output. This pin must be tied HI or to V_{IN} for normal operation.
5	Adj (Adjustable Only)	A resistor divider from this pin to the V_{OUT} pin and ground sets the output voltage. To minimize the error due to the error amplifier, select the values of the resistor dividers to be less than 10K Ω .
5	C_{BYP} (Fixed Only)	A 470 to 1000pF bypass capacitor connected to this pin reduces the output noise.
4	V_{OUT}	The output of the regulator. A capacitor of at least 2.2 μ F with max ESR of 1 Ω must be connected from this pin to ground to ensure stability.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT

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Block Diagram

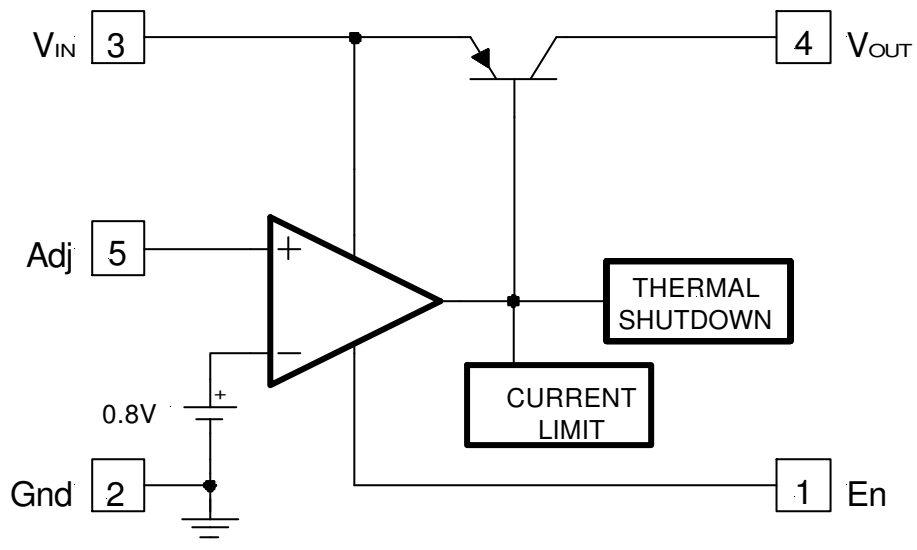


Figure 3 - APU8852Y5-3 Adjustable output block diagram.

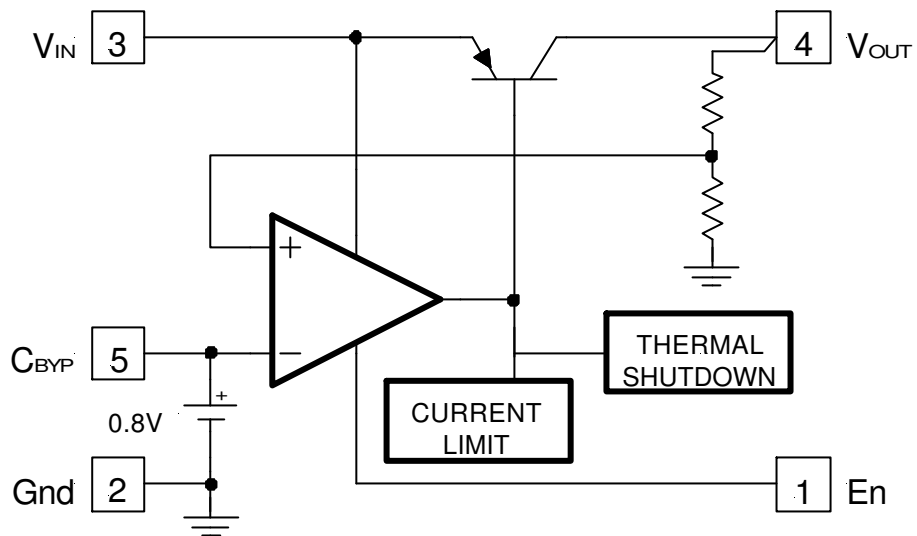
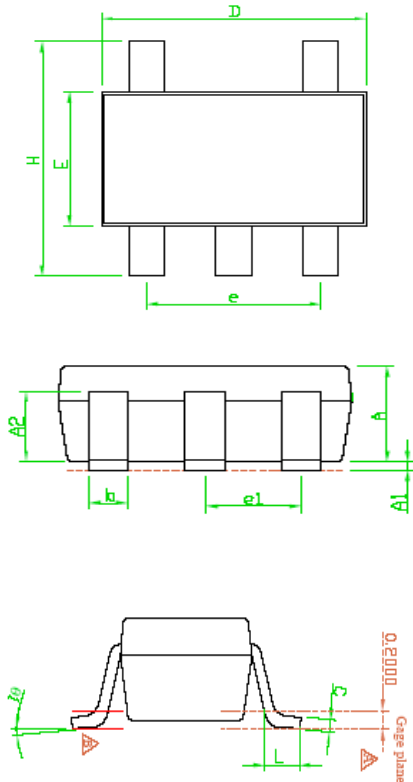


Figure 4 - APU8852Y5-3 Fixed Mode output block diagram.



Package Dimensions: SOT-23-5L



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	---	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.50	1.60	1.80
e	---	1.90(TYP)	---
H	2.60	2.80	3.00
L	0.37	---	---
θ1	1°	5°	9°
e2	---	0.95(TYP)	---

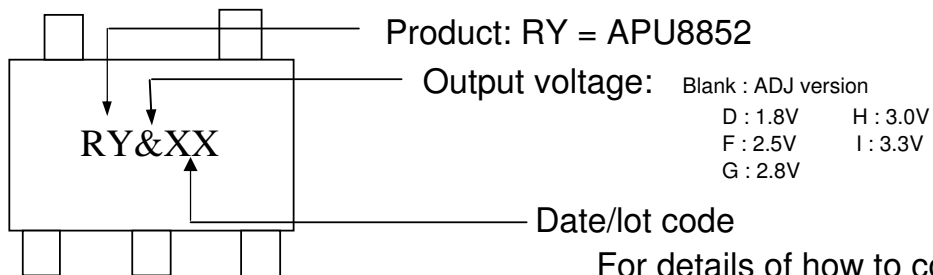
Note 1 : Package body sizes exclude mold flash protrusions or gate burrs.

Note 2 : Tolerance ± 0.1000 mm (4mil) unless otherwise specified.

Note 3 : Coplanarity : 0.1000 mm

Note 4 : Dimension L is measured in gage plane.

Marking Information



For details of how to convert this to standard YYWW date code format, please contact us directly.