Synchronous PWM Controller with Over-Current Protection

Features

- Current Limit using Lower MOSFET Sensing
- Using the 6V internal regulator for charge pump circuit allows single supply operation up to 18V
- Programmable Switching Frequency up to 400KHz
- Soft-Start Function
- 0.8V Precision Reference Voltage Available
- Uncommitted Error Amplifier Available for DDR Voltage Tracking Applications
- Stable with Ceramic Capacitor
- RoHS-compliant, halogen-free packages

Applications

- DDR Memory V_{DDQ}/V_{TT} Applications
- Graphic Card
- Hard Disk Drive
- Netcom on-board DC to DC regulator application
- Output voltage as low as 0.8V
- Low Cost On-Board DC to DC

Description

The APU3039 controller IC is designed to provide a synchronous Buck regulator and is targeted for applications where cost and size are critical. The APU3039 operates with a single input supply up to 18V, and the output voltage can be programmed as low as 0.8V for low voltage applications. Selectable current limit is provided to tailor to external MOSFET's on-resistance for optimum cost and performance. The APU3039 features an uncommitted error amplifier for tracking output voltage and is capable of sourcing or sinking current for applications such as DDR bus termination.

This device features a programmable switching frequency set from 200KHz to 400KHz, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

Typical Application

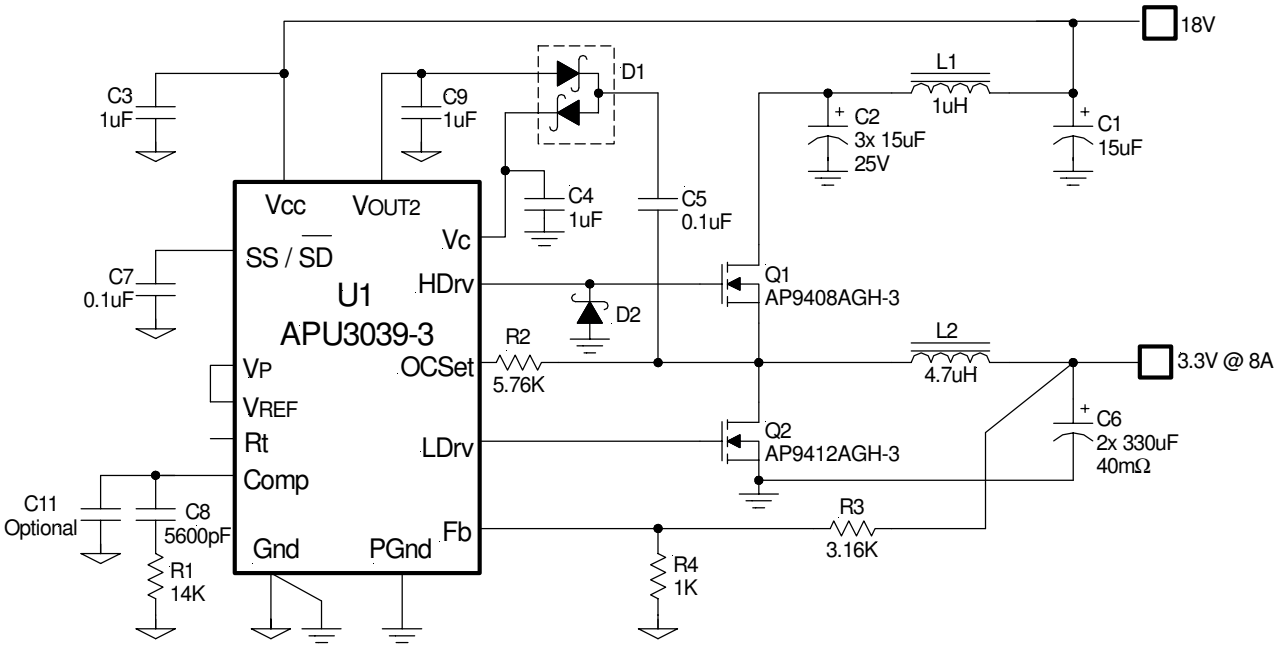


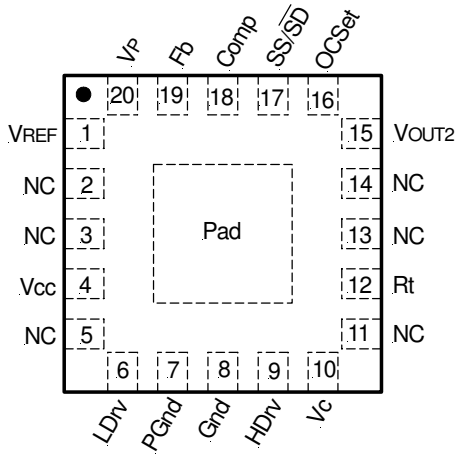
Figure 1 - Typical application of APU3039-3

Ordering Information

APU3039M-HF-3TR	RoHS-compliant, halogen-free 14-Pin plastic SOIC, shipped on tape and reel, 3000pcs/reel.
APU3039VN-HF-3TR	RoHS-compliant, halogen-free 20-Pin 5x5mm VQFN, shipped on tape and reel, 3000pcs/reel.

Pin Configuration

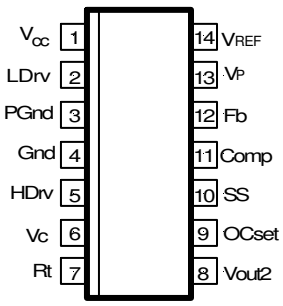
20-Pin VQFN 5x5



$R_{th(ja)}$ = 37℃/W
$R_{th(jc)}$ = 2.3℃/W

*Exposed pad on underside is connected to a typical 1" square copper pad through vias for 4-layer PCB board design.

14-PIN PLASTIC SOIC (M)



$R_{th(ja)}$ = 88℃/W
$R_{th(jc)}$ = 45℃/W

Absolute Maximum Ratings

Vcc Supply Voltage	-0.5V to 25V
Vc Supply Voltage	-0.5V to 25V
Storage Temperature Range	-65℃ to 150℃
Operating Junction Temperature Range	0℃ to 125℃

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Specifications

Unless otherwise specified, specifications apply over Vcc=5V, Vc=12V and T_A=0-70°C. Typical values refer to 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temp.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
Fb Voltage Initial Accuracy	V_{FB}		0.784	0.800	0.816	V
Fb Voltage Line Regulation	L_{REG}	4.75V<Vcc<20V		0.3		%
Reference Voltage						
Ref Voltage Initial Accuracy	V_{REF}		0.784	0.8	0.816	V
Drive Current	I_{REF}	Note 1		2		µA
UVLO						
UVLO Threshold - Vcc	UVLO V_{CC}	Supply Ramping Up		4.4		V
UVLO Hysteresis - Vcc				0.26		V
UVLO Threshold - Vc	UVLO V_C	Supply Ramping Up		3.47		V
UVLO Hysteresis - Vc				0.20		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.3	0.4	0.5	V
Supply Current						
Vcc Dynamic Supply Current	Dyn I_{CC}	Freq=200KHz, C_L=1500pF		7	15	mA
Vc Dynamic Supply Current	Dyn I_C	Freq=200KHz, C_L=1500pF		7	9	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V		5	9	mA
Vc Static Supply Current	I_{CQ}	SS=0V		3	4	mA
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V	-1	+0.08	+1	µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V	30	55	70	µA
Transconductance				700		µmho
VP Voltage Range	V_P	Note 1	0.8		1.5	V
Soft-Start Section						
Charge Current	SS I_B	SS=0V	14	22	35	µA
Oscillator Section	Freq	Rt=Open		200		KHz
Frequency		Rt=Gnd		400		
Ramp Amplitude	V_{RAMP}	Note 1		1.25		V_{PP}
Output Drivers						
Lo Drive Rise Time	$Tr_{(LO)}$	C_{LOAD}=1500pF, V_{CC}=12V		40	100	ns
Hi Drive Rise Time	$Tr_{(HI)}$	C_{LOAD}=1500pF, V_{CC}=12V		40	100	ns
Lo Drive Fall Time	$Tf_{(LO)}$	C_{LOAD}=1500pF		40	100	ns
Hi Drive Fall Time	$Tf_{(HI)}$	C_{LOAD}=1500pF		40	100	ns
Dead Band Time	T_{DB}	HDrv going Hi or Low		100		ns
Max Duty Cycle	D_{MAX}	Fb=0.6V, Freq=200KHz		88		%
Min Duty Cycle	D_{MIN}	Fb=1.0V			0	%
Internal Regulator						
Output Voltage	V_{OUT2}	Vcc=12V	5.7	6	6.3	V
Drive Current	I_{OUT2}		40	65		mA
Current Limit						
OC Threshold Set Current	I_{OCSET}		21	28	35	µA
OC Comp Off-Set Voltage	$V_{OC(OFFSET)}$		-2	1.5	5	mV

Note 1: Guaranteed by design but not tested in production.

Pin Descriptions (Pin numbering for 20pin VQFN)

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	V_{REF}	Reference Voltage. This pin can source current about 2μA.
4	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side FET driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
6	LDrv	Output driver for the synchronous power MOSFET.
7	PGnd	This pin serves as the separate ground for MOSFET's driver and should be connected to system's ground plane.
8	Gnd	This pin serves as analog ground for internal reference and control circuitry. A high frequency capacitor must be connected from Vcc pin to this pin for noise free operation.
9	HDrv	Output driver for the high side power MOSFET. This pin should not go negative (below ground), this may cause problem for the gate drive circuit. It can happen when the inductor current goes negative (Source/Sink), soft-start at no load and for the fast load transient from full load to no load. To prevent negative voltage at gate drive, a low forward voltage drop diode might be connected between this pin and ground.
10	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1μF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
12	Rt	The switching frequency can be Programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. By floating the pin, the switching frequency will be 200KHz and by grounding the pin, the switching frequency will be 400KHz.
15	V_{OUT2}	Output of internal regulator. The output is protected for short circuit. A high frequency capacitor is recommended to be connected from this pin to ground.
16	OCSet	This pin is connected to the Drain of the lower MOSFET via an external resister and it provides the positive sensing for the internal current sensing circuitry. The external resistor programs the current limit threshold depending on the $R_{DS(ON)}$ of the power MOSFET. An external capacitor can be placed in parallel with the programming resistor to provide high frequency noise filtering.
17	SS / $\overline{SD}$	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin down below 0.4V.
18	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
19	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
20	V_P	Non-inverting input of error amplifier.
2,3,5, 11,13,14	NC	No connection.

Block Diagram

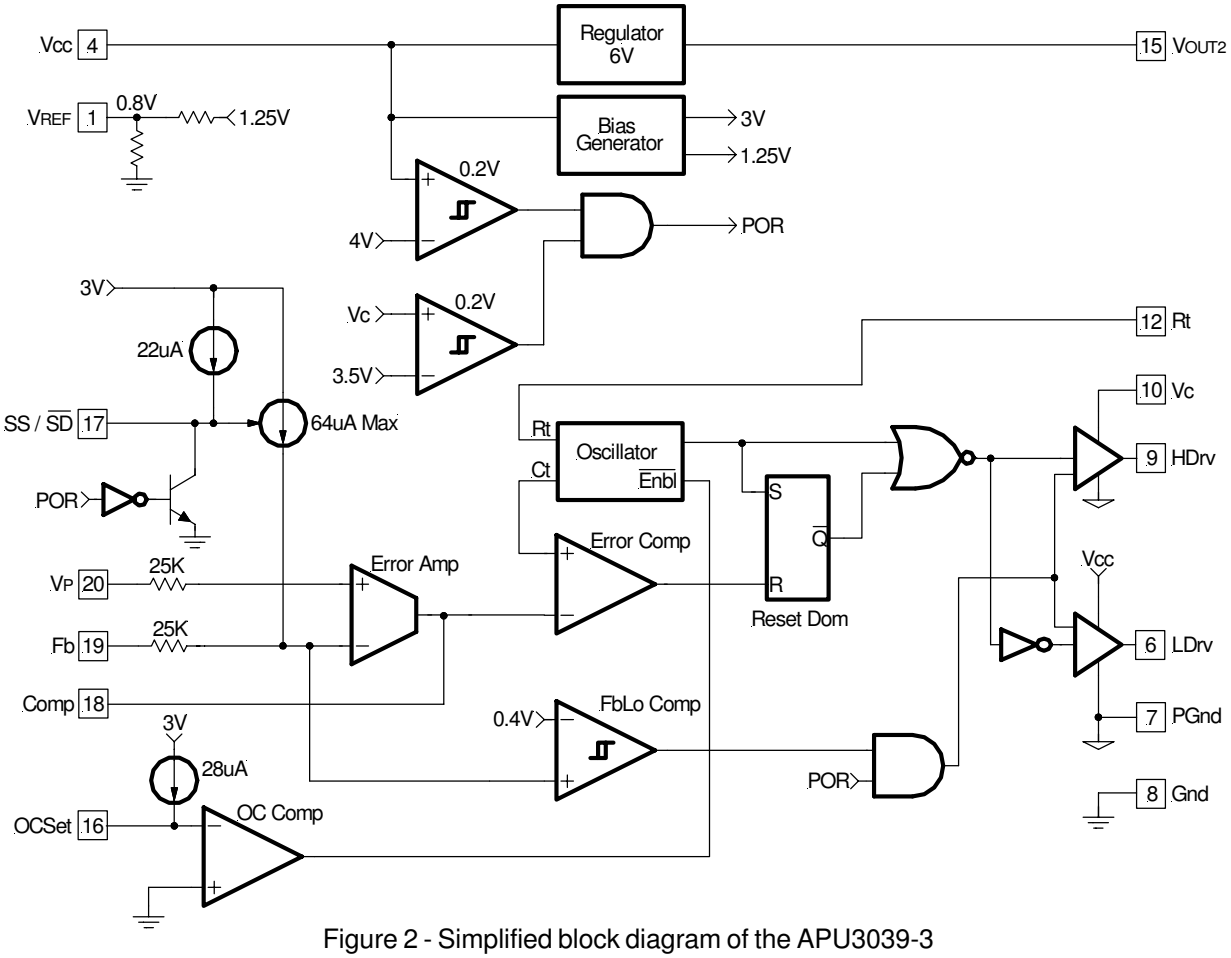


Figure 2 - Simplified block diagram of the APU3039-3

Theory of Operation

Introduction

The APU3039 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an uncommitted error amplifier, an internal oscillator, a PWM comparator, an internal regulator, a comparator for current limit, gate drivers, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the voltage on non-inverting input of error amplifier(V_P). This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor. The oscillation frequency is programmable between 200KHz to 400KHz by using an external resistor. Figure 14 shows switching frequency vs. external resistor (Rt).

Soft-Start

The APU3039 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.4V and 4.4V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter and disables the short circuit protection. During the power up, the output starts at zero and voltage at Fb is below 0.4V. The feedback UVLO is disabled during this time by injecting a current (64μA) into the Fb. This generates a voltage about 1.6V (64μAx25kΩ) across the negative input of E/A and positive input of the feedback UVLO comparator (see Figure 3).

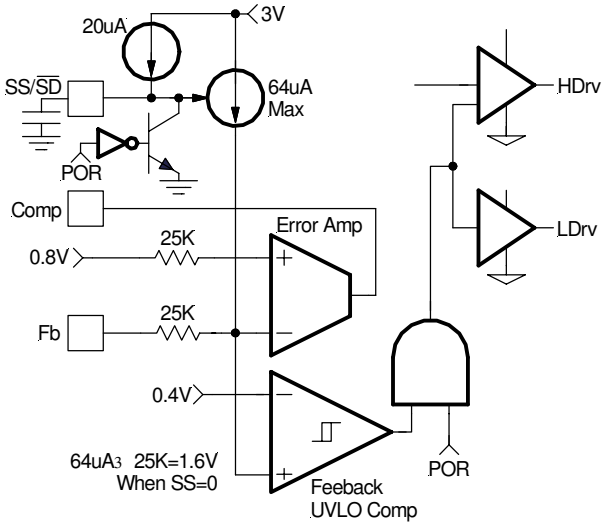


Figure 3 - Soft-start circuit for APU3039.

The magnitude of this current is inversely proportional to the voltage at soft-start pin.

The 20μA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at the positive pin of feedback UVLO comparator and the voltage negative input of E/A.

When the soft-start capacitor is around 1V, the current flowing into the Fb pin is approximately 32μA. The voltage at the positive input of the E/A is approximately:

$$32\mu A \times 25k\Omega = 0.8V$$

The E/A will start to operate and the output voltage starts to increase. As the soft-start capacitor voltage continues to go up, the current flowing into the Fb pin will keep decreasing. Because the voltage at pin of E/A is regulated to reference voltage 0.8V, the voltage at the Fb is:

$$V_{FB} = 0.8 - (25k\Omega \times (\text{Injected Current}))$$

Theory of Operation (cont.)

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 2V and the output voltage goes into steady state.

As shown in Figure 4, the positive pin of feedback UVLO comparator is always higher than 0.4V, therefore, feedback UVLO is not functional during soft-start.

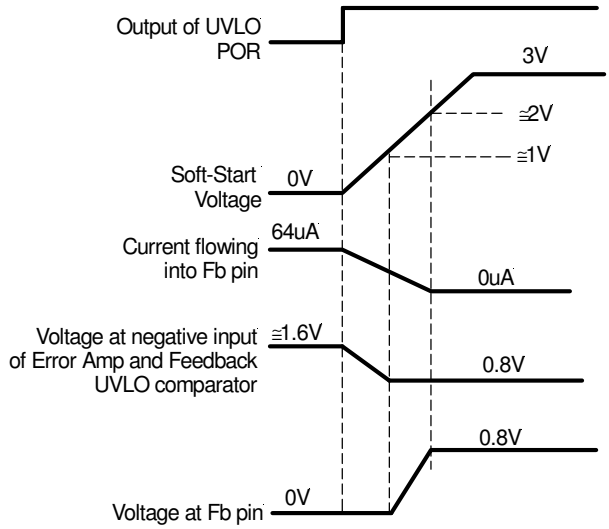


Figure 4 - Theoretical operational waveforms during soft-start.

the output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$20\mu A \times T_{START}/C_{SS} = 2V\text{-}1V$$

For a given start up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 20\mu A \times T_{START}/1V$$

Internal Regulator

The regulator powers directly from Vcc and generates a regulated voltage (6V @ 40mA). The output is protected for short circuit. This voltage can be used for charge pump circuitry as shown in Figure 1.

Supply Voltage Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc or Vcc fall below 3.4V and 4.4V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

Shutdown

The converter can be shutdown by pulling the soft-start pin below 0.4V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Over-Current Protection

Over-current protection is achieved with a cycle by cycle scheme and it is performed by sensing current through the $R_{DS(ON)}$ of low side MOSFET. As shown in Figure 5, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) and sets the current limit set point. The internal current source develops a voltage across R_{SET}. When the low side switch is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times i_L \qquad ---(1)$$

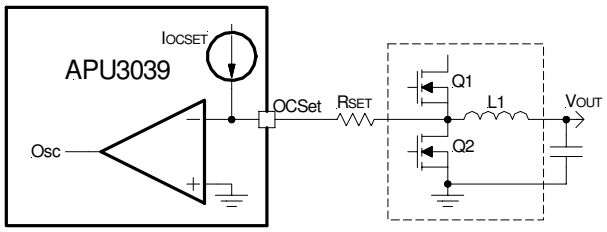


Figure 5 - Diagram of the over current sensing.

When voltage V_{OCSET} is below zero, the current sensing comparator flips and disables the oscillator. The high side MOSFET is turned off and the low side MOSFET is turned on until the inductor current reduces to below current set value. The critical inductor current can be calculated by setting:

$$V_{OCSET} = I_{OCSET} \times R_{SET} - R_{DS(ON)} \times I_L = 0$$

$$I_{SET} = I_{L(CRITICAL)} = \frac{R_{SET} \times I_{OCSET}}{R_{DS(ON)}} \qquad ---(2)$$

If the over-current condition is temporary and goes away quickly, the APU3039 will resume its normal operation.

If output is shorted or over-current condition persists, the output voltage will keep going down until it is below 0.4V. Then the output under-voltage lock out comparator goes high and turns off both MOSFETs. The operation waveforms are shown in Figure 6.