



### 3A Ultra-Low Dropout Regulator with Enable

#### Features

- Ultra-low Dropout Voltage of 0.21V (typ.) with an Output Current of 2A and Output Voltage of 1.2V
- Compatible with Low ESR Output Capacitors (Multi-layer Chip Capacitors (MLCC))
- Enable Pull-low for APE8903Cxx-A  
Enable Pull-high for APE8903Cxx-B
- Fast Transient Response
- Adjustable Output Voltage using External Resistors
- Power-on-reset Monitoring on both VCNTL and VIN Pins
- Internal Soft-start
- Current-limit and Thermal Shutdown Protection
- Power-OK Output with a Delay Time
- SO-8 with Exposed Pad, or DFN 3x3-10L Package.
- RoHS-compliant Halogen-free Packages.

#### Description

The APE8903C series is a 3A ultra-low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8903C series integrates many functions. A power-on-reset (POR) circuit monitors both supply voltages to prevent incorrect operation. Thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with a time delay which is set internally, and can be used for power sequencing control. The APE8903C series can be enabled by other power systems. Pulling and holding the EN pin below 0.4V shuts off the output.

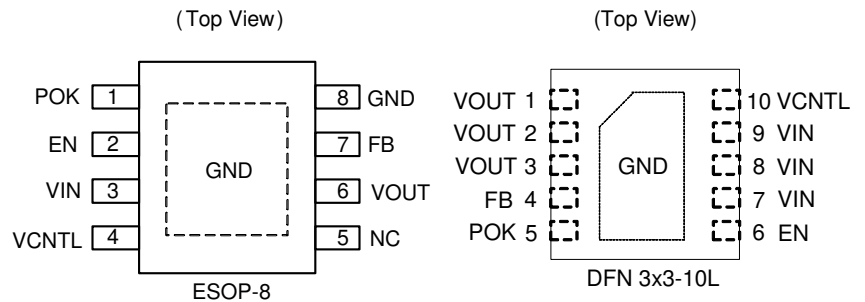
The APE8903C series is available in a DFN 3x3-10L or an ESOP-8 package which features the small size of an SO-8 with an exposed pad to reduce the junction-to-case resistance, making it suitable for 2-3W applications .

#### Ordering Information

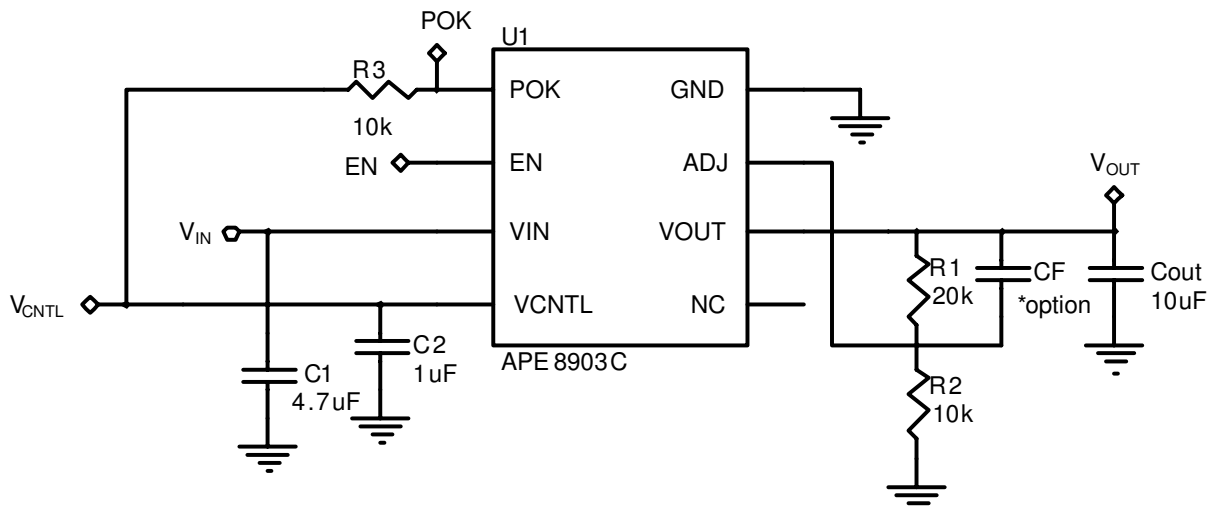
##### APE8903Cxx-x-HF-3TR



#### Pin Configuration



#### Typical Application Circuit





**Absolute Maximum Ratings (Note 1)**

CNTL Supply Voltage ( $V_{CNTL}$ )	-----	-0.3V To 6.5V
Input Supply Voltage ( $V_{IN}$ )	-----	-0.3V To 6.5V
EN and FB Pin Voltage ( $V_{EN}/V_{FB}$ )	-----	-0.3V To $V_{CNTL}+0.3V$
Power Good Voltage ( $V_{POK}$ )	-----	-0.3V To 6.5V
Power Dissipation ( $P_D$ )	-----	2.5W (Note 2)
Storage Temperature Range ( $T_{ST}$ )	-----	-65°C To 150°C
Junction Temperature Range ( $T_J$ )	-----	-40°C To 150°C
Thermal Resistance, Junction to Ambient ( $R_{th(ja)}$ ) <sup>Note</sup>		
	ESO-8 ---	40°C/W
	DFN 3x3-10L ---	62.5°C/W
Thermal Resistance, Junction to Case ( $R_{th(jc)}$ )		
	ESO-8 ---	15°C/W
	DFN 3x3-10L ---	17°C/W

Note.  $R_{th(ja)}$  is measured with a PCB copper area of approximately 1.5 in<sup>2</sup> (Multi-layer) connected to the exposed package pad

**Recommended Operating Conditions**

Operating Junction Temperature Range ( $T_{OJ}$ )	-----	-40°C To 125°C
Operating Ambient Temperature Range ( $T_{OA}$ )	-----	-40°C To 85°C
VCNTL Supply Voltage ( $V_{CNTL}$ )	-----	3V To 6V
Input Supply Voltage ( $V_{IN}$ )	-----	1.1V To 5.5V
Output Voltage ( $V_{OUT}$ ) at $V_{CNTL}=5V$	-----	0.8V To 2.8V
Output Current ( $I_{OUT}$ )	-----	0A to 3A

- Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Specifications.
- Note2:** The maximum power dissipation is a function of the maximum junction temperature,  $T_{jmax}$ ; total thermal resistance,  $R_{th(ja)}$  and ambient temperature  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $(T_{jmax} - T_A) / R_{th(ja)}$ . If this dissipation is exceeded, the die temperature will rise above 150°C and the IC will go into thermal shutdown.
- Note3:** Low duty pulse techniques are used during test to maintain a junction temperature as close to ambient as possible.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.  
 USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.  
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**Electrical Specifications**

$V_{CNTL}=5V$ ,  $V_{IN}=1.8V$ ,  $V_{OUT}=1.2V$ ,  $T_A=25^{\circ}C$  unless otherwise specified

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS	
$V_{CNTL}$ Operation Voltage	$V_{CNTL}$		2.8	-	5.5	V	
$V_{IN}$ POR Threshold	$V_{IN}$		0.8	0.9	1	V	
$V_{IN}$ POR Hysteresis	$V_{IN(hys)}$		-	0.5	-	V	
$V_{CNTL}$ Nominal Supply Current	$I_{CNTL}$	EN= $V_{CNTL}$	-	1.3	-	mA	
$V_{CNTL}$ Shutdown Current	$I_{SD}$	EN=0V	APE8903Cxx-A	-	-	1	uA
			APE8903Cxx-B	-	10	30	
Feedback Voltage	$V_{FB}$	$V_{CNTL}=3 \sim 6V$ , $I_{OUT}=10mA$ , $V_{IN}=V_{OUT}+0.5\sim 5.5V$	0.784	0.8	0.816	V	
Load Regulation		$I_{OUT}=0A \sim 2A$	-	0.5	1	%	
On Resistance	$R_{DS(ON)}$	$I_{OUT}=100mA$ , $V_{CNTL}=V_{EN}=5.0V$ , $V_{OUT}=1.2V$	-	105	150	mΩ	
Dropout Voltage	$V_{DROP}$	$I_{OUT} = 2A$ , $V_{CNTL}=5V$ , $V_{OUT} = 1.2V$	-	0.21	0.3	V	
$V_{OUT}$ Pull Low Resistance		EN=0V	-	40	-	Ω	
Soft Start Time	$T_{SS}$		-	0.2	-	ms	
EN Pin Logic High Threshold Voltage	$V_{ENH}$	Enable	1.2	-	-	V	
	$V_{ENL}$	Disable	-	-	0.6		
EN Pin Pull-Up Current	$I_{EN}$	EN=5V, APE8903Cxx-A	-	10	20	uA	
		EN=GND, APE8903Cxx-B	-	10	20		
Current Limit	$I_{LIM}$	$V_{CNTL}=5V$ , $V_{IN}=V_{OUT}+1V$	3.1	-	-	A	
Ripple Rejection	$V_{IN}$	PSRR F=120Hz, $I_{OUT}=100mA$	-	65	-	dB	
	$V_{CNTL}$		-	65	-		
POK Threshold Voltage for Power OK	$V_{POK}$	VFB Rising	92%	94%	96%	$V_{FB}$	
POK Threshold Voltage for Power Not OK	$V_{PNOK}$	VFB Falling	83%	88%	91%	$V_{FB}$	
POK Low Voltage		POK sinks 5mA	-	-	0.1	V	
POK Delay Time	$T_{DELAY}$		0.8	2	10	ms	
Thermal Shutdown Threshold <sup>(Note1)</sup>	$T_{SD}$		-	160	-	°C	
Thermal Shutdown Hysteresis <sup>(Note1)</sup>			-	40	-	°C	

Note1: Guarantee by design, not production tested.





## Pin Descriptions

### FB

Receives the feedback voltage from the external resistor divider of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left( 1 + \frac{R1}{R2} \right) \quad (V)$$

where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected in parallel with R1 to improve load transient response. The recommended range of values for resistor R2 is 1kΩ to 4.7kΩ for AL output capacitors and 30kΩ to 100kΩ for MLCC output capacitors.

### VIN

Main supply input pins for power conversion. The voltage at this pin is monitored for Power-On Reset purposes.

### VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purposes.

### POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of the output voltage by sensing the FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

### EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. For APE8903Cxx-B, this pin is pulled up internally to VCNTL voltage, enabling the regulator. For APE8903Cxx-A, this pin is pulled down internally to GND voltage, shutting down the regulator. The pull-high or pull-low current is 10uA (typ.)

### VOUT

Output of the regulator. Please connect Pin 6 using wide tracks. It is necessary to connect an output capacitor to this pin for closed-loop compensation and to improve the transient response.

## Function Description

### Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent incorrect logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless of the output voltage when the VCNTL voltage falls below its falling POR threshold.

### Internal Soft-Start

An internal soft-start function controls slew rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 0.2ms.

### Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain, providing very fast transient response and improved load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

### Current-Limit

The APE8903C monitors the current via the output N-MOSFET and limits the maximum current to prevent the load and the regulator from damage during overload or short circuit conditions.



## **Function Description (cont.)**

### **Thermal Shutdown**

A thermal shutdown circuit limits the junction temperature of the APE8903C. When the junction temperature exceeds +160 °C, a thermal sensor turns off the output NMOSFET, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40 °C, resulting in a pulsed output during continuous thermal overload conditions.

## **Application Information**

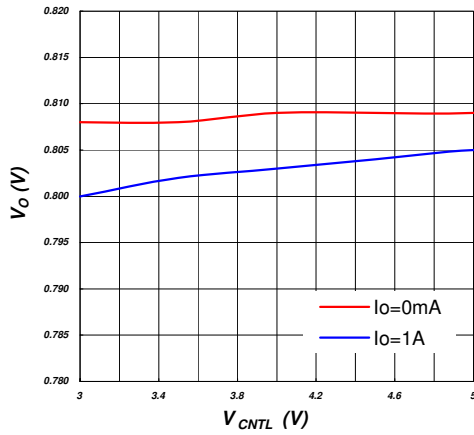
### **Capacitor Selection**

Normally, use a MLCC capacitor on the input and output of the APE8903C. Larger input capacitor values provide better supply-noise rejection and transient response. A higher value output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. The X5R and X7R type of MLCC are recommended. When using aluminum electrolytic capacitors, 100uF for input capacitor and 220uF for output capacitor ( $30\text{m}\Omega < \text{ESR} < 200\text{m}\Omega$ ) are recommended. Output capacitors of larger value can reduce noise and improve load transient response, stability, and PSRR.

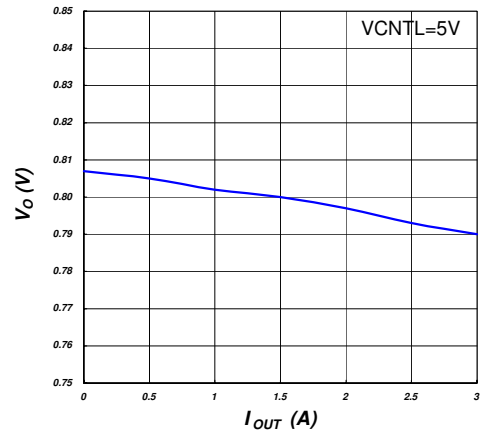


### Typical Performance Characteristics

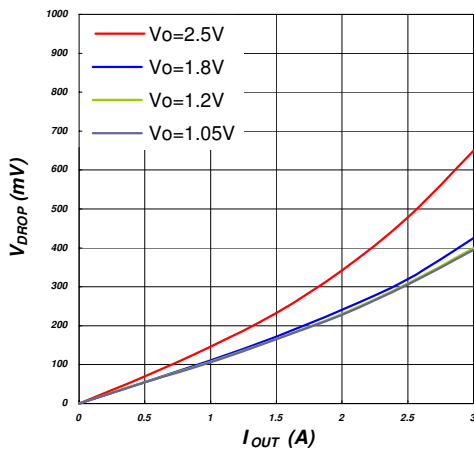
( $V_{CC}=3.3V$ ,  $T_A=25^\circ$  unless otherwise noted.)



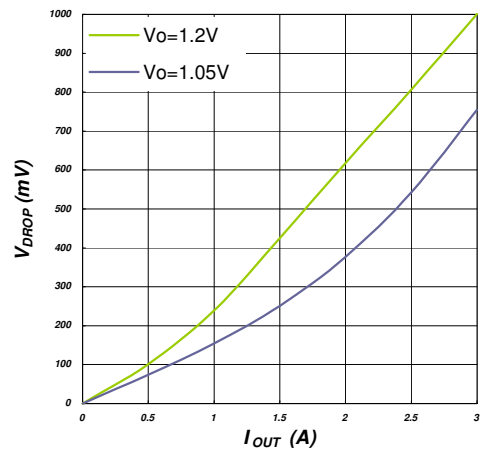
Line Regulation



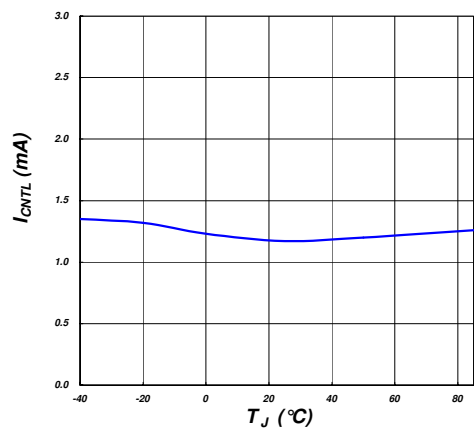
Load Regulation



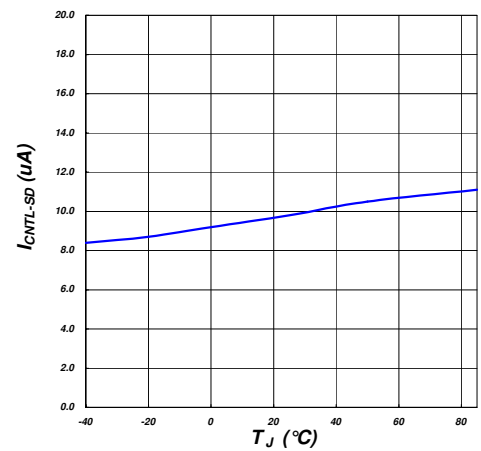
Dropout Voltage at  $V_{CNTL}=5V$



Dropout Voltage at  $V_{CNTL}=3.3V$



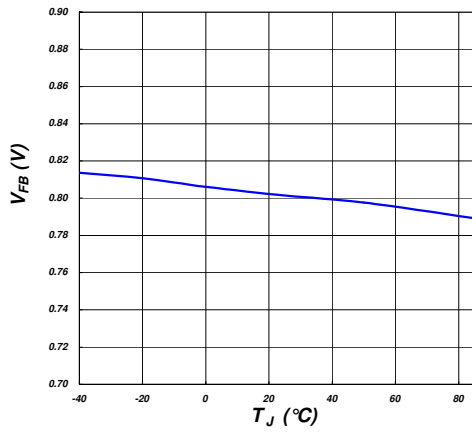
$I_{CNTL}$  vs.  $T_J$



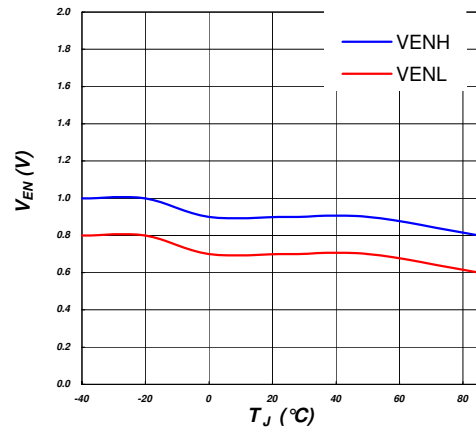
$I_{CNTL-SD}$  (APE8903Cxx-B) vs.  $T_J$



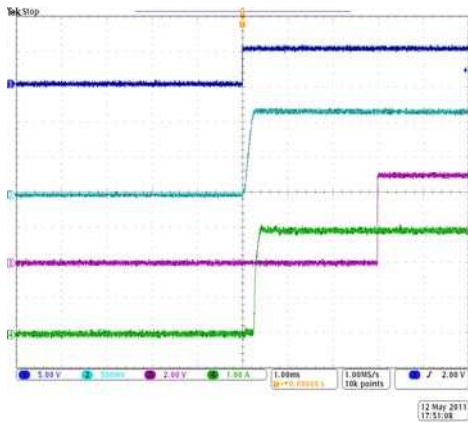
Typical Performance Characteristics (continued)



V<sub>FB</sub> vs. T<sub>J</sub>

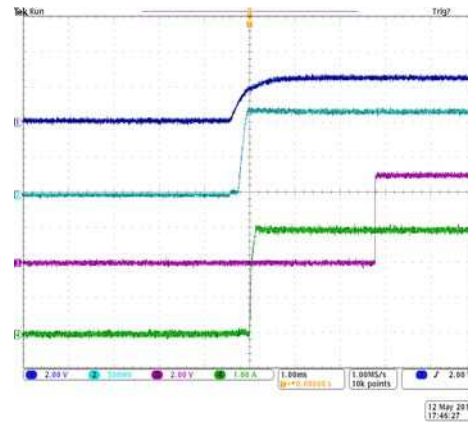


V<sub>EN</sub> vs. T<sub>J</sub>



EN on with POK Delay

V<sub>EN</sub>  
V<sub>OUT</sub>  
POK  
I<sub>OUT</sub>=3A

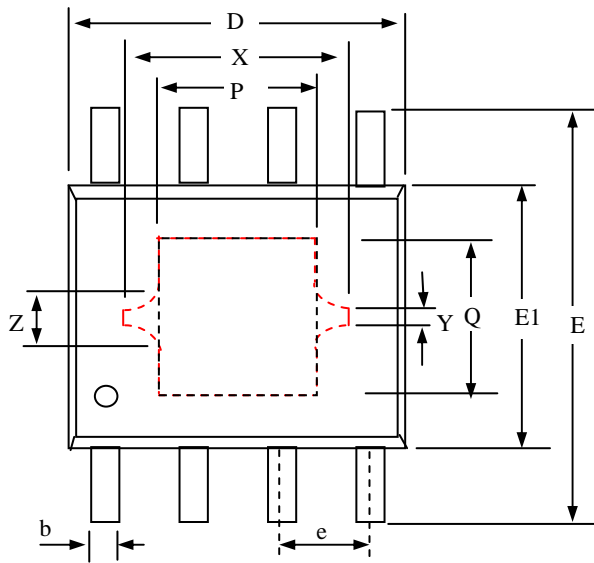


V<sub>IN</sub> Power -ON

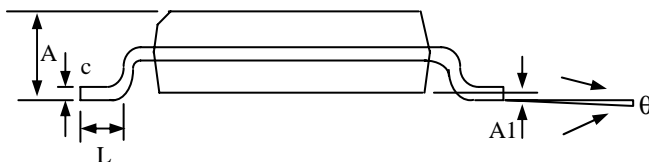
V<sub>IN</sub>  
V<sub>OUT</sub>  
POK  
I<sub>OUT</sub>=3A



**Package Dimensions: ESOP-8**

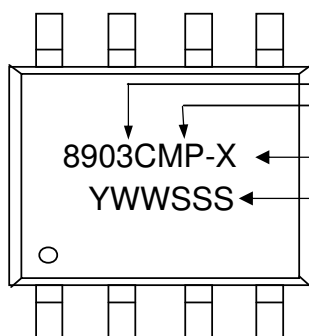


SYMBOLS	Millimeters		
	MIN	NOM	MAX
E	5.70	6.00	6.30
D	4.70	4.95	5.20
E1	3.70	3.95	4.20
$\theta$	0°	4°	8°
L	0.30	0.80	1.30
c	0.10	0.20	0.30
A1	0.00	0.08	0.15
b	0.31	0.41	0.51
A	1.30	1.55	1.80
e	1.27 TYP.		
P	1.65	2.13	2.60
Q	1.65	2.13	2.60
X	3.25 REF.		
Y	0.20 REF.		
Z	0.47 REF.		



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

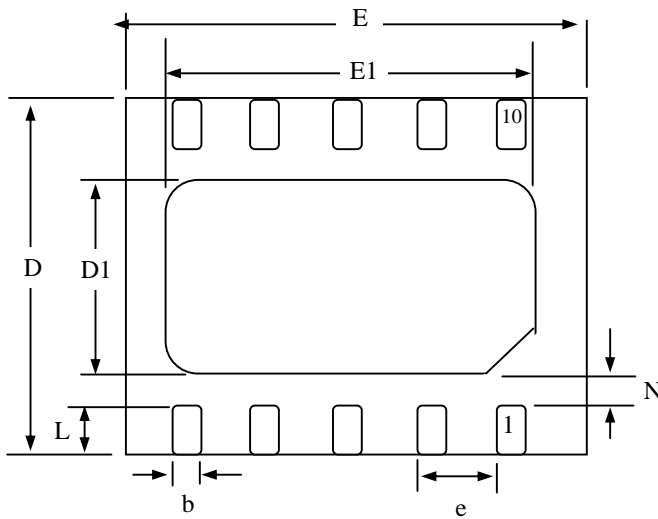
**Marking Information**



Product : APE8903C  
 Package code : MP = RoHS-compliant halogen-free ESOP-8  
 Enable function option (A or B)  
 Date/lot code (YWWSSS)  
 Y: Last digit of the year  
 W: Work week  
 SSS: Lot code sequence

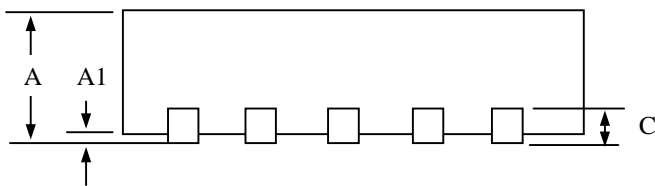


**Package Dimensions: DFN3x3-10L**



**BOTTOM VIEW**

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.70	0.85	1.00
A1	0.00	0.03	0.05
b	0.18	0.24	0.30
C	0.195	0.203	0.211
D	2.90	3.00	3.10
D1	1.55	1.62	1.69
E	2.90	3.00	3.10
E1	2.25	2.45	2.65
e	0.5 (ref.)		
L	0.35	0.43	0.50
N	0.25	0.30	0.35



1. All dimensions are in millimeters
2. Dimensions do not include mold protrusions.

**Marking Information**

