3A Ultra-Low Dropout Regulator with Enable

Features

- **Ultra-low Dropout Voltage of 0.23V (typ.) at 2A Output Current and 1.2V Output Voltage**
- **Compatible with Low ESR Output Capacitors (Multi-layer Chip Capacitors (MLCC))**
- **Enable Pull-low for APE8903BMP-A**
  Enable Pull-high for APE8903BMP-B
- **Fast Transient Response**
- **Adjustable Output Voltage using External Resistors**
- **Power-on-reset Monitoring on both VCNTL and VIN Pins**
- **Internal Soft-start**
- **Under-voltage Protection**
- **Current-limit and Thermal Shutdown Protection**
- **Power-OK Output with a Delay Time**
- **SO-8 with Exposed Pad**
- **RoHS-compliant Halogen-free Package.**

Description

The APE8903B series is a 3A ultra-low dropout linear regulator. This product is specifically designed to provide well supply voltage for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8903B series integrates many functions. A power-on-reset (POR) circuit monitors both supply voltages to prevent incorrect operation. Thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with a time delay which is set internally, and can be used for power sequencing control. The APE8903B series can be enabled by other power systems. Pulling and holding the EN pin below 0.4V shuts off the output.

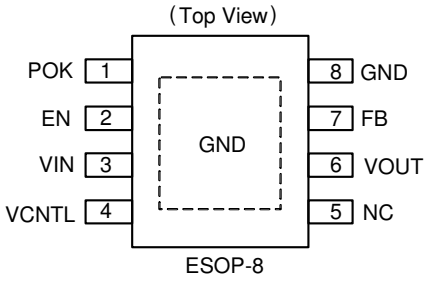
The APE8903B series is available in the ESOP-8 package which features the small size of an SO-8 and has an exposed pad to reduce the junction-to-case resistance, making it suitable for 2-3W applications .

Ordering Information

APE8903BMP-X-HF-3TR

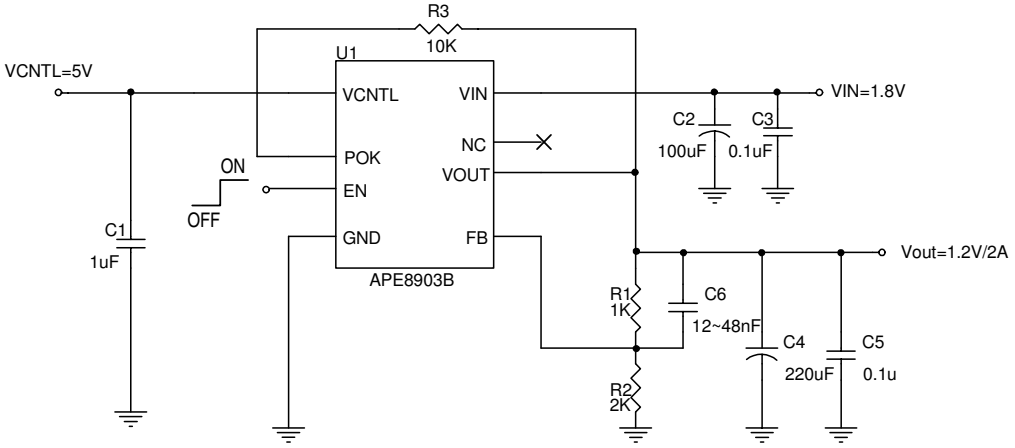
EN Function
A : Pull Low
B : Pull High

Pin Configuration



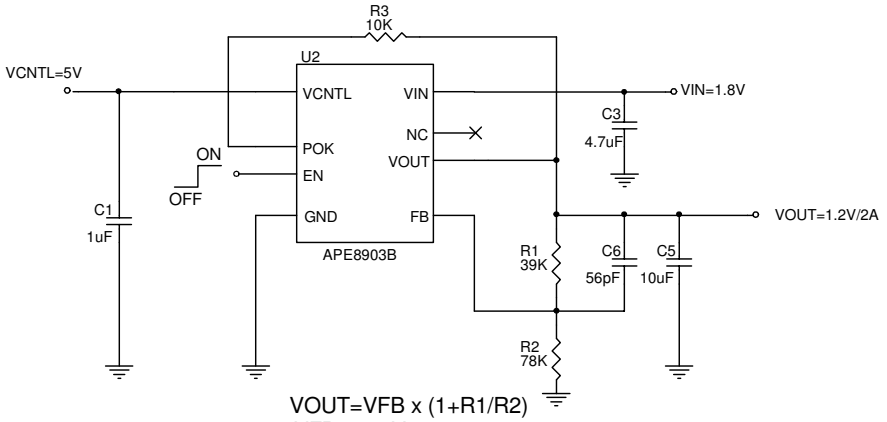
Typical Application Circuit

Using an Output Capacitor with ESR>20mΩ



Typical Application Circuit

Using an MLCC as the Output Capacitor



Absolute Maximum Ratings (Note 1)

CNTL Supply Voltage (V_{CNTL})	-0.3V To 6.5V
Input Supply Voltage (V_{IN})	-0.3V To 6.5V
EN and FB Pin Voltage (V_{EN}/V_{FB})	-0.3V To VCNTL+0.3V
Power Good Voltage (V_{POK})	-0.3V To 6.5V
Power Dissipation (P_D)	2.5W (Note 2)
Storage Temperature Range (T_{ST})	-65℃ To 150℃
Junction Temperature Range (T_J)	-40℃ To 150℃
Thermal Resistance, Junction to Ambient (Rth_{ja})^{Note}	40℃/W
Thermal Resistance, Junction to Case (Rth_{jc})	15℃/W

Note. Rth_{ja} is measured with a PCB copper area of approximately 1.5 in^2 (Multi-layer) connected to the exposed package pad

Recommended Operating Conditions

Operating Junction Temperature Range (T_{OJ})	-40℃ To 125℃
Operating Ambient Temperature Range (T_{OA})	-40℃ To 85℃
VCNTL Supply Voltage (V_{CNTL})	3V To 6V
Input Supply Voltage (V_{IN})	1.1V To 5.5V
Output Voltage (V_{OUT}) at V_{CNTL}= 5V	0.8V To 2.8V
Output Current (I_{OUT})	0A to 3A

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be guaranteed. For guaranteed specifications and test conditions see the Electrical Specifications.

Note2: The maximum power dissipation is a function of the maximum junction temperature, T_{Jmax} ; total thermal resistance, $R_{th(ja)}$ and ambient temperature T_A . The maximum allowable power dissipation at any ambient temperature is $(T_{jmax} - T_A) / R_{th(ja)}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the IC will go into thermal shutdown.

Note3: Low duty pulse techniques are used during test to maintain a junction temperature as close to ambient as possible.

Electrical Specifications

V_{CNTL}= 5V, V_{IN}=1.8V, V_{OUT}=1.2V, T_A=25°C unless otherwise specified

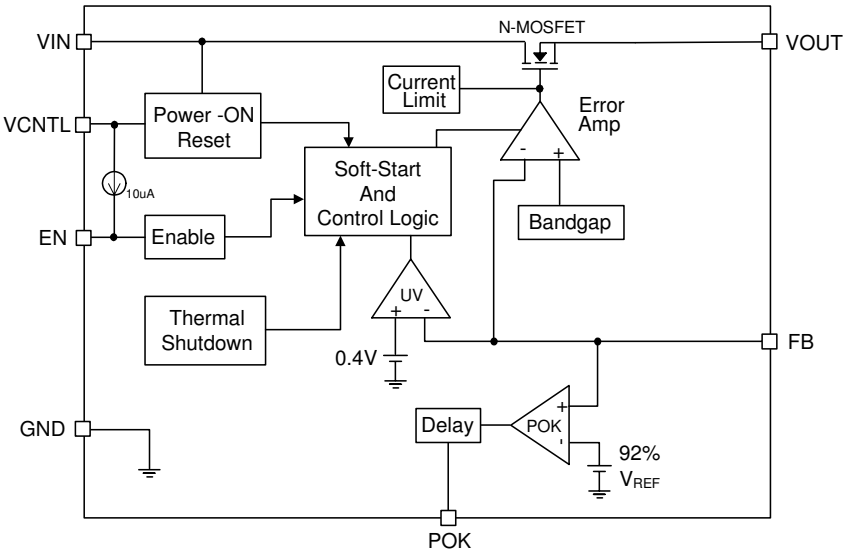
Parameter	SYM	TEST CONDITION		MIN	TYP	MAX	UNITS
V_{CNTL} POR Threshold	V_{CNTL}			2.5	2.7	2.9	V
V_{CNTL} POR Hysteresis	$V_{CNTL(hys)}$			-	0.4	-	V
V_{IN} POR Threshold	V_{IN}			0.8	0.9	1	V
V_{IN} POR Hysteresis	$V_{IN(hys)}$			-	0.5	-	V
V_{CNTL} Nominal Supply Current	I_{CNTL}	EN= V_{CNTL}		0.4	1	1.5	mA
VCNTL Shutdown Current	I_{SD}	EN=0V	APE8903BMP-A	-	-	1	uA
			APE8903BMP-B	-	10	30	
Feedback Voltage	V_{FB}	V_{CNTL}=3 ~ 6V, I_{OUT}=10mA, V_{IN}=V_{OUT}+0.5~5.5V		0.784	0.8	0.816	V
Load Regulation		I_{OUT}=0A ~ 2A		-	0.2	1	%
On Resistance	$R_{DS(ON)}$	I_{OUT}=100mA, V_{CNTL}=V_{EN}=5.0V, V_{OUT}=1.2V		-	115	150	mΩ
Dropout Voltage	V_{DROP}	I_{OUT} = 2A, V_{CNTL}=5V, V_{OUT} = 1.2V		-	0.23	0.3	V
V_{OUT} Pull Low Resistance		EN=0V		-	90	-	Ω
Soft Start Time	T_{SS}			-	2	-	ms
EN Pin Logic High Threshold Voltage	V_{ENH}	Enable		1.2	-	-	V
	V_{ENL}	Disable		-	-	0.6	
EN Hysteresis				-	40	-	mV
EN Pin Pull-Up Current	I_{EN}	EN=5V, APE8903BMP-A		-	10	20	uA
		EN=GND, APE8903BMP-B		-	10	20	
Current Limit	I_{LIM}	V_{CNTL}=5V, V_{IN}=V_{OUT}+1V		3.1	-	-	A
Ripple Rejection V_{IN}	PSRR	F=120Hz, I_{OUT}=100mA		-	65	-	dB
Ripple Rejection V_{CNTL}				-	65	-	
Inrush current		V_{CNTL}=5V, C_{OUT}=10uF, EN startup, I_{OUT}=2A		-	0.5	-	A
Under-Voltage Threshold		VFB Falling		-	0.4	-	V
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising		89%	92%	95%	VFB
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling		78%	81%	84%	VFB
POK Low Voltage		POK sinks 5mA		-	0.25	0.4	V
POK Delay Time	T_{DELAY}			0.8	2	10	ms
Thermal Shutdown Temp	TSD			-	160	-	°C
Thermal Shutdown Hysteresis				-	40	-	°C

Pin Descriptions

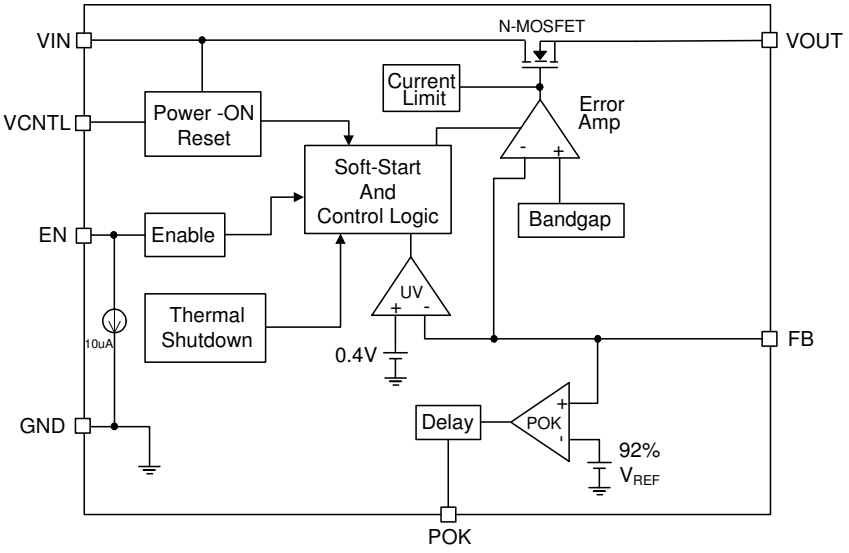
PIN SYMBOL	PIN DESCRIPTION
POK	Power OK Output Pin
EN	Internal Pull-high (APE8903BMP-B) or Pull-low (APE8903BMP-A) EN=High or Floating -> Enable EN=Low -> Shutdown Mode
VIN	Input Voltage.
VCNTL	CNTL Pin Input Voltage
NC	No Connect
VOUT	Output Voltage
FB	Feedback Pin
GND	GND Pin

Block Diagram

APE8903BMP-A



APE8903BMP-B



Pin Descriptions

FB

Receives the feedback voltage from the external resistor divider of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad (V)$$

where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected in parallel with R1 to improve load transient response. The recommended range of values for resistor R2 is 1kΩ to 4.7kΩ for AL output capacitors and 30kΩ to 100kΩ for MLCC output capacitors.

VIN

Main supply input pins for power conversion. The voltage at this pin is monitored for Power-On Reset purposes.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purposes.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of the output voltage by sensing the FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

EN

Enable control pin. Pulling and holding this pin below 0.4V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. For APE8903BMP-B, this pin is pulled up internally to VCNTL voltage, enabling the regulator. For APE8903BMP-A, this pin is pulled down internally to GND voltage, shutting down the regulator. The pull-high or pull-low current is 10uA (typ.)

VOUT

Output of the regulator. Please connect Pin 6 using wide tracks. It is necessary to connect an output capacitor to this pin for closed-loop compensation and to improve the transient response.

Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent incorrect logic controls. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless of the output voltage when the VCNTL voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls slew rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2ms.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain, providing very fast transient response and improved load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

Current-Limit

The APE8903B monitors the current via the output NMOS and limits the maximum current to prevent the load and the regulator from damage during overload or short circuit conditions.

Function Description (cont.)

Under-Voltage Protection (UVP)

The APE8903B monitors the voltage on FB pin after soft-start process is finished. Therefore the UVP is disabled during soft-start. When the voltage on FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APE8903B starts a new soft-start to regulate output.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APE8903B. When the junction temperature exceeds +160℃, a thermal sensor turns off the output NMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40℃, resulting in a pulsed output during continuous thermal overload conditions.

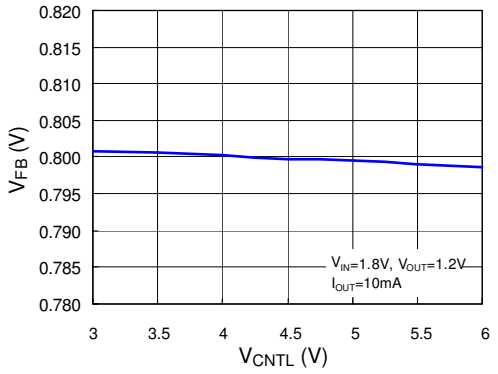
Application Information

Capacitor Selection

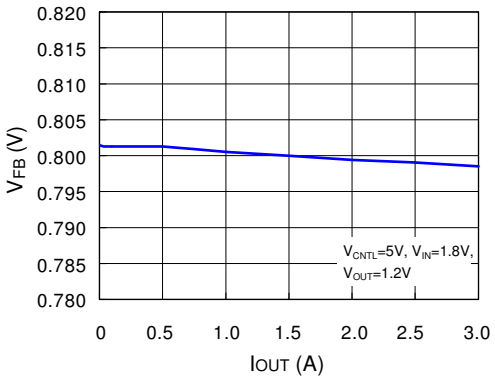
Normally, use a MLCC capacitor on the input and output of the APE8903B. Larger input capacitor values provide better supply-noise rejection and transient response. A higher value output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. The X5R and X7R type of MLCC are recommended. When using aluminum electrolytic capacitors, 100uF for input capacitor and 220uF for output capacitor ($30m\Omega < ESR < 200m\Omega$) are recommended. Output capacitors of larger value can reduce noise and improve load transient response, stability, and PSRR.

Typical Performance Characteristics

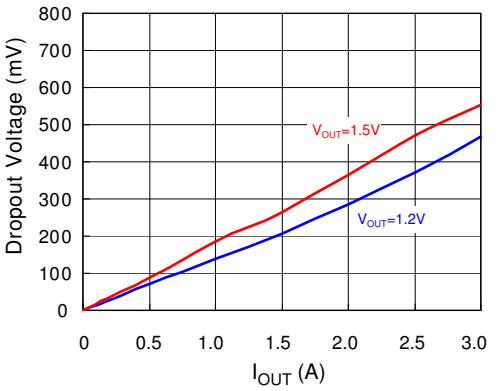
(V_{CC}= 3.3V, T_A=25° unless otherwise noted.)



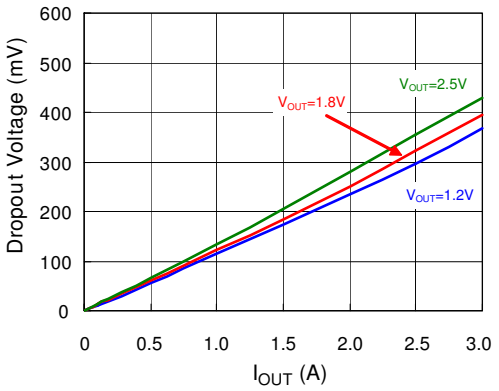
Line Regulation



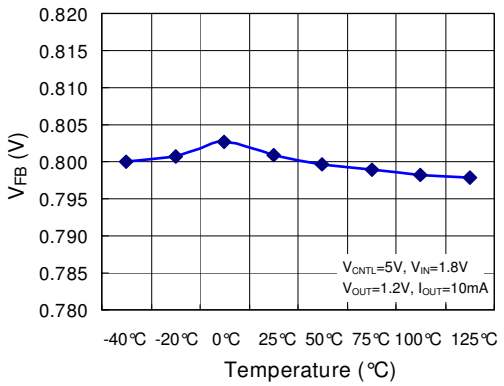
Load Regulation



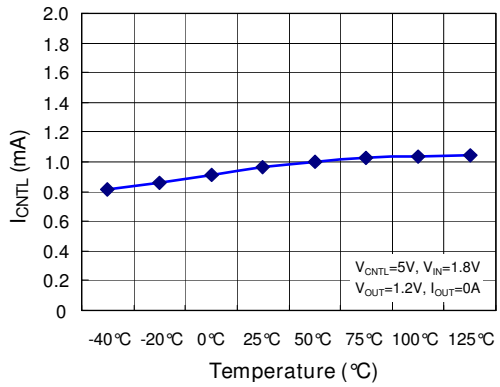
Dropout Voltage (V_{CNTL}=3.3V)



Dropout Voltage (V_{CNTL}=5V)

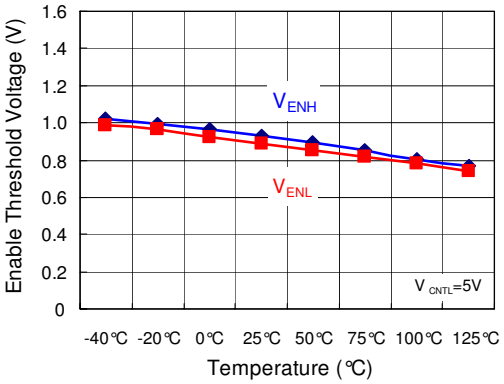


V_{FB} vs. Temperature

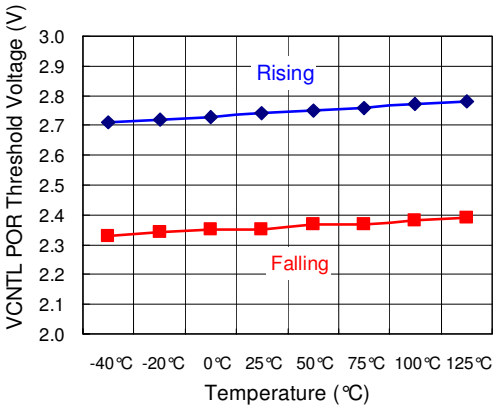


Quiescent Current vs. Temperature

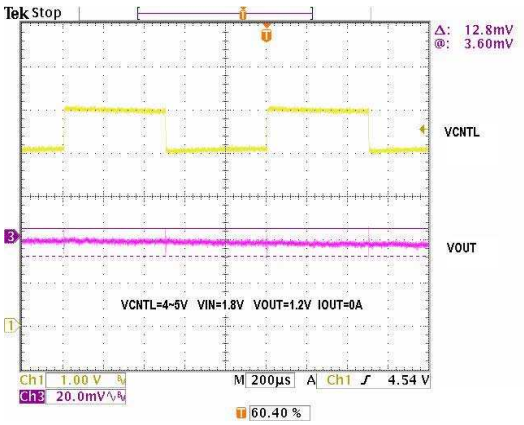
Typical Performance Characteristics (continued)



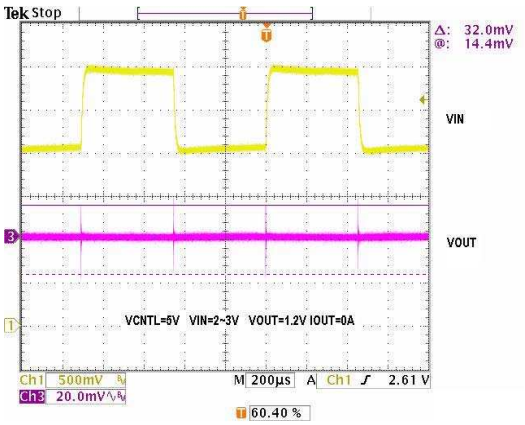
Enable Threshold Voltage vs.Temperature



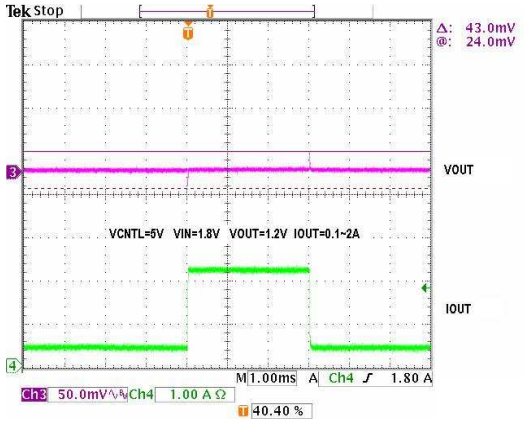
V_{CNTL} POR Threshold vs.Temperature



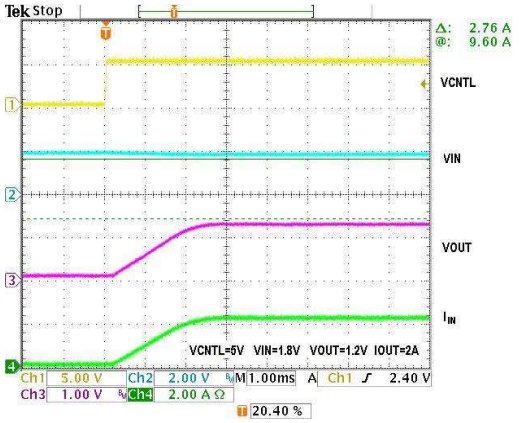
Line Transient



Line Transient

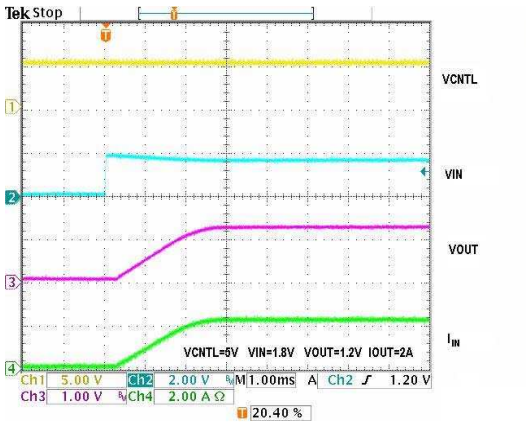


Load Transient

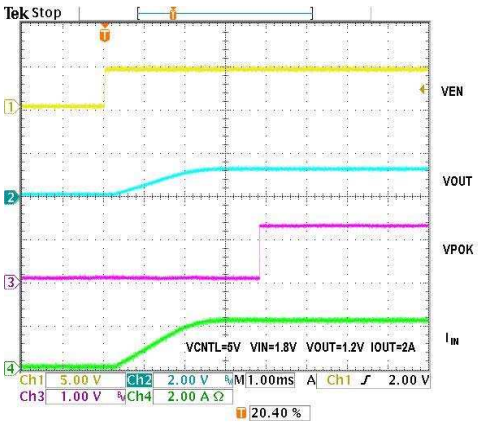


VCNTL Power –ON

Typical Performance Characteristics (continued)

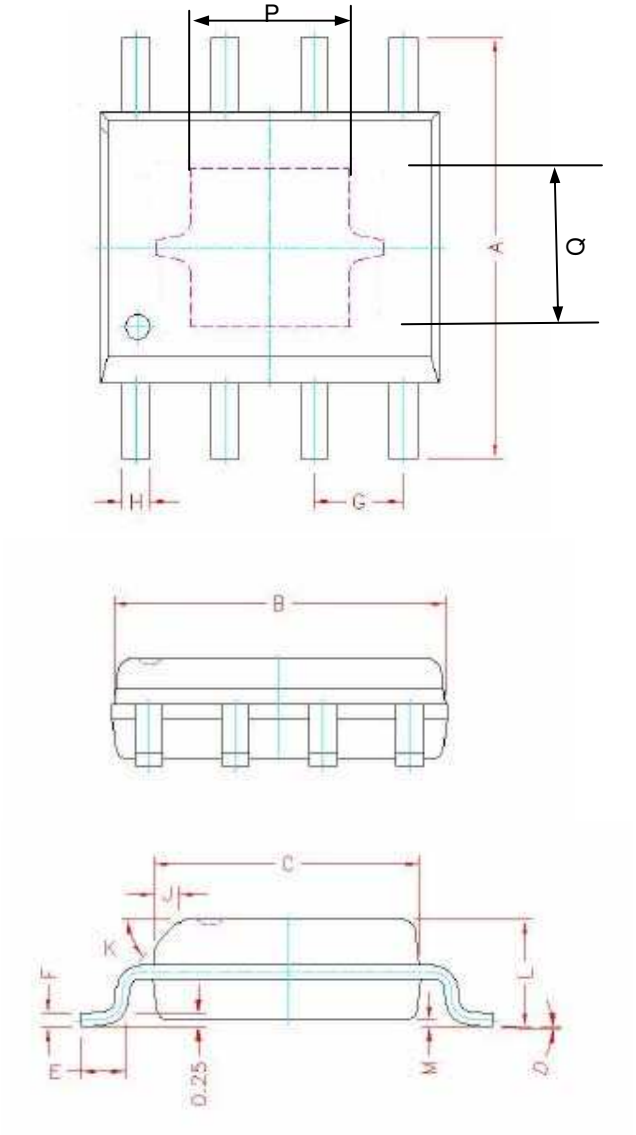


VIN Power –ON



Enable –ON with POK Delay

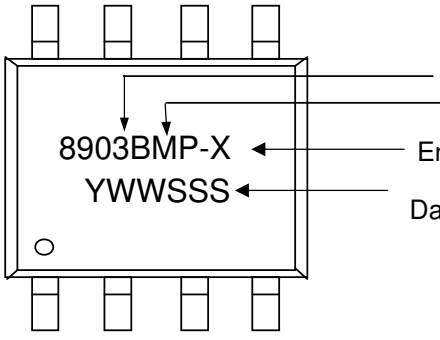
Package Dimensions: ESOP-8



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	5.80	6.00	6.20
B	4.80	4.90	5.00
C	3.80	3.90	4.00
D	0°	4°	8°
E	0.40	0.65	0.90
F	0.19	0.22	0.25
M	0.00	0.08	0.15
H	0.35	0.42	0.49
L	1.35	1.55	1.75
J	0.375 REF.		
K	45°		
G	1.27 TYP.		
P	2.15	2.25	2.35
Q	2.15	2.25	2.35

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



Product : APE8903B

Package code : MP = RoHS-compliant halogen-free ESOP-8

Enable function option (A or B)

Date/lot code (YWWSSS)

Y: Last digit of the year

W: Work week

SSS: Lot code sequence