2A Ultra Low Dropout Linear Regulator

Features

- **Dropout of 0.23V (typ.) at 2A at 1.2V Output Voltage**
- **Low ESR Output Capacitor (Multi-layer Chip Capacitors (MLCC)) Applicable**
- **Enable Pin Option - Pull Low (-A) or Pull High (-B)**
- **Fast Transient Response**
- **Adjustable Output Voltage by External Resistors**
- **Power-On-Reset Monitoring on Both VCNTL and VIN Pins**
- **Internal Soft-Start**
- **Under-Voltage Protection**
- **Current-Limit and Thermal Shutdown Protection**
- **Power-OK Output with a Delay Time**
- **RoHS-compliant halogen-free ESO-8 package**

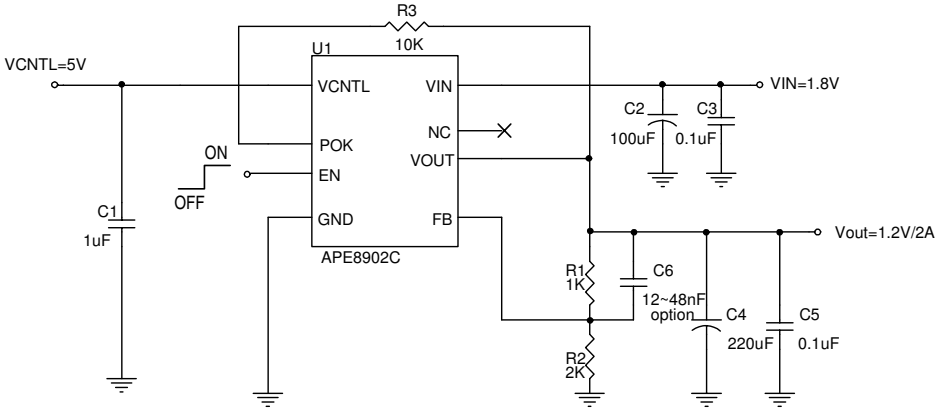
Description

The APE8902C is a 2A ultra low dropout linear regulator, specifically designed to provide reliable supply voltages for front-side-bus termination on motherboards and NB applications. The IC needs two supply voltages, a control voltage for the circuitry and a main supply voltage for power conversion, to reduce power dissipation and provide extremely low dropout. The APE8902C integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages to prevent incorrect operation. Thermal shutdown and current limit functions protect the device against thermal and current over-loads. A POK indicates the output status with a time delay which is set internally, and can control another converter for power sequencing. The APE8902C can be enabled by another power system. Pulling and holding the EN pin below 0.6V shuts off the output.

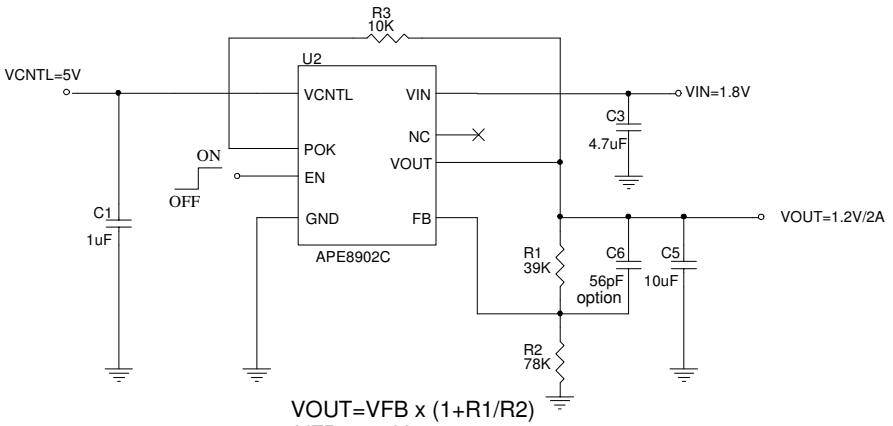
The APE8902CMP is available in an ESO-8 package, which features the small size of an SO-8 with an exposed pad to reduce the junction-to-case thermal impedance, and is suitable for 2-3W applications.

Typical Application

1. Using an Aluminum Electrolytic Output Capacitor



2. Using an MLCC Output Capacitor



VOUT=VFB x (1+R1/R2)
VFB = 0.8V

Absolute Maximum Ratings (at T_A = 25℃)

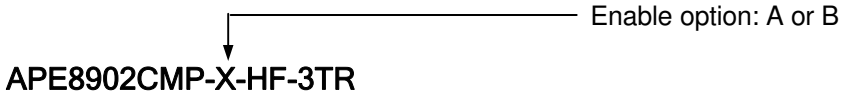
VCNTL Supply Voltage (V_{CNTL})	-0.3V to 6.5V
VIN Supply Voltage (V_{IN})	-0.3V to 6.5V
EN & FB Pin Voltage (V_{EN}, V_{FB})	-0.3V to VCNTL+0.3V
Power Good Voltage (V_{POK})	-0.3V to 6.5V
Output Voltage (V_{OUT})	0.8V to 6V
Power Dissipation (P_D)	2.5W
Storage Temperature Range (T_{ST})	-65℃ to 150℃
Junction Temperature Range (T_J)	-40℃ to 150℃
Thermal Resistance, Junction-Ambient (Rth_{ja})	
ESOP-8	40℃/W
Thermal Resistance, Junction-Case (Rth_{jc})	
ESOP-8	15℃/W

Note. Rth_{ja} is measured with a PCB copper area (must be connected to the exposed pad) of approximately 1.5 in^2 (Multi-layer).

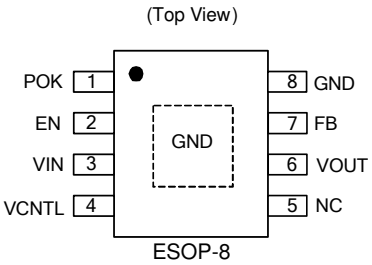
Recommended Operating Conditions

Operating Junction Temperature Range (T_{OJ})	-40℃ to 125℃
Operating Ambient Temperature Range (T_{OA})	-40℃ to 85℃
V_{CNTL} Supply Voltage (VCNTL)	3V to 6V
VIN Supply Voltage (V_{IN})	1.1V to 5.5V
Output Voltage (V_{OUT}) with V_{CNTL}=5V	0.8V to 2.8V
Output Current (I_{OUT})	0A to 2A

Ordering Information



Pin Configuration



Electrical Specifications

(V_{CNTL} = 5V, V_{IN} = 1.8V, V_{OUT} = 1.2V, T_A=25°C unless otherwise specified)

Parameter	SYM	TEST CONDITION		MIN	TYP	MAX	UNITS
V_{CNTL} POR Threshold	V_{CNTL}			2.5	2.7	2.9	V
V_{CNTL} POR Hysteresis	$V_{CNTL(hys)}$			-	0.4	-	V
V_{IN} POR Threshold	V_{IN}			0.8	0.9	1	V
V_{IN} POR Hysteresis	$V_{IN(hys)}$			-	0.5	-	V
V_{CNTL} Nominal Supply Current	I_{CNTL}	EN= V_{CNTL}		0.4	1	1.5	mA
V_{CNTL} Shutdown Current	I_{SD}	EN = 0V	APE8902CMP-A	-	-	1	uA
			APE8902CMP-B	-	10	30	uA
Feedback Voltage	V_{FB}	V_{CNTL}=3 ~ 6V, I_{OUT}=10mA, V_{IN}=V_{OUT}+0.5~5.5V		0.784	0.8	0.816	V
Load Regulation		I_{OUT}=0A ~ 2A		-	0.2	1	%
On Resistance	$R_{DS(ON)}$	I_{OUT}=100mA, V_{CNTL}=V_{EN}=5.0V, V_{OUT}=1.2V		-	115	150	mΩ
Dropout Voltage	V_{DROP}	I_{OUT} = 2A, V_{CNTL}=5V, V_{OUT} = 1.2V		-	0.23	0.3	V
V_{OUT} Pull Low Resistance		EN=0V		-	90	-	Ω
Soft Start Time	T_{SS}			-	2	-	ms
EN Pin Logic High Threshold Voltage	V_{ENH}	Enable		1.2	-	-	V
	V_{ENL}	Disable		-	-	0.6	
EN Hysteresis				-	40	-	mV
EN Pin Pull-Up Current	I_{EN}	EN=5V, APE8902CMP-A		-	10	20	uA
		EN=GND, APE8902CMP-B		-	10	20	
Current Limit	I_{LIM}	V_{CNTL}=5V, V_{IN}=V_{OUT}+1V		2.5	2.8	-	A
Ripple Rejection	V_{IN}	PSRR	F=120Hz, I_{OUT}=100mA	-	65	-	dB
	V_{CNTL}			-	65	-	
Inrush Current		V_{CNTL}=5V, C_{OUT}=10uF, EN startup, I_{OUT}=2A		-	0.5	-	A
Under-Voltage Threshold		VFB Falling		-	0.4	-	V
POK Threshold Voltage for Power OK	V_{POK}	VFB Rising		-	92%	-	VFB
POK Threshold Voltage for Power Not OK	V_{PNOK}	VFB Falling		-	81%	-	VFB
POK Low Voltage		POK sinks 5mA		-	0.25	0.4	V
POK Delay Time	T_{DELAY}			0.8	2	10	ms
Thermal Shutdown Temp	TSD			-	160	-	°C
Thermal Shutdown Hysteresis				-	40	-	°C

Pin Descriptions

PIN SYMBOL	PIN DESCRIPTION
POK	Power OK Output Pin
EN	Internal Pull High (APE8902CMP-B) or Pull Low (APE8902CMP-A) EN=High -> Enable EN=Low -> Shutdown Mode
VIN	Input Voltage.
VCNTL	CNTL Pin Input Voltage
NC	No Connect
VOUT	Output Voltage
FB	Feedback Pin
GND	GND Pin

Pin Functions

FB

Connecting this pin to an external resistor divider receives the feedback voltage of the regulator. The output voltage set by the resistor divider is determined by:

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right) \quad (V)$$

where R1 is connected from VOUT to FB with Kelvin sensing and R2 is connected from FB to GND. A bypass capacitor may be connected in parallel with R1 to improve the load transient response. The recommended range for R2 is 1k~4.7kΩ for an AL output capacitor and 30k~100kΩ where an MLCC output capacitor is used.

VIN

Main supply input pins for power conversion. The voltage at this pin is monitored for Power-On Reset purpose.

VCNTL

Power input pin of the control circuitry. Connecting this pin to a +5V (recommended) supply voltage provides the bias for the control circuitry. The voltage at this pin is monitored for Power-On Reset purpose.

POK

Power-OK signal output pin. This pin is an open-drain output used to indicate status of output voltage by sensing FB voltage. This pin is pulled low when the rising FB voltage is not above the VPOK threshold or the falling FB voltage is below the VPOK threshold, indicating the output is not OK.

EN

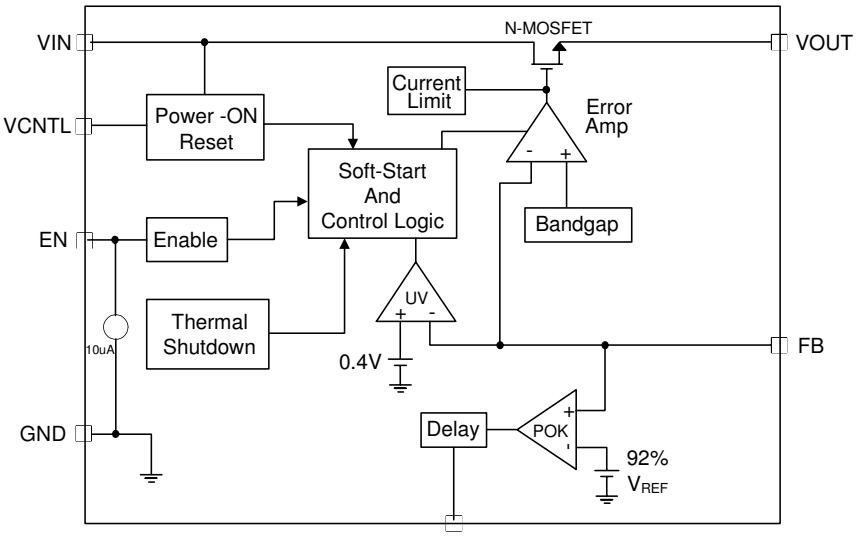
Enable control pin. Pulling and holding this pin below 0.6V shuts down the output. When re-enabled, the IC undergoes a new soft-start cycle. For APE8902CMP-B, this pin is pulled up internally to the VCNTL voltage, enabling the regulator. For APE8902CMP-A, this pin is pulled down internally to the GND voltage, shutting down the regulator. The pull-high or pull-low current is 10uA (typ.)

VOUT

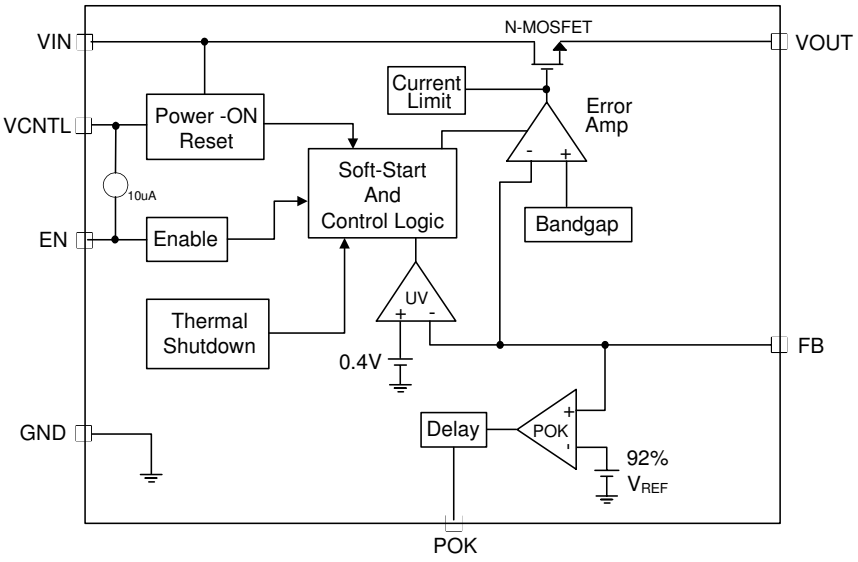
Regulator output pin. Use of wide tracks for this pin is recommended. It is also necessary to connect an output capacitor to this pin for closed-loop compensation and improved transient response.

Block Diagrams

APE8902CMP-A



APE8902CMP-B



Functional Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors input voltages at both CNTL and VIN pins to prevent incorrect operation. The POR function initiates a soft-start process after the two supply voltages exceed their rising POR threshold voltages during powering on. The POR function also pulls low the POK pin regardless of the output voltage when the VCNTL voltage falls below its falling POR threshold.

Internal Soft-Start

An internal soft-start function controls the slew rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 2ms.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier, designed with high bandwidth and DC gain, provides very fast transient response and improved load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS FET which provides the load current from VIN to VOUT.

Current-Limit

The APE8902C monitors the current via the output NMOS FET and limits the maximum current to prevent damage to the load and the APE8902C during overload or short-circuit conditions.

Under-Voltage Protection (UVP)

The APE8902C monitors the voltage on FB pin after the soft-start process is finished. The UVP is disabled during the soft-start. When the voltage on the FB pin falls below the under-voltage threshold, the UVP circuit shuts off the output immediately. After a while, the APE8902C starts a new soft-start to regulate output.

Thermal Shutdown

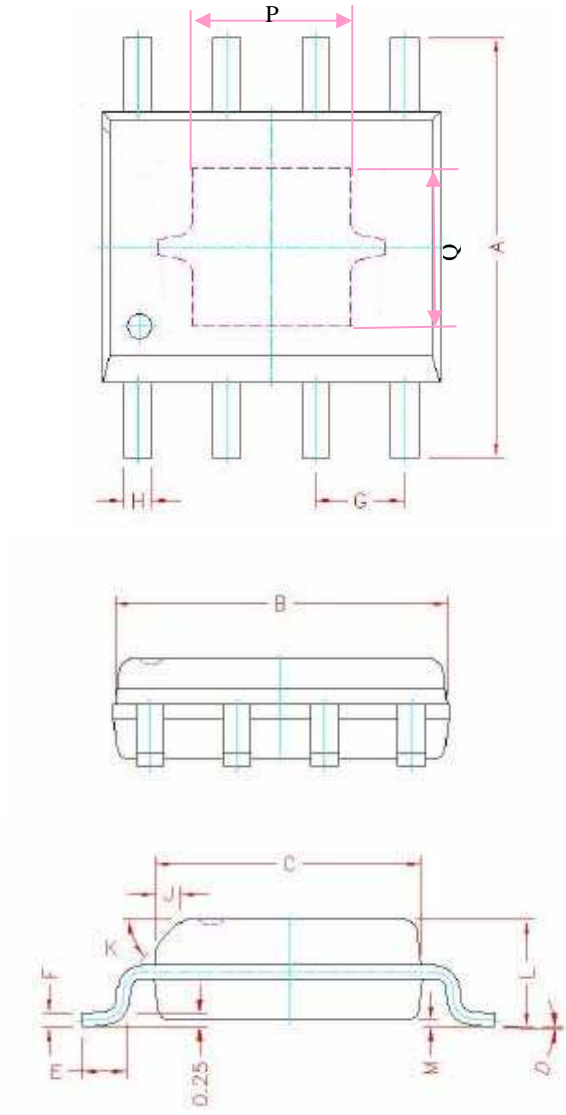
The thermal shutdown circuit limits the junction temperature of the APE8902C. When the junction temperature exceeds +160℃, a thermal sensor turns off the output NMOS FET, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40℃, resulting in a pulsed output during continuous thermal overload conditions.

Applications Information

Capacitor Selection

MLCC capacitors are normally recommended for the input and output of the APE8902C. Larger input capacitor values provide better supply-noise rejection and transient response. A higher value of output capacitor may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. The X5R and X7R type of MLCC are recommended. If using aluminum electrolytic capacitors, 100uF for the input capacitor and 220uF for the output capacitor ($30m\Omega < ESR < 200m\Omega$) are recommended. Output capacitors of larger value can reduce noise and improve load transient response, stability, and PSRR.

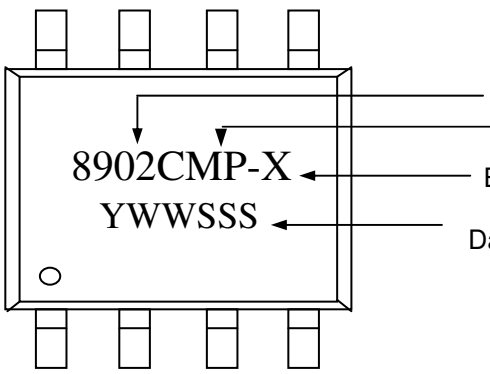
Package Dimensions: ESO-8



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	5.80	6.00	6.20
B	4.80	4.90	5.00
C	3.80	3.90	4.00
D	0°	4°	8°
E	0.40	0.65	0.90
F	0.19	0.22	0.25
M	0.00	0.08	0.15
H	0.35	0.42	0.49
L	1.35	1.55	1.75
J	0.375 REF.		
K	45°		
G	1.27 TYP.		
P	2.15	2.25	2.35
Q	2.15	2.25	2.35

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



Product: APE8902C

Package Code: MP = RoHS-compliant halogen-free ESO-8

Enable Function: A or B

Date Code (YWWSSS)

Y: Last digit of the year

WW: Work week

SSS: Lot code sequence