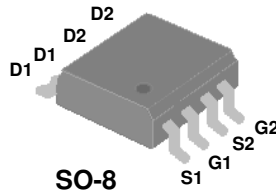




**Complementary N and P-channel
Enhancement-mode Power MOSFETs**

- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Performance
- RoHS-compliant, halogen-free

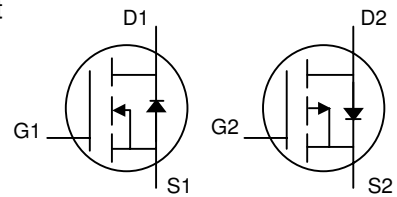


N-CH	BV_{DSS}	100V
	$R_{DS(ON)}$	150mΩ
	I_D	2.5A
P-CH	BV_{DSS}	-100V
	$R_{DS(ON)}$	160mΩ
	I_D	-2.5A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The AP5521GM-HF-3 is in a standard SO-8 package, which is widely used for commercial and industrial surface-mount applications, and is well suited for applications such as DC and servo motor drives.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	100	-100	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D at $T_A=25^\circ C$	Continuous Drain Current ³	2.5	-2.5	A
I_D at $T_A=70^\circ C$	Continuous Drain Current ³	2.0	-2.0	A
I_{DM}	Pulsed Drain Current ¹	10	-10	A
P_D at $T_A=25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	62.5	°C/W

Ordering Information

AP5521GM-HF-3TR : in RoHS-compliant, halogen-free SO-8, shipped on tape and reel (3000 pcs/reel)



N-channel Electrical Specifications at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$B_{V_{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=2A$	-	120	150	m Ω
		$V_{GS}=5V, I_D=1A$	-	145	250	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.4	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=2A$	-	3.3	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=2A$	-	6	10	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=50V$	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=50V$	-	4.5	-	ns
t_r	Rise Time	$I_D=1A$	-	6.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	16	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	5.5	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	420	670	pF
C_{oss}	Output Capacitance	$V_{DS}=15V$	-	70	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	50	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1.5A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time ²	$I_S=2A, V_{GS}=0V$	-	35	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	50	-	nC

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 135°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



P-channel Electrical Specifications at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-2A$	-	125	160	m Ω
		$V_{GS}=-5V, I_D=-1A$	-	145	250	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-2	-3	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-2A$	-	8	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-80V, V_{GS}=0V$	-	-	-10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-2A$	-	14	22.5	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-50V$	-	4	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	7	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-50V$	-	10	-	ns
t_r	Rise Time	$I_D=-1A$	-	5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	50	-	ns
t_f	Fall Time	$V_{GS}=-10V$	-	21	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1400	2240	pF
C_{oss}	Output Capacitance	$V_{DS}=-15V$	-	135	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-1.5A, V_{GS}=0V$	-	-	-1.3	V
t_{rr}	Reverse Recovery Time ²	$I_S=-2A, V_{GS}=0V$	-	40	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	80	-	nC

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 135°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

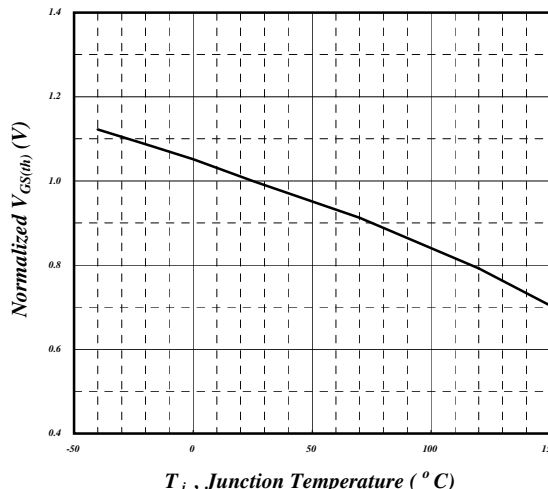
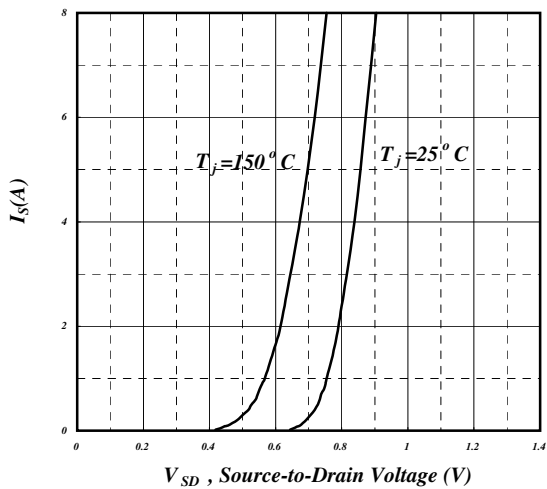
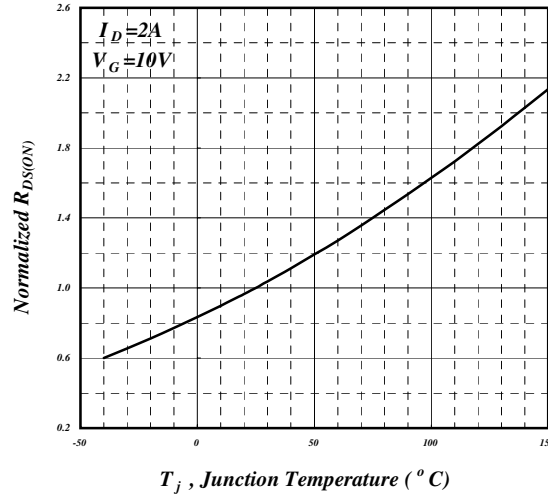
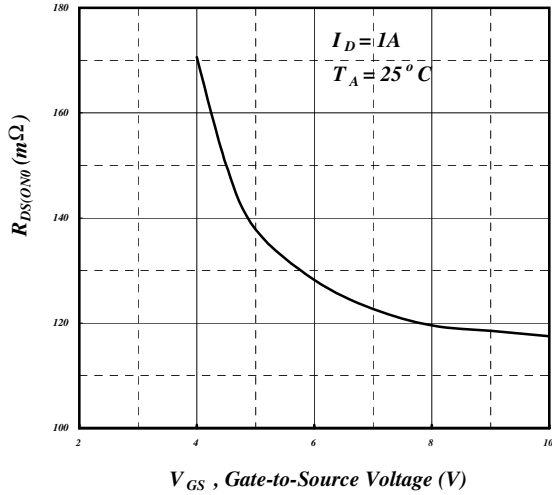
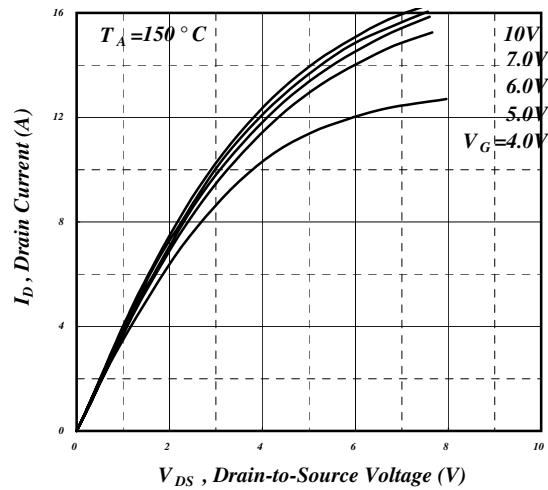
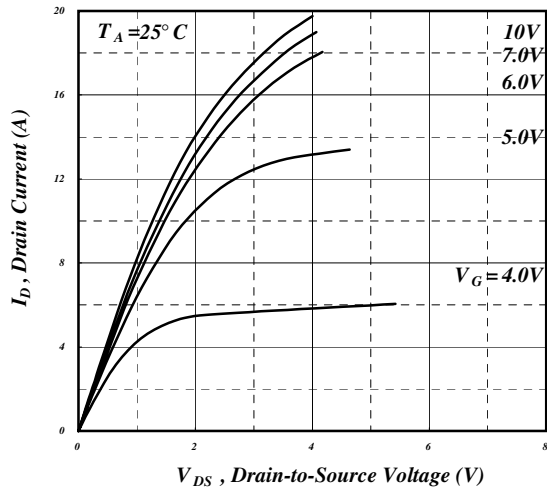
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Typical N-channel Electrical Characteristics





Typical N-channel Electrical Characteristics (cont.)

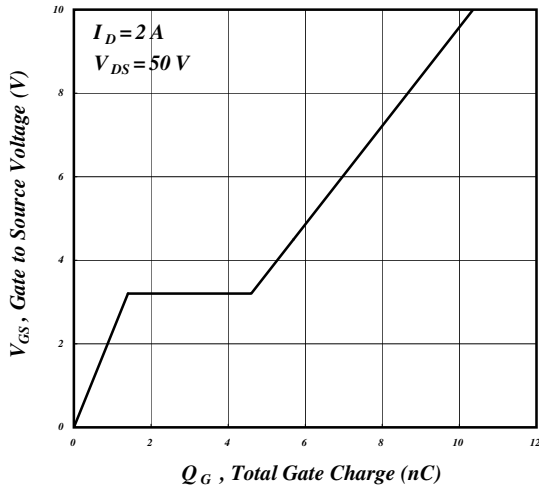


Fig 7. Gate Charge Characteristics

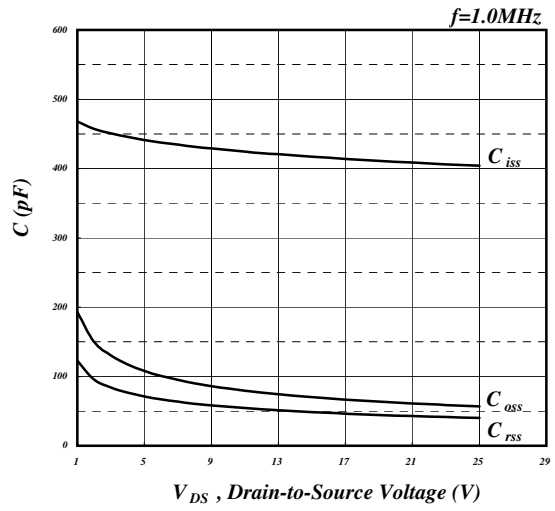


Fig 8. Typical Capacitance Characteristics

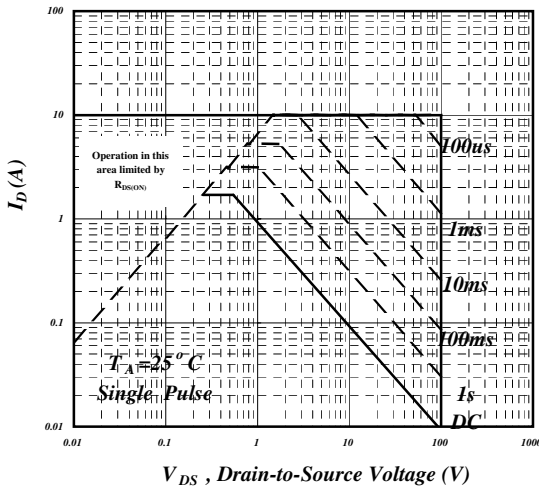


Fig 9. Maximum Safe Operating Area

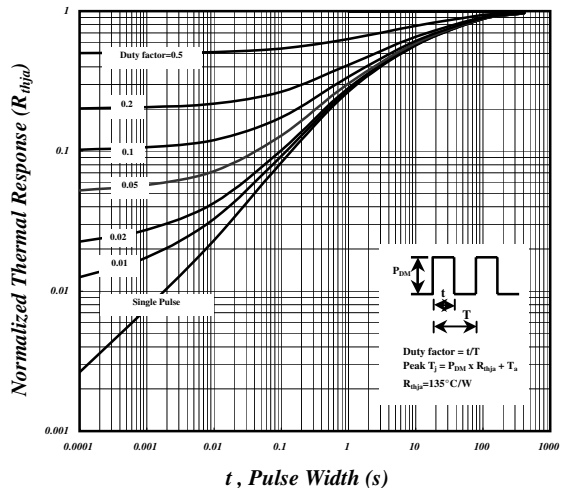


Fig 10. Effective Transient Thermal Impedance

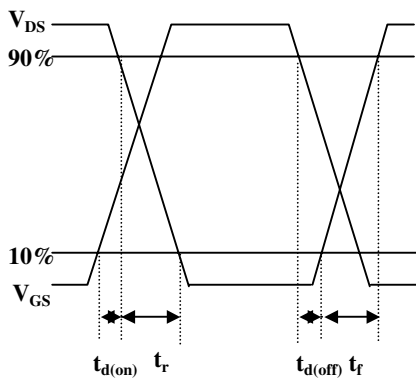


Fig 11. Switching Time Waveform

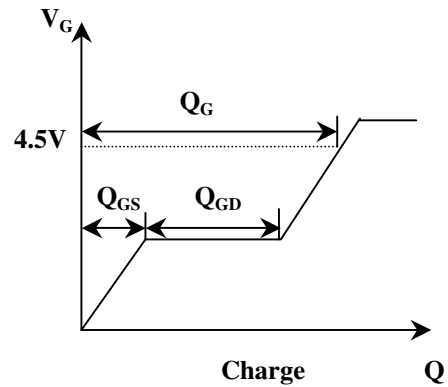


Fig 12. Gate Charge Waveform



Typical P-channel Electrical Characteristics

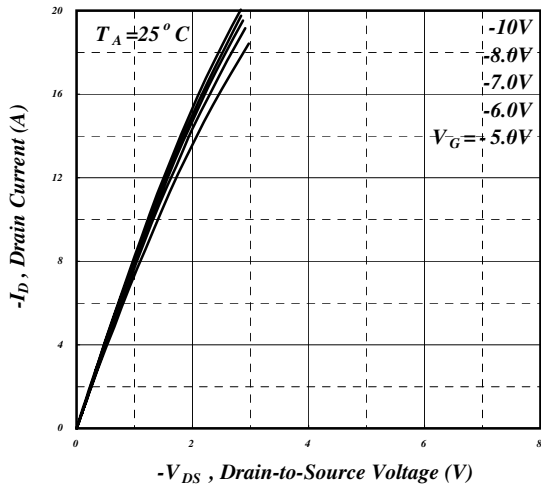


Fig 1. Typical Output Characteristics

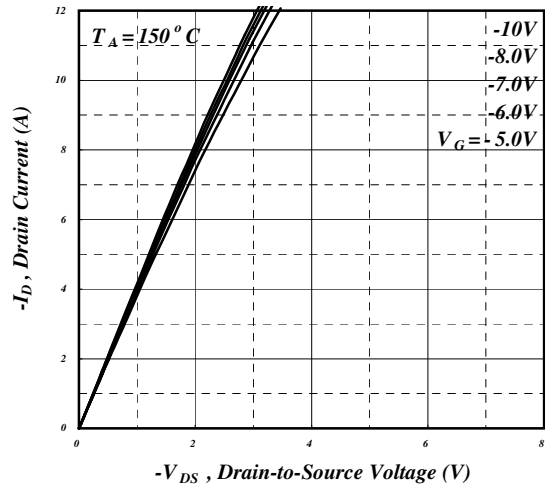


Fig 2. Typical Output Characteristics

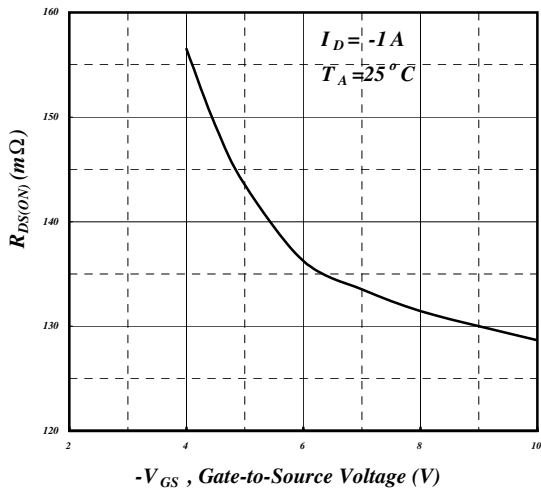


Fig 3. On-Resistance vs. Gate Voltage

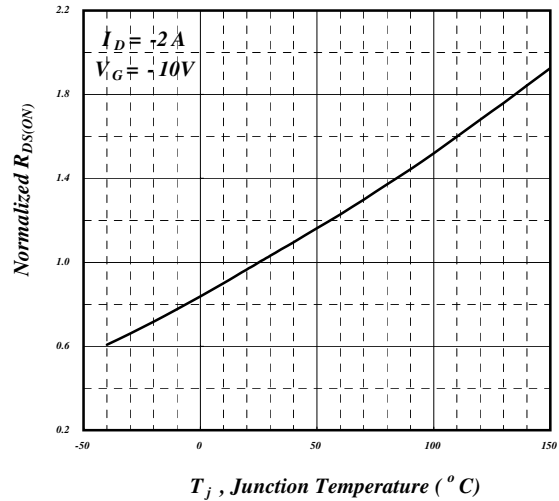


Fig 4. Normalized On-Resistance vs. Junction Temperature

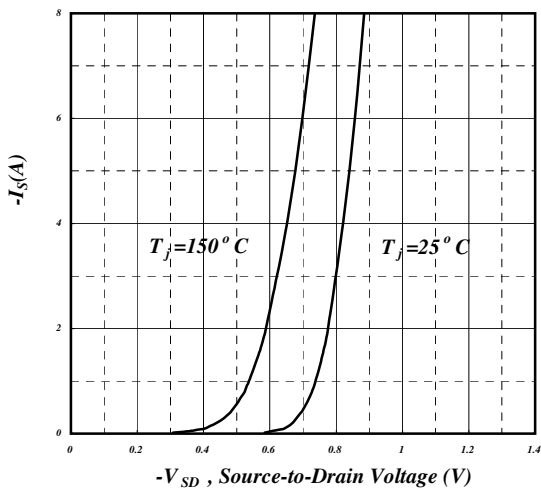


Fig 5. Forward Characteristic of Reverse Diode

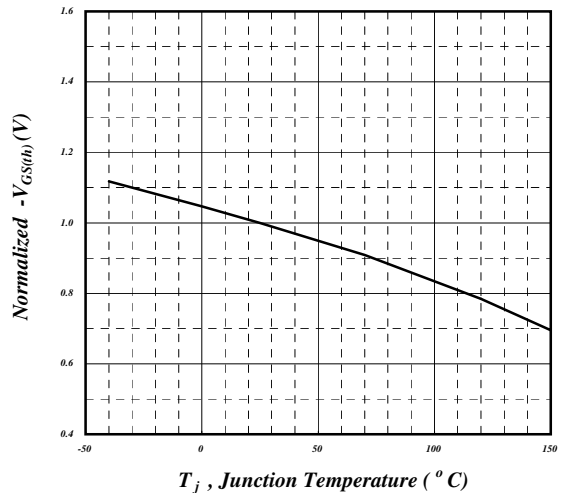


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical P-channel Electrical Characteristics (cont.)

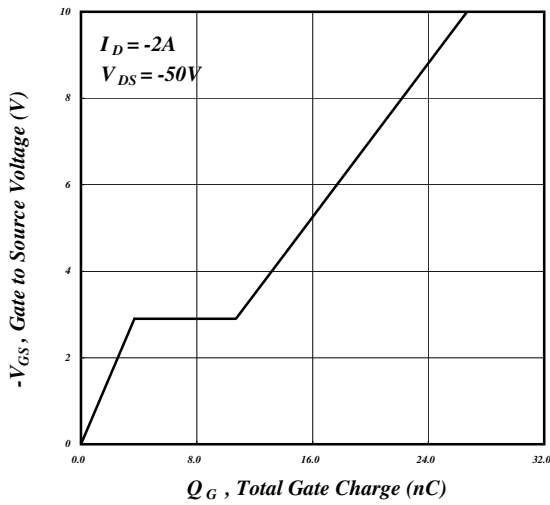


Fig 7. Gate Charge Characteristics

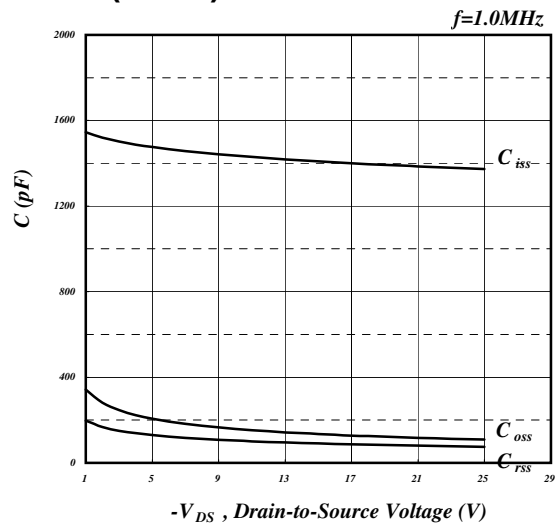


Fig 8. Typical Capacitance Characteristics

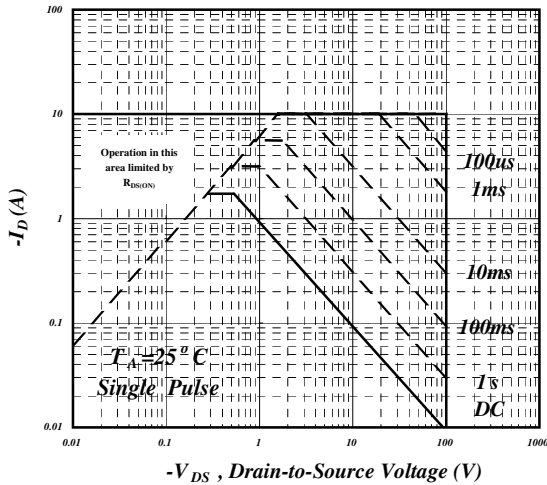


Fig 9. Maximum Safe Operating Area

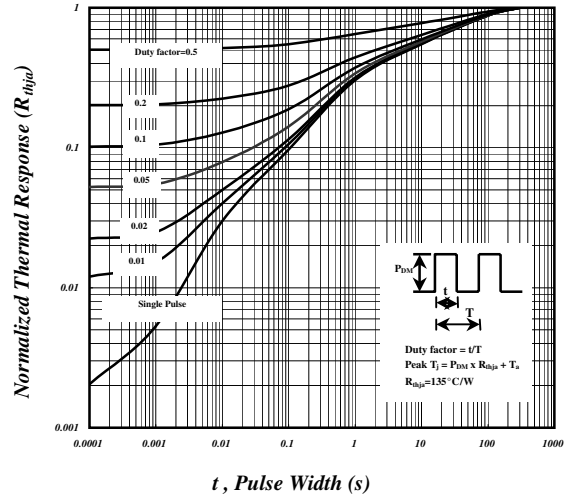


Fig 10. Effective Transient Thermal Impedance

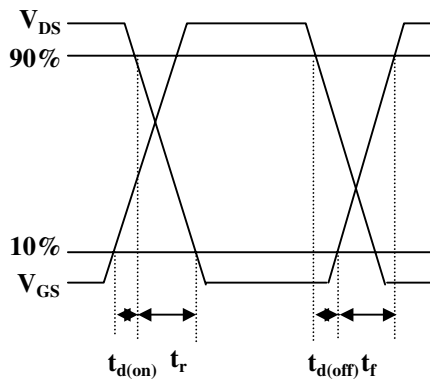


Fig 11. Switching Time Waveform

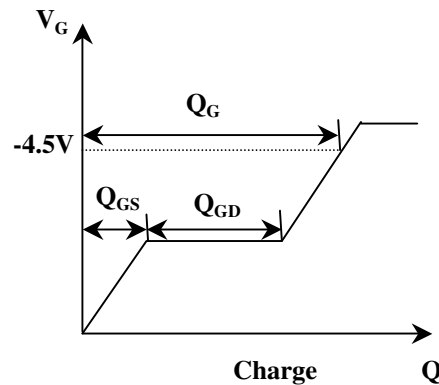
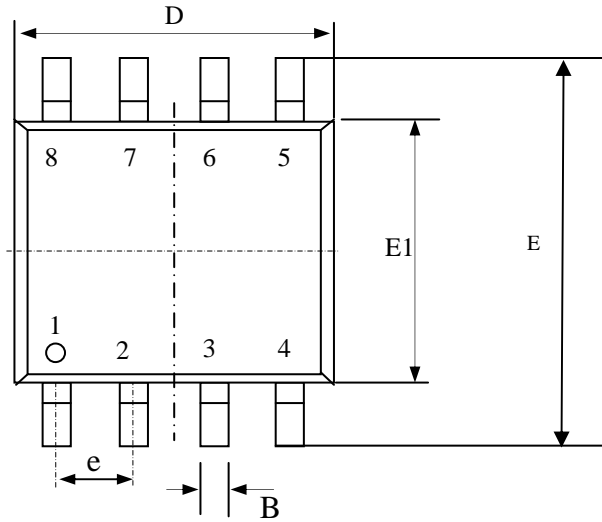


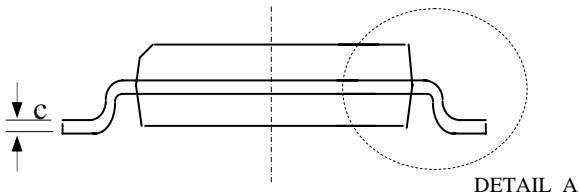
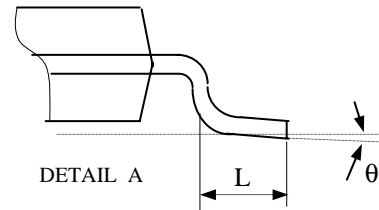
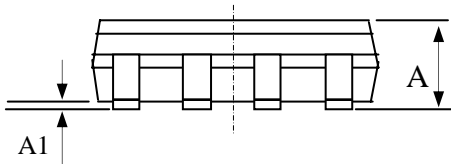
Fig 12. Gate Charge Waveform



Package Dimensions: SO-8

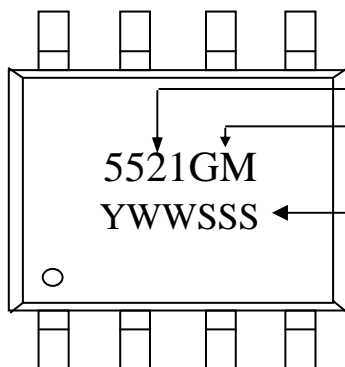


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.15	6.50
L	0.38	0.71	1.27
θ	0	4.00	8.00
e	1.27 TYP		



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information:



Product: AP5521
 Package:
 GM = RoHS-compliant halogen-free SO-8
 Date/lot code (YWWSSS)
 Y: Last digit of the year
 WW: Work week
 SSS: Lot code sequence