



Low Voltage Adjustable Shunt Regulators

Features

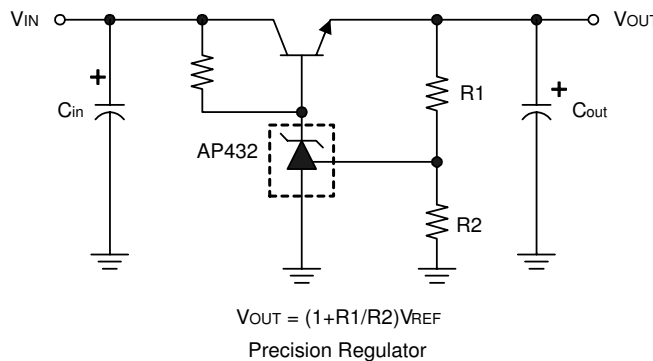
- Precision reference voltage
 B : 1.24V ±1%
 A : 1.24V ±0.5%
- Sink current capability: 200mA.
- Minimum cathode current for regulation: 150µA
- Equivalent full-range temp coefficient: 30 ppm/°C
- Fast turn-on response.
- Low dynamic output impedance: 0.2Ω
- Programmable output voltage to 20v
- Low output noise
- Packages: SOT-89, SOT-23, SOT-23-5L, SO-8 and TO-92
- RoHS-compliant, halogen-free (HF)

Description

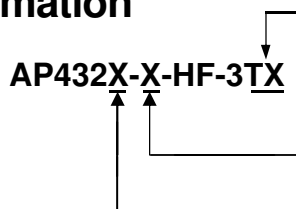
The AP432-3 are 3-terminal adjustable precision shunt regulators with guaranteed temperature stability over the applicable extended commercial temperature range. The output voltage may be set at any level greater than 1.24V (VREF) up to 20V merely by selecting two external resistors that act as a voltage divider network. These devices have a typical output impedance of 0.2Ω. Active output circuitry provides very sharp turn-on characteristics, making these devices excellent improved replacements for Zener diodes in many applications.

The precise +/- 1% reference voltage tolerance of the AP432x-B-3 makes it possible in many applications to avoid the use of a variable resistor, consequently saving cost and eliminating the drift and reliability problems associated with it.

Typical Application



Ordering information



Packing: TB = tubes (for TO-92)
 TR = tape and reel (surface mount packages only)

Reference Voltage and Tolerance:
 A : 1.24V +/- 0.5%
 B or omitted : 1.24V +/- 1%

Package code:
 M : SO-8
 G : SOT-89
 T : TO-92
 N : SOT-23
 Y : SOT-23-5L

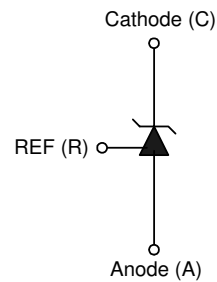
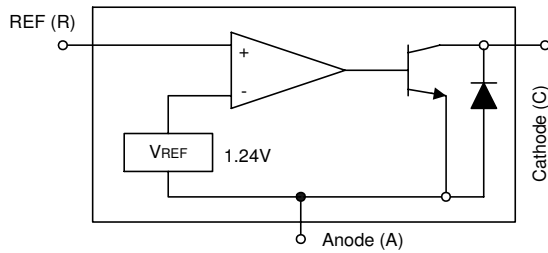
For example, AP432Y-A-HF-3TR:

AP432 0.5% tolerance in RoHS-compliant HF SOT-23-5L, packed in tape and reel



Block Diagram

Symbol



Pin Configurations

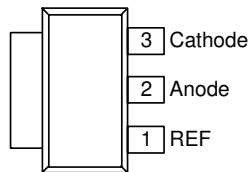
Order Number

Pin Configuration (Top View)

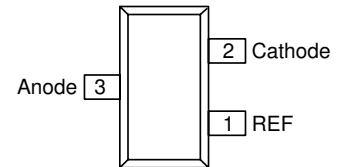
Order Number

Pin Configuration (Top View)

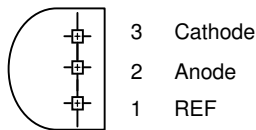
AP432G
(SOT-89)



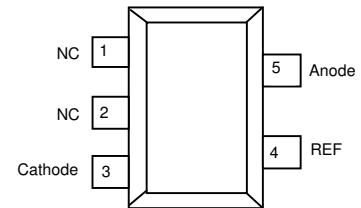
AP432N
(SOT-23)



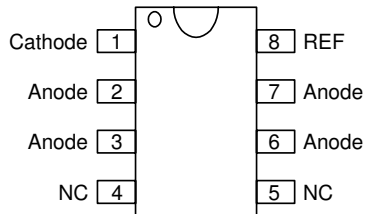
AP432T
(TO-92)



AP432Y
(SOT-23-5L)



AP432M
(SO-8)



THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

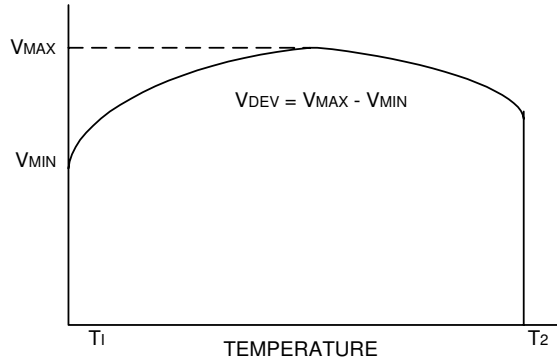
APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Electrical Characteristics (cont.) (Ta=25°C, unless otherwise specified.)

Note 3. Deviation of reference input voltage over temperature.



Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference over the full temperature range.

The average temperature coefficient of the reference input voltage αV_{REF} is defined as:

$$|\alpha V_{REF}| = \frac{\left(\frac{V_{DEV}}{V_{REF(25^\circ C)}}\right) \times 10^6}{T_2 - T_1} \dots\dots\dots (\text{ppm}/^\circ\text{C})$$

Where:

T₂ – T₁ = full temperature change.

αV_{REF} can be positive or negative depending on whether the slope is positive or negative.

Note 4. The dynamic output impedance, R_Z

The dynamic output impedance, R_Z, is defined as:

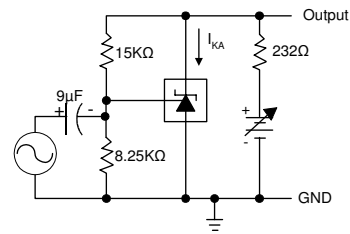
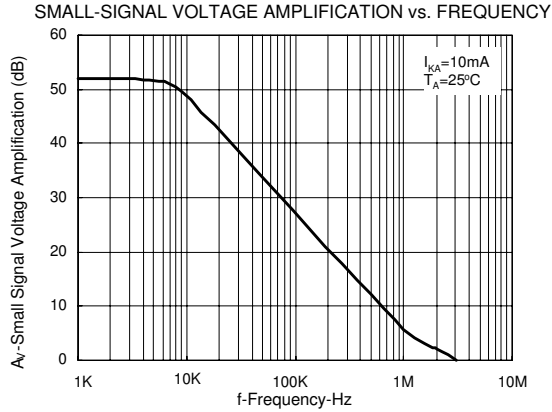
$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$$

When the device is programmed with two external resistors R₁ and R₂ (see Figure 2.), the dynamic output impedance of the overall circuit, is defined as:

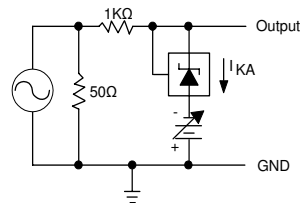
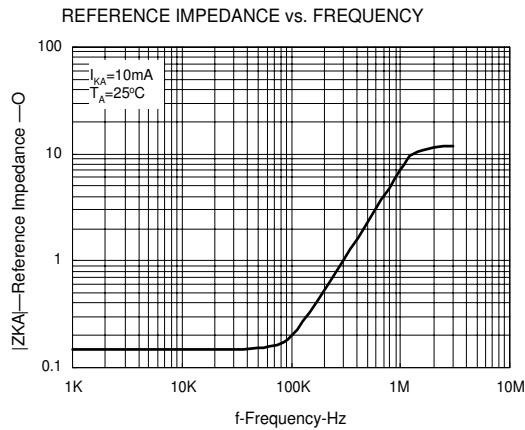
$$|Z_{KA}'| = \frac{\Delta V}{\Delta i} \sim |Z_{KA}| \left(1 + \frac{R_1}{R_2}\right)$$



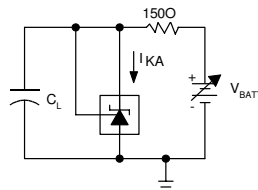
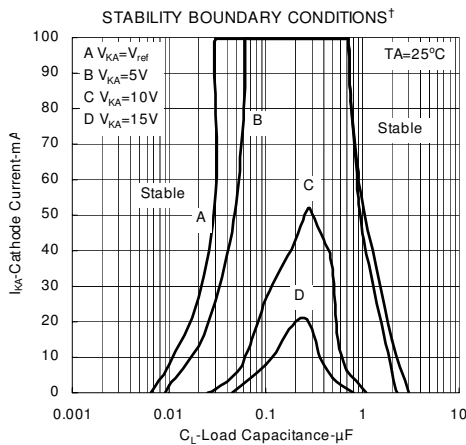
Electrical Characteristics (cont.) (Ta=25°C, unless otherwise specified.)



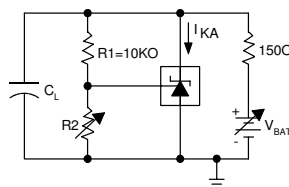
TEST CIRCUIT FOR VOLTAGE AMPLIFICATION



TEST CIRCUIT FOR REFERENCE IMPEDANCE



TEST CIRCUIT FOR CURVE A

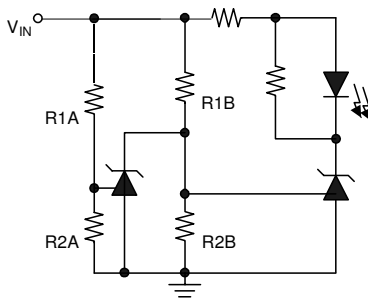


TEST CIRCUIT FOR CURVE B, C, AND D

† The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_{KA} conditions with $C_L=0. V_{BATT}$ and C_L were then adjusted to determine the ranges of stability.

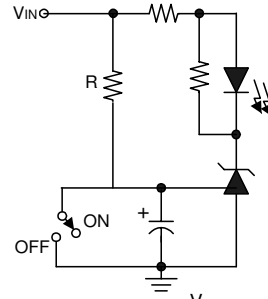


Application Examples



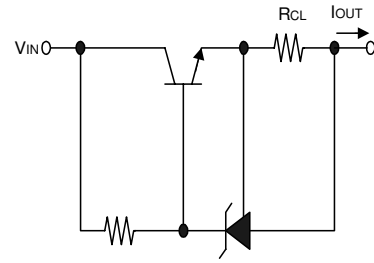
LED on when Low Limit < VIN < High Limit
Low Limit ≈ VREF (1 + R1B/R2B)
High Limit ≈ VREF (1 + R1A/R2A)

Fig.4 Voltage Monitor



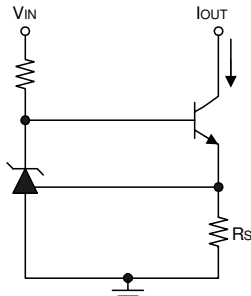
$$\text{Delay} = RC \times \ln\left(\frac{V_{IN}}{V_{IN} - V_{REF}}\right)$$

Fig.5 Delay Timer



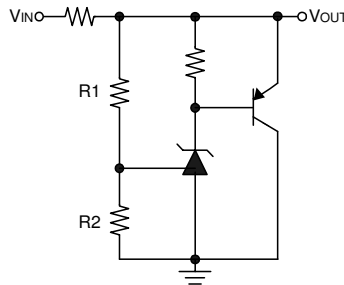
$$I_{OUT} = V_{REF} / R_{CL}$$

Fig.6 Current Limiter or Current Source



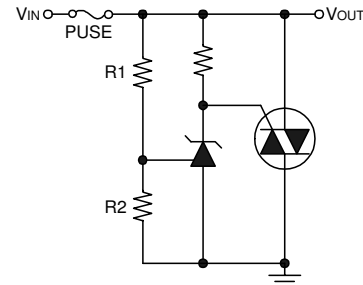
$$I_{OUT} = V_{REF} / R_s$$

Fig.7 Constant-Current Sink



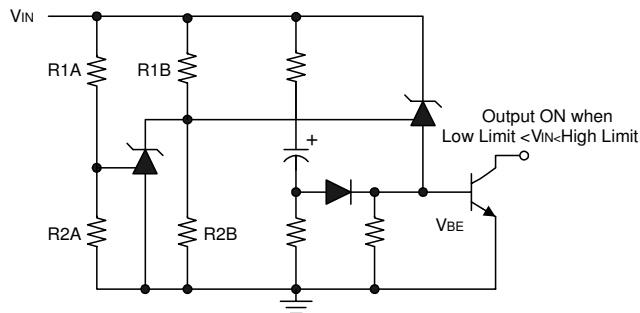
$$V_{OUT} = (1 + R1/R2) \times V_{REF}$$

Fig.8 Higher-Current Shunt Regulator



$$\text{LIMIT} \approx (1 + R1/R2) \times V_{REF}$$

Fig.9 Crow Bar

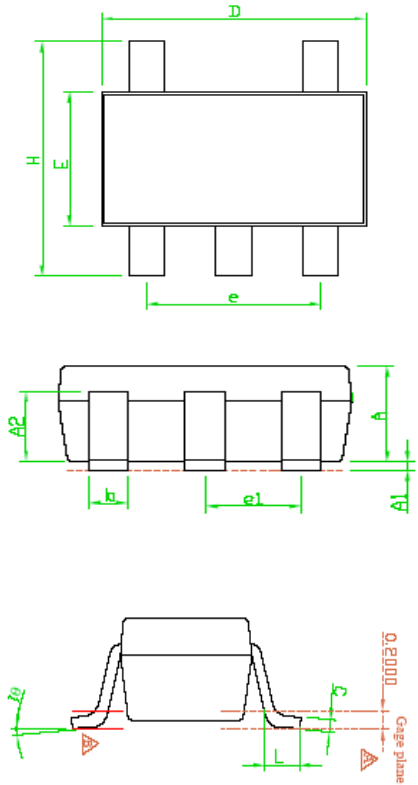


Low Limit ≈ VREF(1 + R1B/R2B) + VBE
High Limit ≈ VREF(1 + R1A/R2A)

Fig.10 Over-Voltage / Under-Voltage Protection Circuit



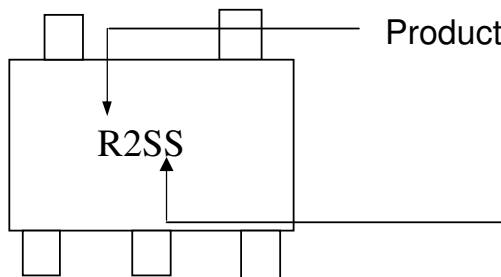
Package Dimensions: SOT-23-5L



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	---	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.50	1.60	1.80
e	---	1.90(TYP)	---
H	2.60	2.80	3.00
L	0.37	---	---
$\theta 1$	1°	5°	9°
e2	---	0.95(TYP)	---

- Note 1: Package body sizes exclude mold flash protrusions or gate burrs.
- Note 2: Tolerance ± 0.1000 mm (4mil) unless otherwise specified.
- Note 3: Coplanarity: 0.1000 mm
- Note 4: Dimension L is measured in gage plane.

Marking Information

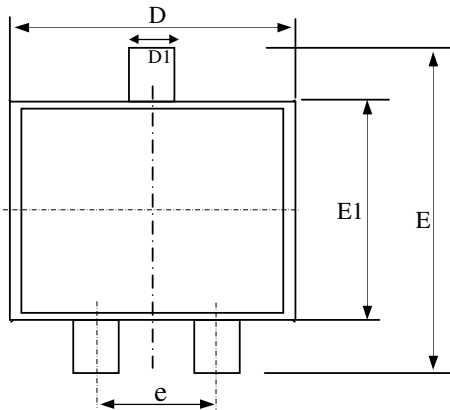


Date/lot code

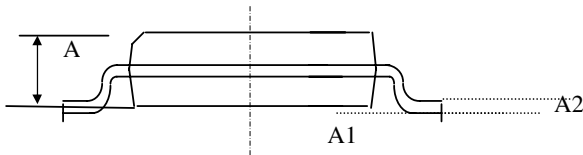
For details of how to convert this to standard YYWW date code format, please contact us directly.



Package Dimensions: SOT-23

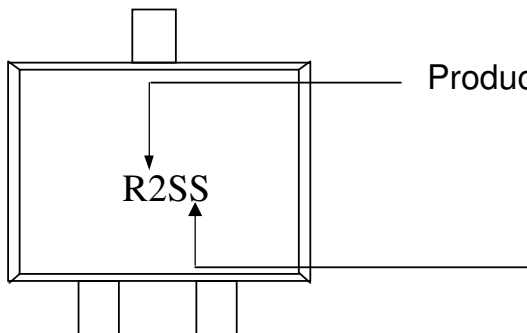


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.00	1.15	1.30
A1	0.00	--	0.10
A2	0.10	0.15	0.25
D1	0.30	0.40	0.50
e	1.70	2.00	2.30
D	2.70	2.90	3.10
E	2.40	2.65	3.00
E1	1.40	1.50	1.60



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information

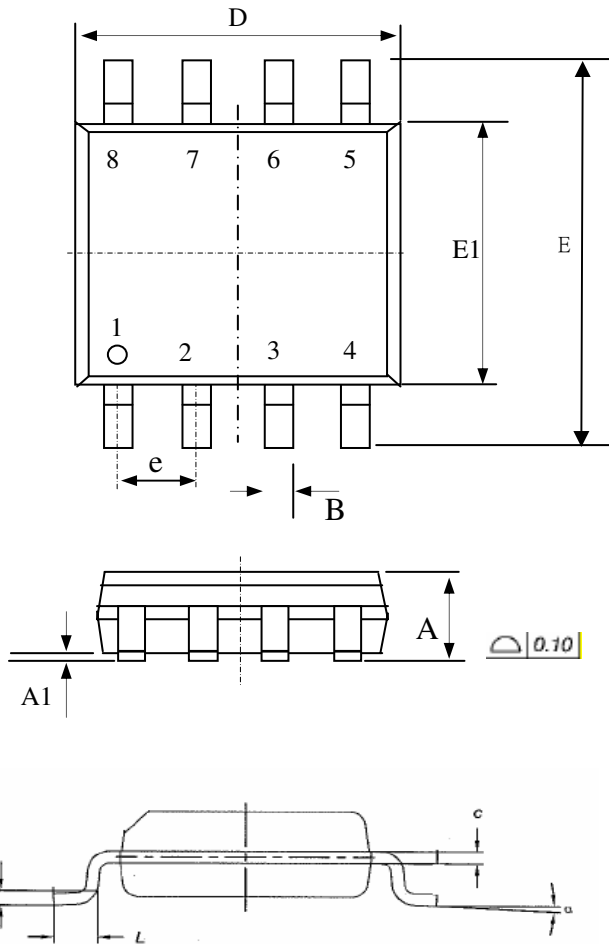


Date/lot code

For details of how to convert this to standard YYWW date code format, please contact us directly.



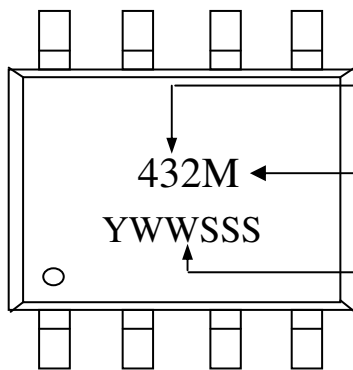
Package Dimensions: SO-8



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
c	0.19	0.22	0.25
D	4.80	4.90	5.00
E	5.80	6.15	6.50
E1	3.80	3.90	4.00
e	1.27 TYP		
G	0.254 TYP		
L	0.38	—	0.90
α	0.00	4.00	8.00

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



Product: AP432

Package code:

M = SO-8

Date/lot code (YWWSSS)

Y: Last Digit Of The Year

WW: Work week

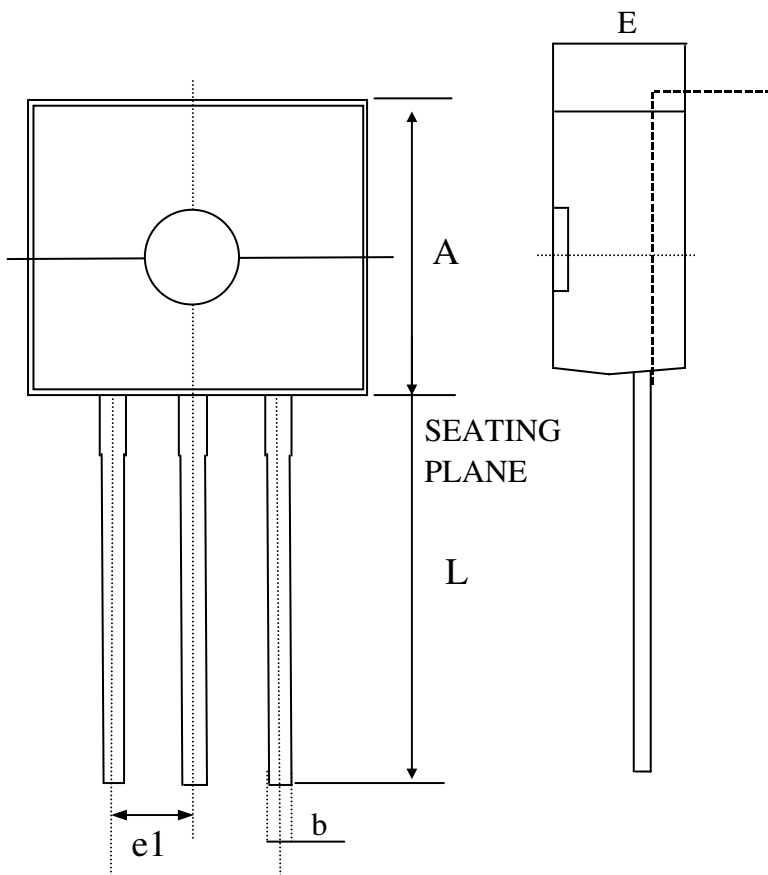
SSS: Lot code sequence

If last "S" is a number, the product is not HF.

If last "S" is a letter, the product is halogen free.

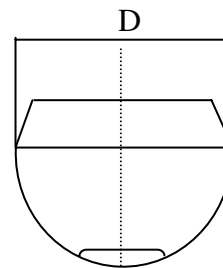


Package Dimensions: TO-92

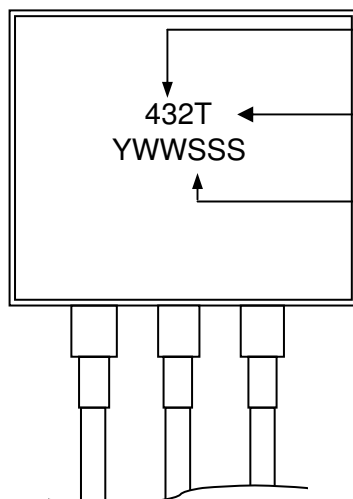


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.32	4.83	5.34
D	4.1	4.8	5.3
E	3.1	3.9	4.7
b	----	0.38	----
L	12.7	---	----
e1	----	1.27	----

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.



Marking Information



Product: AP432

Package code:

T = TO-92

Date/lot code (YWWSSS)

Y: Last Digit Of The Year

WW: Work week

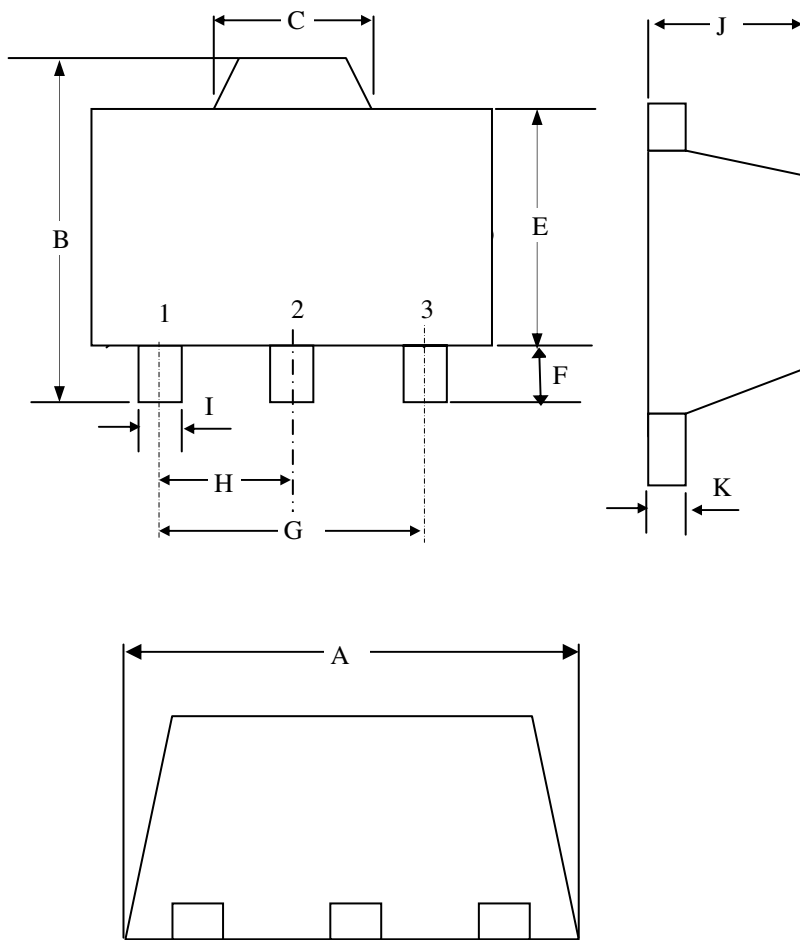
SSS: Lot code sequence

If last "S" is a number, the product is not HF.

If last "S" is a letter, the product is halogen free.



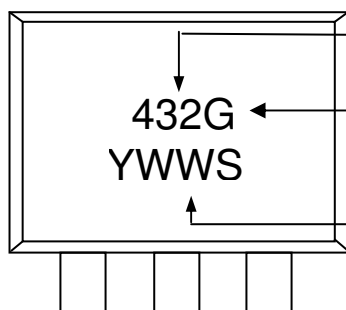
Package Dimensions: SOT-89



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.40	-	4.60
B	4.05	-	4.25
C	1.40	-	1.75
E	2.40	-	2.60
F	0.89	-	1.20
I	0.35	-	0.55
H	----	1.50	----
G	----	3.00	----
J	1.40	-	1.60
K	0.35	-	0.43

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information



Date/lot code (YWWS)

Y: Last Digit Of The Year

WW: Work week

S: Lot code sequence

If "S" has an underline, the product is halogen-free.

If "S" has no underline, the product is not HF.