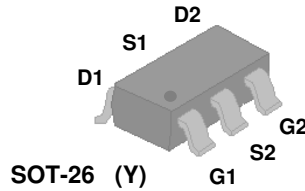




**Complementary N and P-channel  
Enhancement-mode Power MOSFETs**

- Low Gate Charge
- Low On-resistance
- Fast Switching Performance
- RoHS-compliant, halogen-free

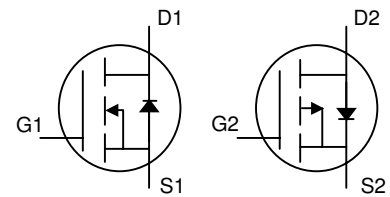


N-CH	$BV_{DSS}$	30V
	$R_{DS(ON)}$	72m $\Omega$
	$I_D$	3.3A
P-CH	$BV_{DSS}$	-30V
	$R_{DS(ON)}$	150m $\Omega$
	$I_D$	-2.3A

**Description**

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The AP2530GY-HF-3 is in a standard SOT-26 package, which is widely used for commercial and industrial surface-mount applications, and is well suited for applications such as small DC and servo motor drives.



**Absolute Maximum Ratings**

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$ at $T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	3.3	-2.3	A
$I_D$ at $T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	2.6	-1.8	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	10	-10	A
$P_D$ at $T_A=25^\circ\text{C}$	Total Power Dissipation	1.14		W
	Linear Derating Factor	0.01		W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

**Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	110	$^\circ\text{C}/\text{W}$

**Ordering Information**

**AP2530GY-HF-3TR** : in RoHS-compliant, halogen-free SOT-26, shipped on tape and reel (3000 pcs/reel)



**N-channel Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.02	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=3A$	-	-	72	m $\Omega$
		$V_{GS}=4.5V, I_D=2A$	-	-	125	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=3A$	-	4	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=30V, V_{GS}=0V$	-	-	1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=24V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=3A$	-	3	5	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=25V$	-	1	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	2	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=15V$	-	6	-	ns
$t_r$	Rise Time	$I_D=1A$	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	11	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	2	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	170	270	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	50	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	35	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	0.5	0.8	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=0.9A, V_{GS}=0V$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=3A, V_{GS}=0V$	-	14	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	7	-	nC

**Notes:**

1. Pulse width limited by maximum junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board,  $t \leq 10\text{sec}$ ;  $180^\circ\text{C}/\text{W}$  when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



**P-channel Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	-	0.03	-	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-2A$	-	-	150	m $\Omega$
		$V_{GS}=-4.5V, I_D=-1A$	-	-	280	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	-	2	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=-24V, V_{GS}=0V$	-	-	-25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=-2A$	-	3	5	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-25V$	-	1	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	2	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=-15V$	-	6	-	ns
$t_r$	Rise Time	$I_D=-1A$	-	8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-5V$	-	17	-	ns
$t_f$	Fall Time	$R_D=15\Omega$	-	4	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	150	240	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-25V$	-	50	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	40	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	8	12	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=-0.9A, V_{GS}=0V$	-	-	-1.3	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=2A, V_{GS}=0V,$	-	15	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	7	-	nC

**Notes:**

1. Pulse width limited by maximum junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board,  $t \leq 10\text{sec}$ ; 180 $^\circ\text{C}/\text{W}$  when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Typical N-channel Electrical Characteristics

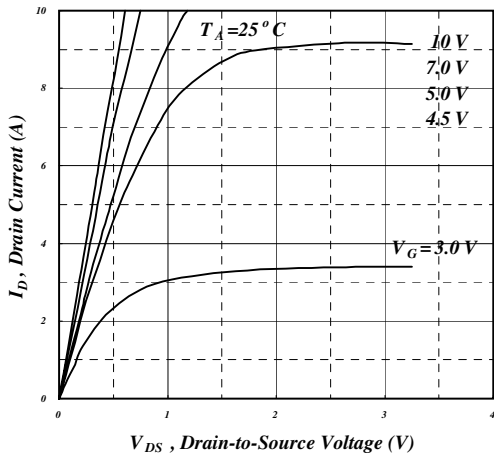


Fig 1. Typical Output Characteristics

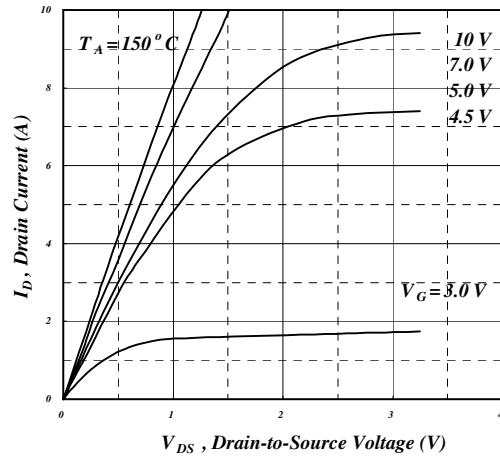


Fig 2. Typical Output Characteristics

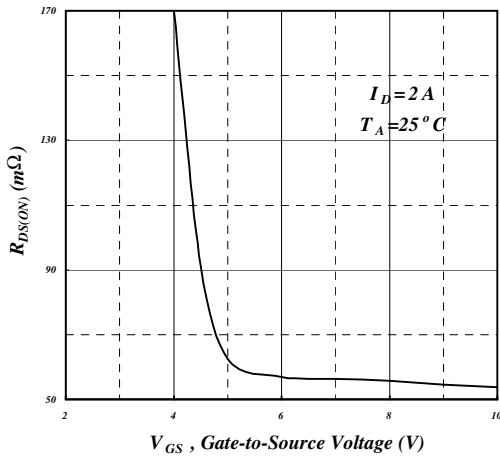


Fig 3. On-Resistance vs. Gate Voltage

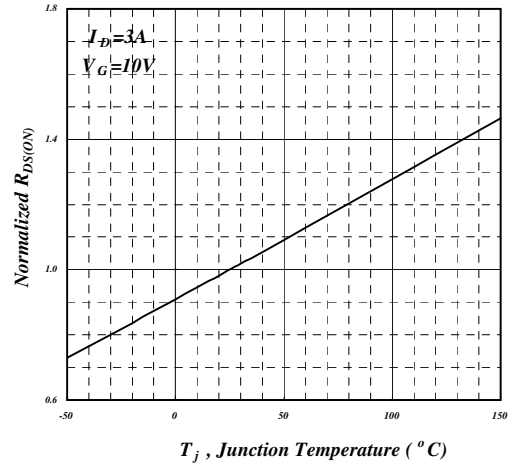


Fig 4. Normalized On-Resistance vs. Junction Temperature

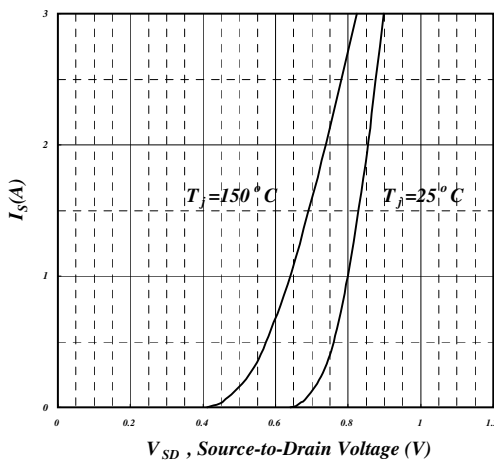


Fig 5. Forward Characteristic of Reverse Diode

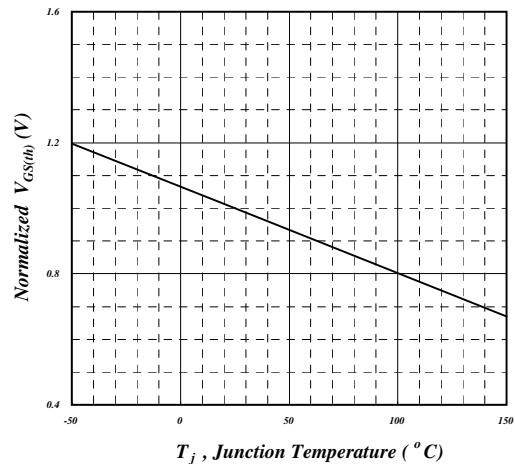


Fig 6. Gate Threshold Voltage vs. Junction Temperature



## Typical N-channel Electrical Characteristics (cont.)

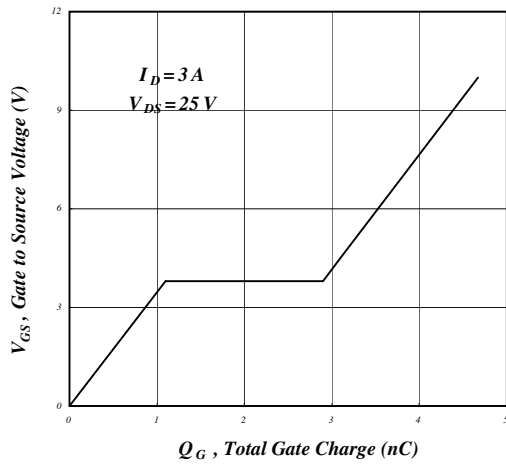


Fig 7. Gate Charge Characteristics

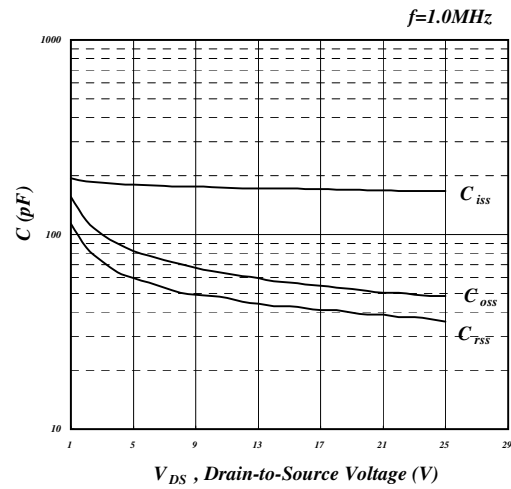


Fig 8. Typical Capacitance Characteristics

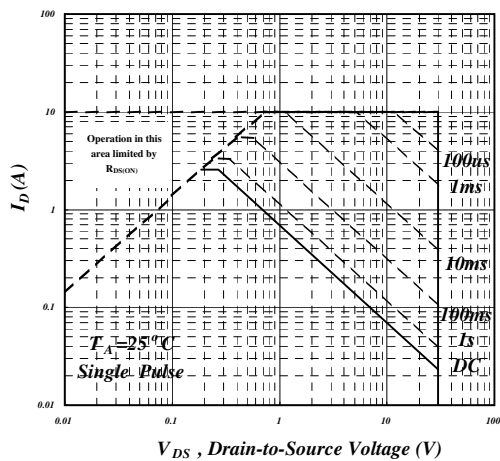


Fig 9. Maximum Safe Operating Area

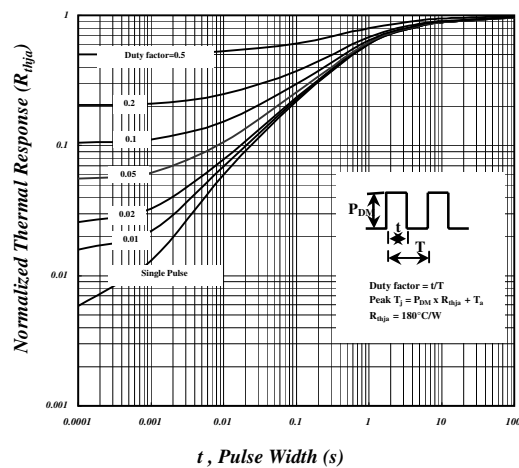


Fig 10. Effective Transient Thermal Impedance

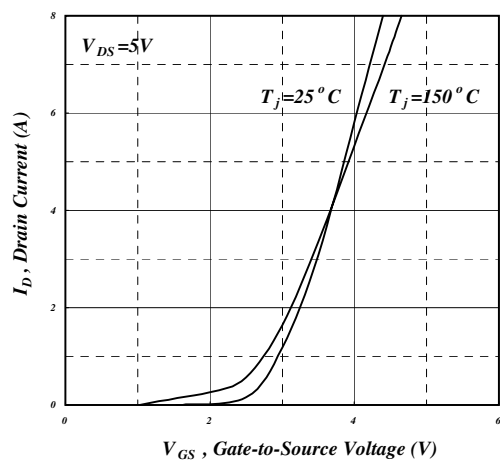


Fig 11. Transfer Characteristics

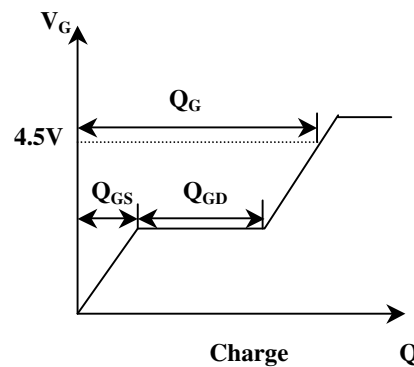


Fig 12. Gate Charge Waveform



Typical P-channel Electrical Characteristics

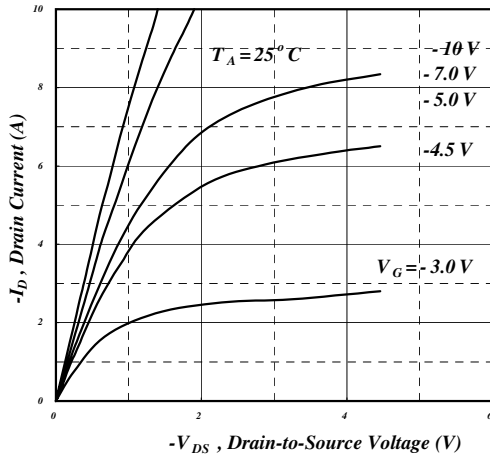


Fig 1. Typical Output Characteristics

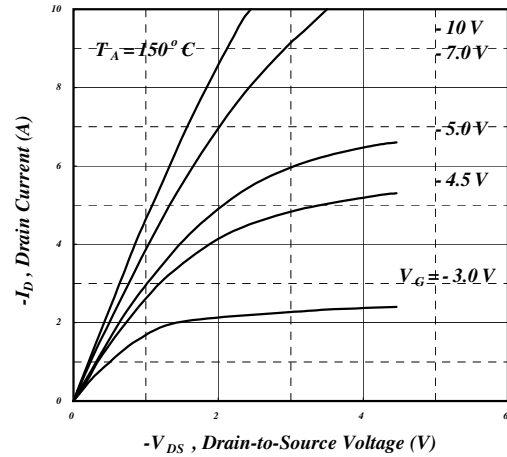


Fig 2. Typical Output Characteristics

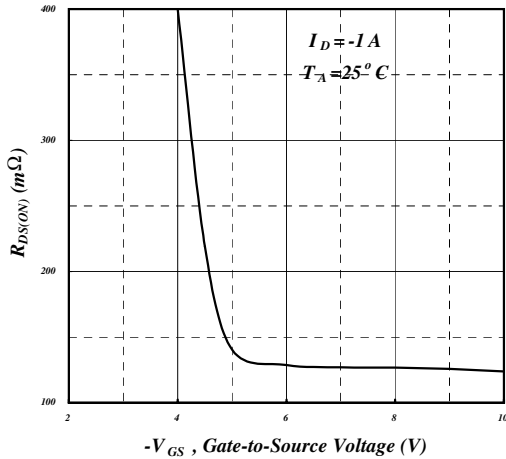


Fig 3. On-Resistance vs. Gate Voltage

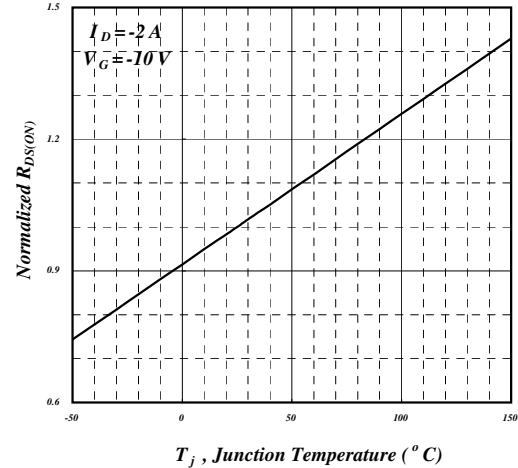


Fig 4. Normalized On-Resistance vs. Junction Temperature

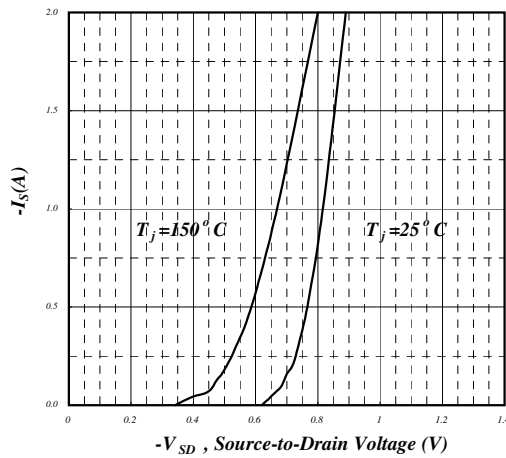


Fig 5. Forward Characteristic of Reverse Diode

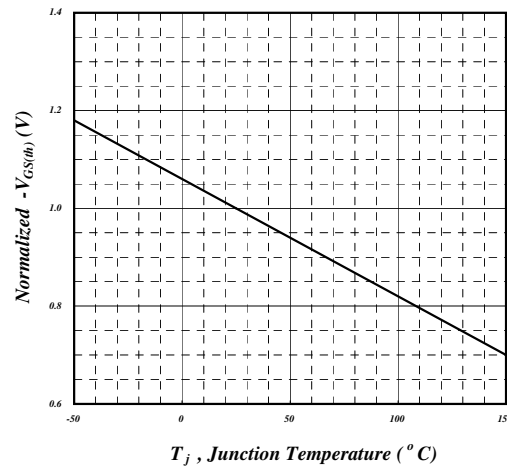


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical P-channel Electrical Characteristics (cont.)

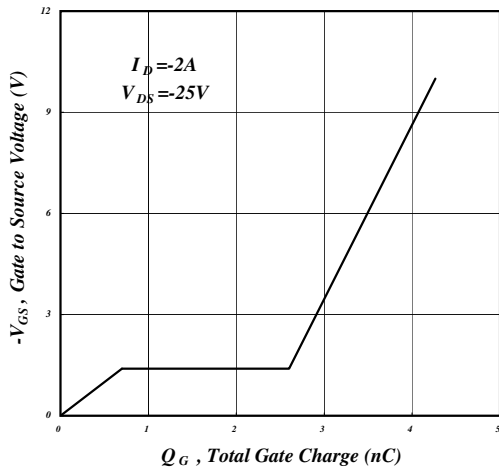


Fig 7. Gate Charge Characteristics

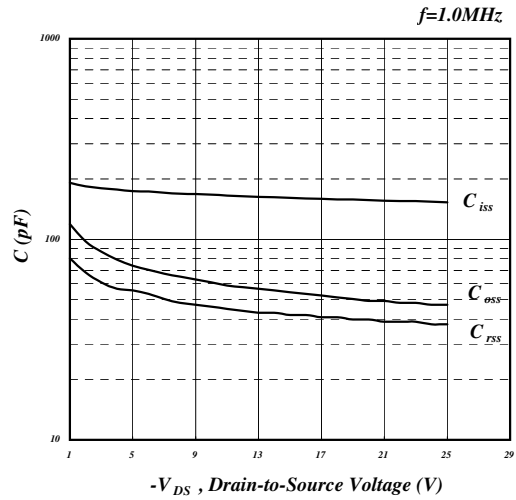


Fig 8. Typical Capacitance Characteristics

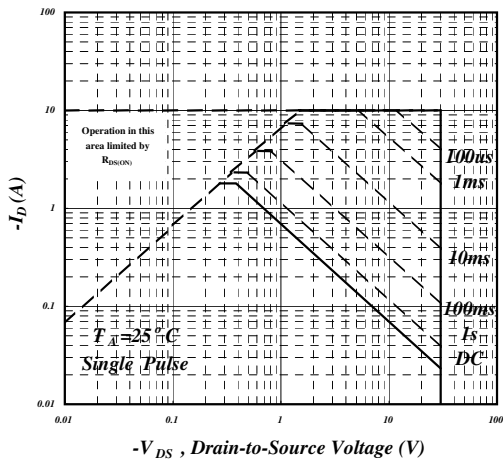


Fig 9. Maximum Safe Operating Area

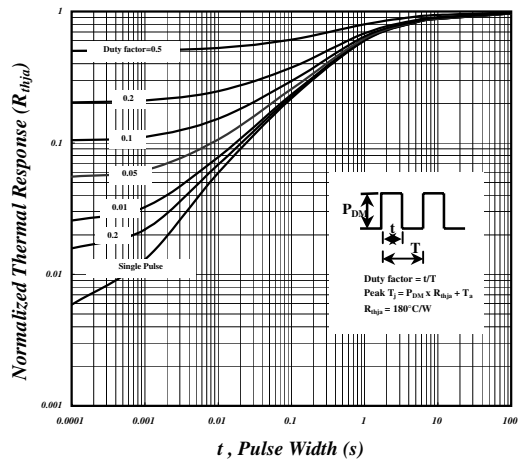


Fig 10. Effective Transient Thermal Impedance

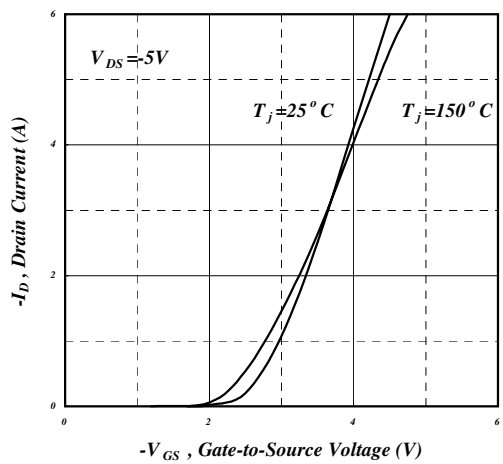


Fig 11. Transfer Characteristics

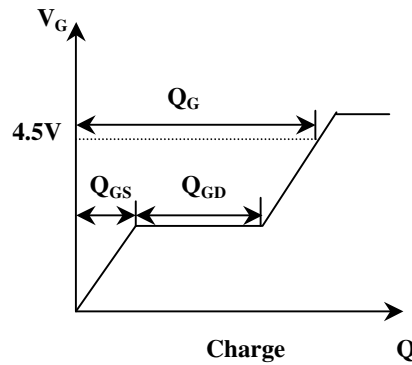
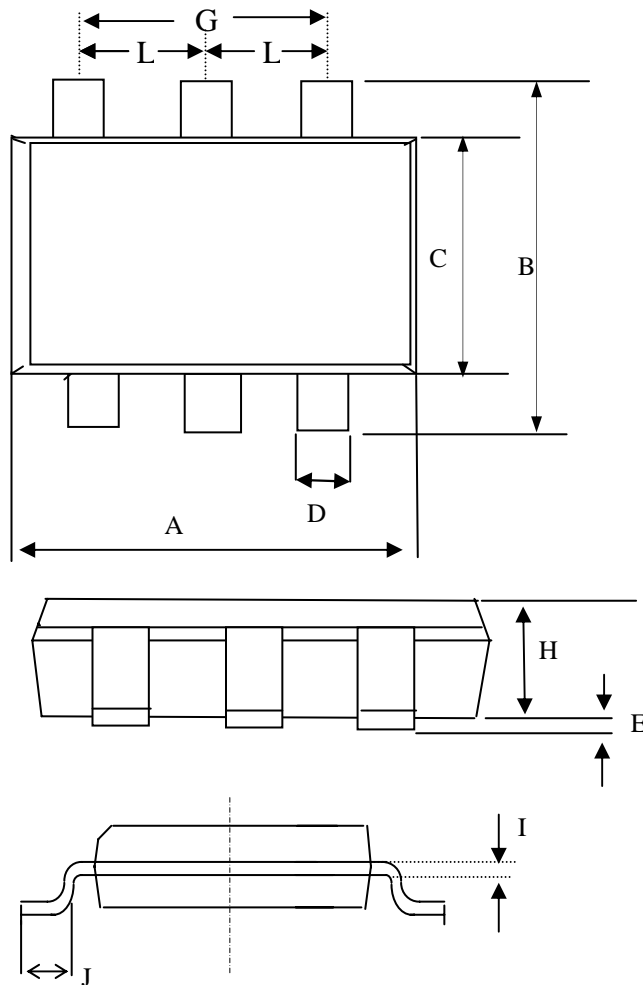


Fig 12. Gate Charge Waveform



Package Dimensions: SOT-26

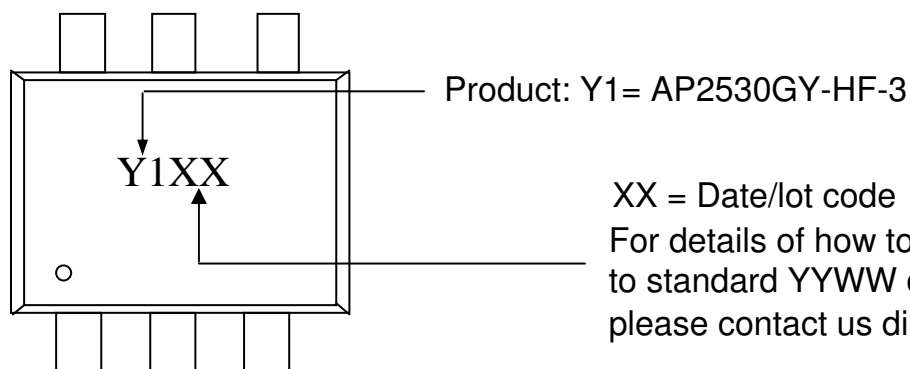


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	2.70	2.90	3.10
B	2.60	2.80	3.00
C	1.40	1.60	1.80
D	0.30	0.43	0.55
E	0.00	0.05	0.10
H	1.20REF		
G	1.90REF		
I	0.12REF		
J	0.37REF		
L	0.95REF		

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information: SOT-26

Laser Marking



XX = Date/lot code  
 For details of how to convert this to standard YYWW date code format, please contact us directly.