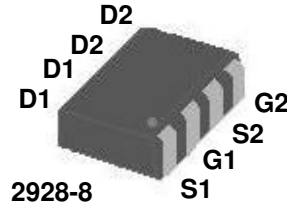




**Complementary N and P-channel
Enhancement-mode Power MOSFETs**

- Simple Drive, from 2.5V
- Low On-resistance
- Fast Switching Performance
- RoHS-compliant, halogen-free

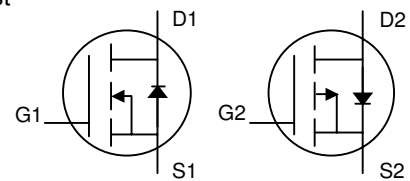


N-CH	BV_{DSS}	20V
	$R_{DS(ON)}$	37m Ω
	I_D	5A
P-CH	BV_{DSS}	-20V
	$R_{DS(ON)}$	75m Ω
	I_D	-3.7A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, low on-resistance and cost-effectiveness.

The AP2451GY-HF-3 is in a 2928-8 J-lead package, which is used in commercial and industrial surface-mount applications where it offers improved on-resistance and thermal performance when compared with similar-sized traditional packages like the SOT-26.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
I_D at $T_A=25^\circ\text{C}$	Continuous Drain Current ³	5	-3.7	A
I_D at $T_A=70^\circ\text{C}$	Continuous Drain Current ³	4	-3	A
I_{DM}	Pulsed Drain Current ¹	20	-20	A
P_D at $T_A=25^\circ\text{C}$	Total Power Dissipation	1.38		W
	Linear Derating Factor	0.011		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	90	$^\circ\text{C}/\text{W}$

Ordering Information

AP2451GY-HF-3TR : in RoHS-compliant, halogen-free 2928-8, shipped on tape and reel (3000pcs/reel)



N-channel Electrical Specifications at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.02	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6A$	-	-	32	mW
		$V_{GS}=4.5V, I_D=5A$	-	-	37	$m\Omega$
		$V_{GS}=2.5V, I_D=3A$	-	-	55	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	-	1.2	V
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=5A$	-	13	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=16V, V_{GS}=0V$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=5A$	-	9	15	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=16V$	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=10V$	-	9	-	ns
t_r	Rise Time	$I_D=1A$	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	16	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	5	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	620	990	pF
C_{oss}	Output Capacitance	$V_{DS}=20V$	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	100	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.2	1.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1.2A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_S=5A, V_{GS}=0V$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	11	-	nC

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 155°C/W at steady state.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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P-channel Electrical Specifications at $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=-1\text{mA}$	-	0.01	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-4A$	-	-	57	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	-	-	75	$\text{m}\Omega$
		$V_{GS}=-2.5V, I_D=-1A$	-	-	105	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-	-1.2	V
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	-	10	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=-16V, V_{GS}=0V$	-	-	-10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-3A$	-	11	18	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-16V$	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-10V$	-	10	-	ns
t_r	Rise Time	$I_D=-1A$	-	16	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=-5V$	-	26	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	16	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	740	1180	pF
C_{oss}	Output Capacitance	$V_{DS}=-20V$	-	160	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	130	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	6.6	10	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage ²	$I_S=-1.2A, V_{GS}=0V$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	$I_S=3A, V_{GS}=0V,$	-	29	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	20	-	nC

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; $155^\circ\text{C}/\text{W}$ at steady state.

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Typical N-channel Electrical Characteristics

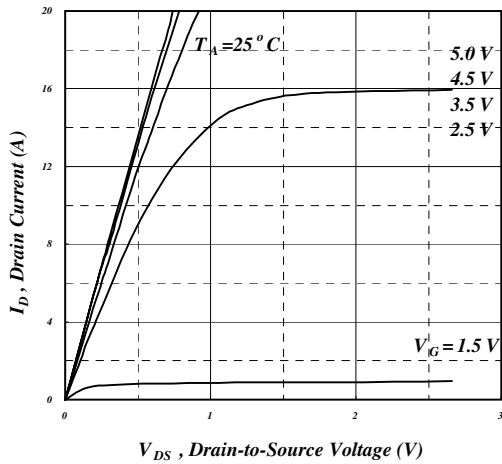


Fig 1. Typical Output Characteristics

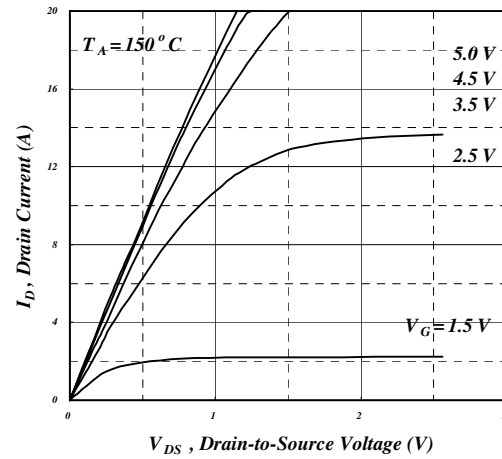


Fig 2. Typical Output Characteristics

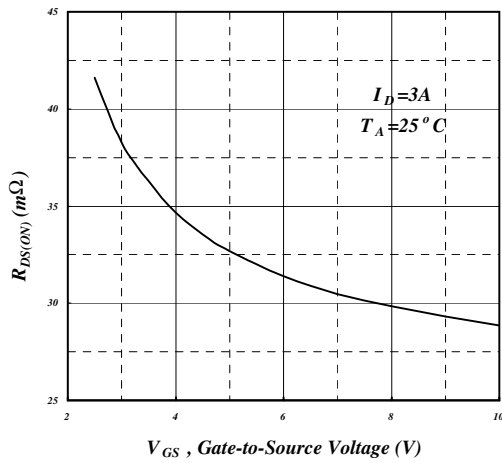


Fig 3. On-Resistance vs. Gate Voltage

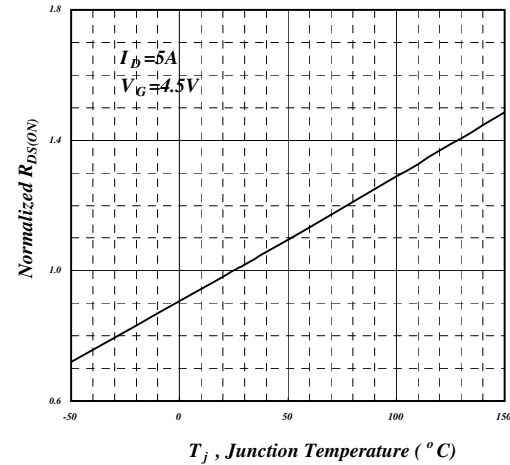


Fig 4. Normalized On-Resistance vs. Junction Temperature

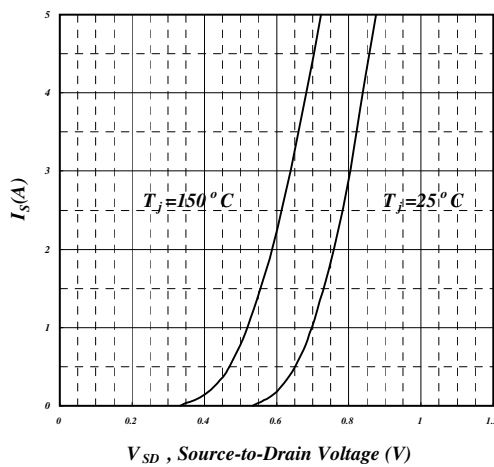


Fig 5. Forward Characteristic of Reverse Diode

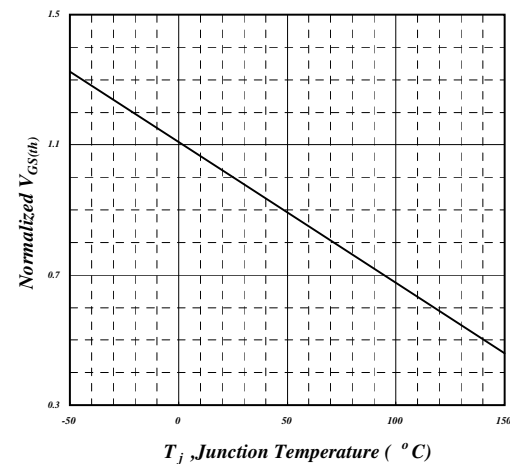


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical N-channel Electrical Characteristics (cont.)

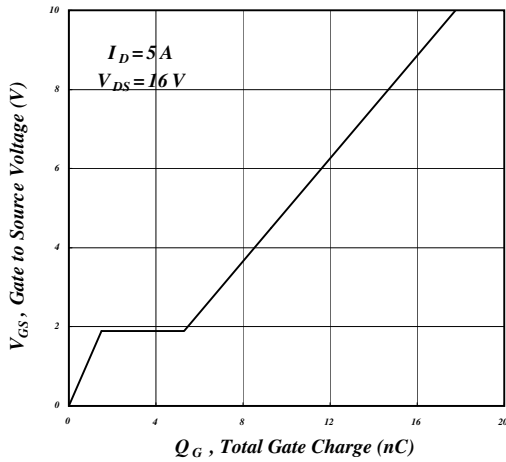


Fig 7. Gate Charge Characteristics

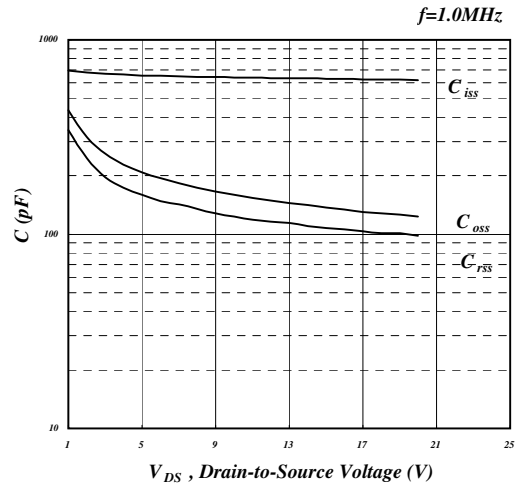


Fig 8. Typical Capacitance Characteristics

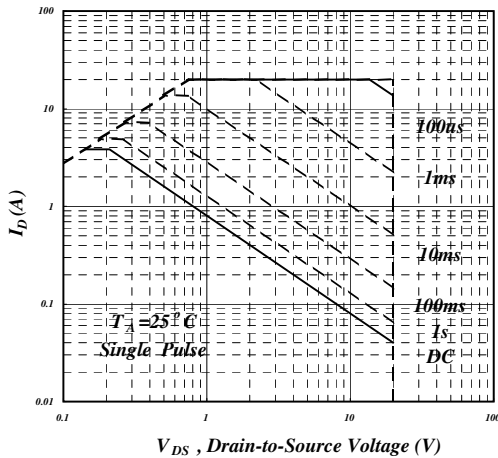


Fig 9. Maximum Safe Operating Area

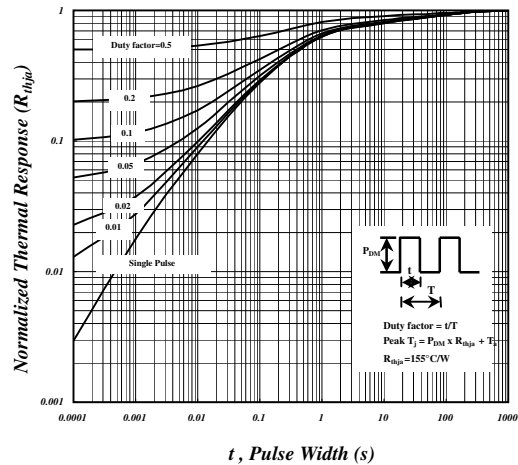


Fig 10. Effective Transient Thermal Impedance

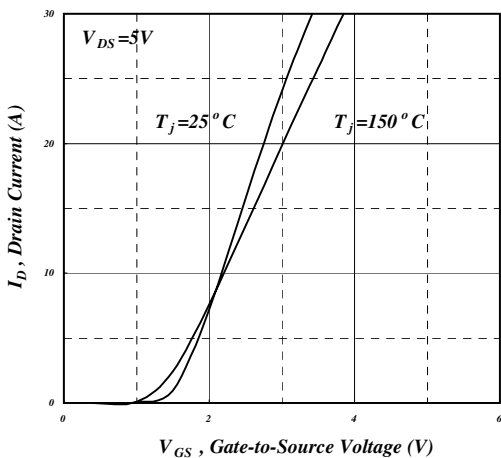


Fig 11. Transfer Characteristics

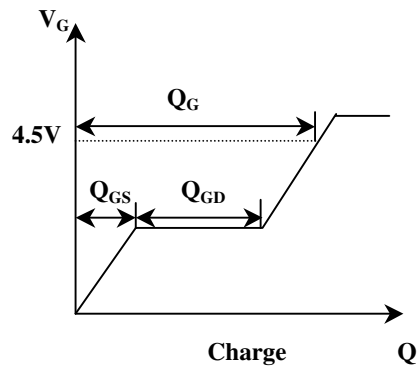


Fig 12. Gate Charge Waveform



Typical P-channel Electrical Characteristics

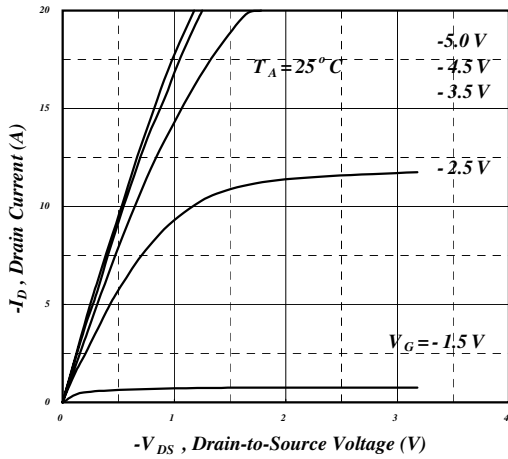


Fig 1. Typical Output Characteristics

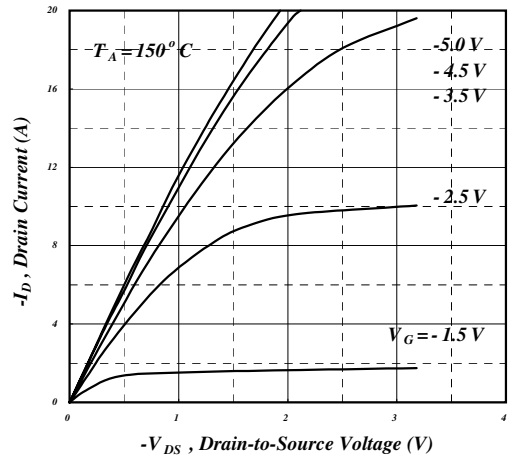


Fig 2. Typical Output Characteristics

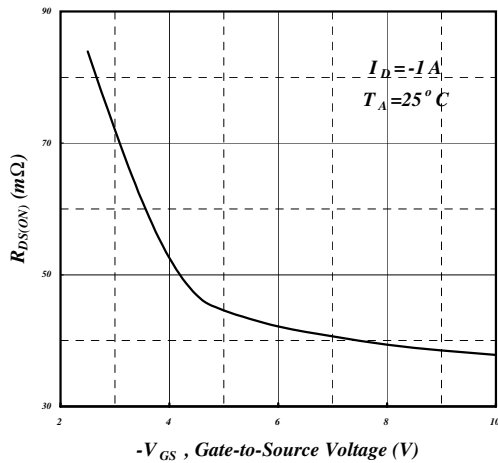


Fig 3. On-Resistance vs. Gate Voltage

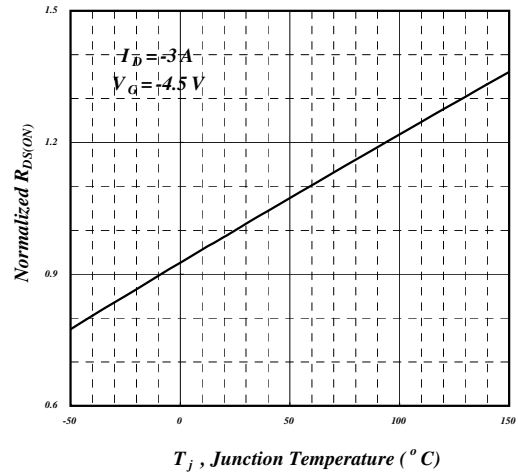


Fig 4. Normalized On-Resistance vs. Junction Temperature

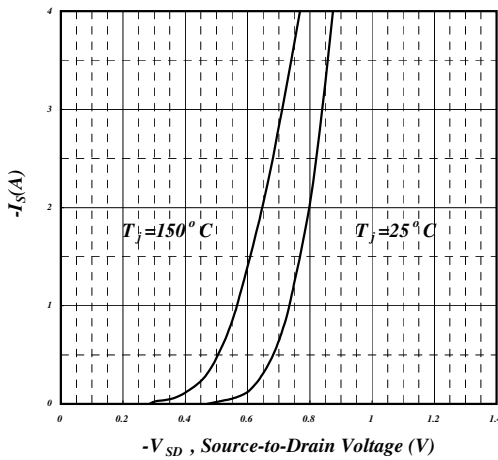


Fig 5. Forward Characteristic of Reverse Diode

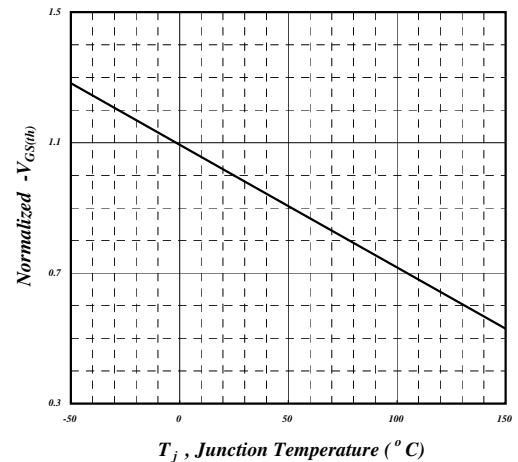


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical P-channel Electrical Characteristics (cont.)

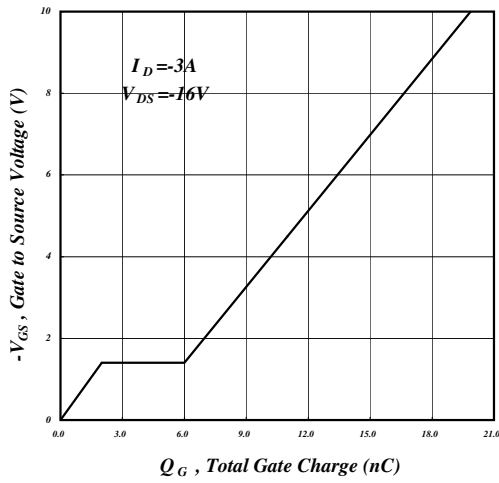


Fig 7. Gate Charge Characteristics

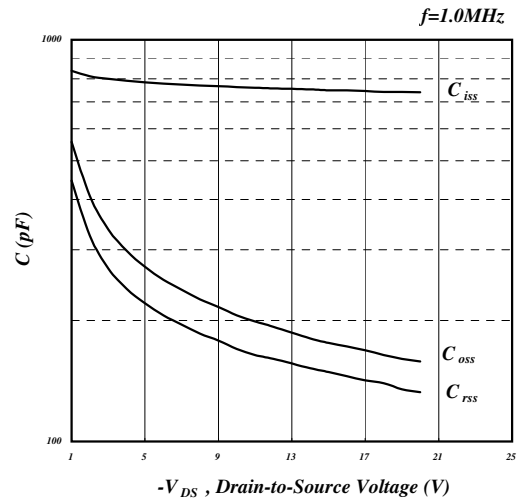


Fig 8. Typical Capacitance Characteristics

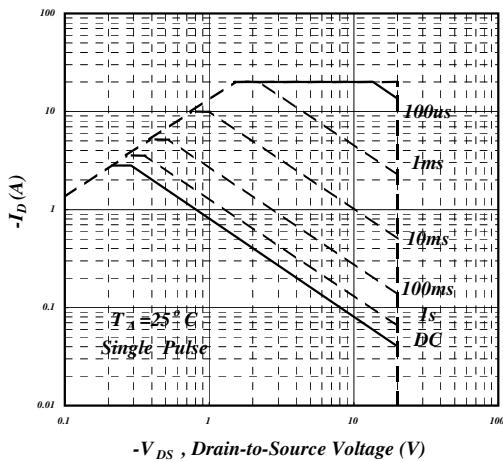


Fig 9. Maximum Safe Operating Area

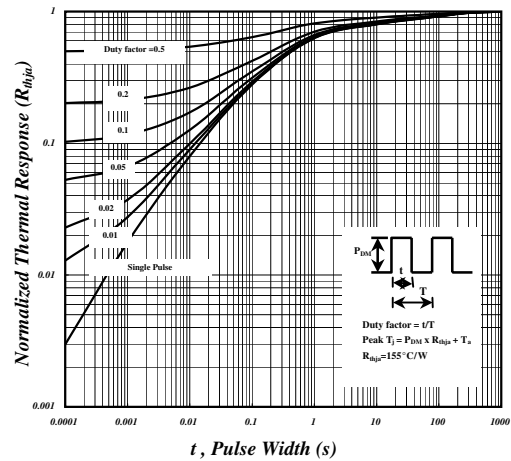


Fig 10. Effective Transient Thermal Impedance

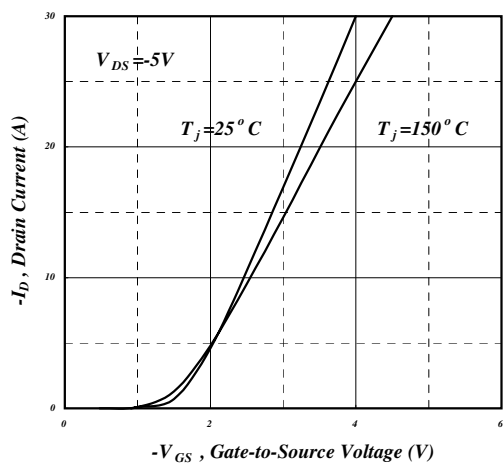


Fig 11. Transfer Characteristics

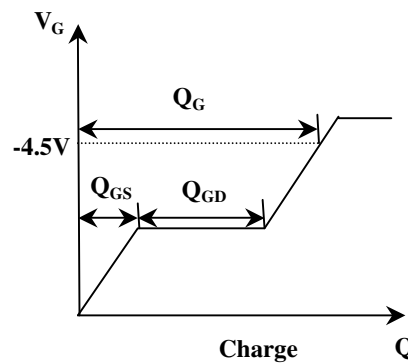
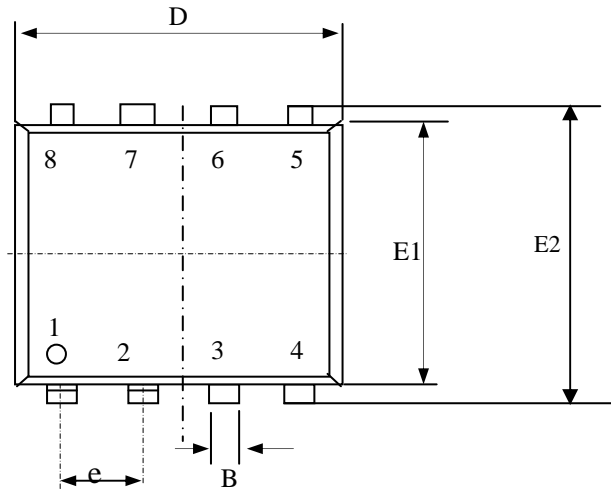


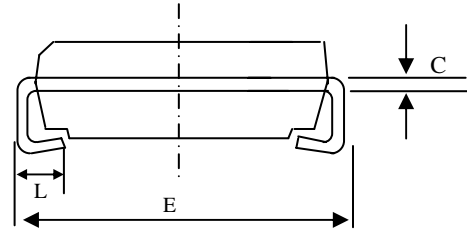
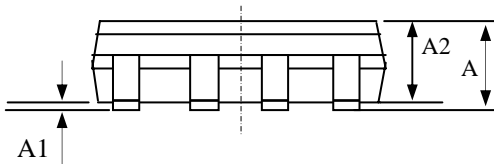
Fig 12. Gate Charge Waveform



Package Dimensions: 2928-8 J-lead



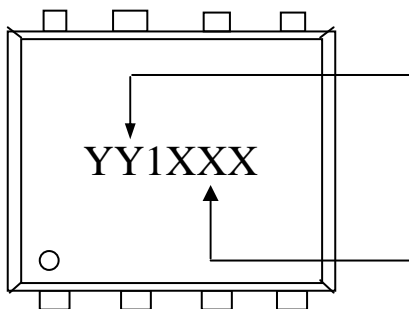
SYMBOLS	Millimeters		
	MIN	NOM	MAX
E	2.50	----	3.00
E1	2.30	2.40	2.50
E2	2.65	2.85	3.05
L	0.30	0.45	0.60
A	0.93	---	1.10
A1	0.01	---	0.10
A2	0.92	---	1.00
D	2.95	3.05	3.10
B	0.25	0.32	0.40
C	0.10	0.15	0.20
e	0.65BSC		



- Note: 1. All dimensions are in millimeters.
 2. Package body size excludes mold flash, protrusions or gate burrs.
 Mold flash, protrusions or gate burrs shall not exceed 0.10mm per side.
 3. Package body size is determined at the outermost extremes of the plastic body, exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
 4. The package top may be smaller than the package bottom.
 5. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the lead width dimension "B" at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Marking Information

Laser Marking



XXX = Date/lot code
 For details of how to convert this to standard YYWW date code format, please contact us directly.