



1.5/3A Sink/Source Bus Termination Regulator

Features

- Ideal for DDR-I and DDR-II Applications
- Sink 1.5A and Source 3A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SCSI-3 Interfaces.
- Highly Accurate Output Voltage at Full-Load
- Output Adjustment using Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Current-shoot-through protection
- Standard SO-8, or TO-252-5L Packages
- RoHS-compliant, Halogen-free

Application

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses in DDR-I, DDR-II and SCSI-III Systems

Description

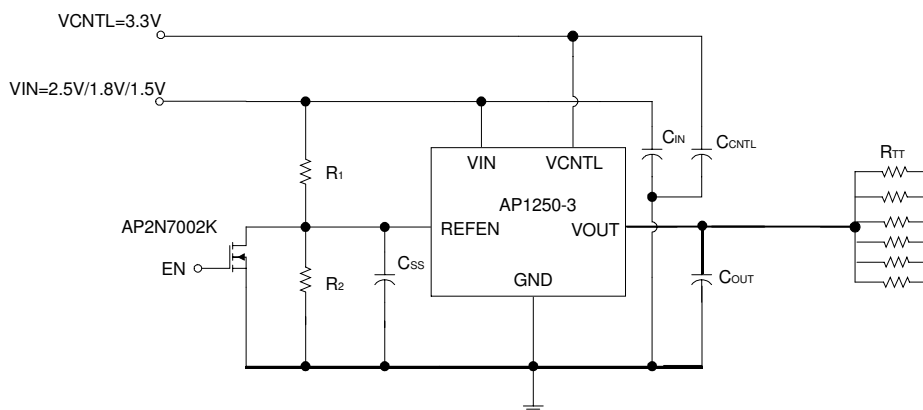
The AP1250-HF-3 is a simple and cost-effective high-speed linear regulator designed to generate termination voltages in double data rate (DDR) memory systems to comply with JEDEC SSTL_2 and SSTL_18, or other specific interfaces such as HSTL, SCSI-2 and SCSI-3.

The regulator is capable of actively sinking 1.5A and sourcing up to 3A while regulating an output voltage to within 40mV. The output termination voltage can be tightly regulated to track 1/2V_{DDQ} by using two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The AP1250-HF-3 also incorporates a high-speed differential amplifier to provide ultra-fast response to line/load transients. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in both directions and on-chip thermal shut-down protection.

The AP1250-HF-3 is available in either a standard SO-8 surface-mount package, or the TO-252-5L with exposed pad/tab for heatsinking.

Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$

Minimum $C_{OUT} = 10\mu F$ (Ceramic) + 100 μF under the worst case testing condition

$C_{SS} = 1\mu F$, $C_{IN} = 470\mu F$ (low ESR), $C_{CNTL} = 47\mu F$



Absolute Maximum Ratings (Note 1)

Input Voltage (V_{IN})	-----	6V
CNTL Pin Voltage (V_{CNTL})	-----	6V
Power Dissipation (P_D)	-----	Internally Limited
Storage Temperature Range (T_{ST})	-----	-55 to +150 °C
Lead Temperature (Soldering, 10sec.)	-----	260 °C
Thermal Resistance from Junction to Case (R_{thjc}) (Note 2)		
	SO-8	20 °C/W
	TO-252-5L	6 °C/W

Note 1 : Exceeding the absolute maximum rating may damage the device.

Note 2 : Surface-mounted on 1in² copper pad of FR4 board.

Ordering Information

AP1250GX-HF-3TR

Package:

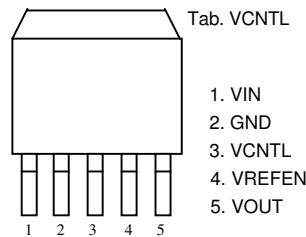
H : TO-252-5L

M : SO-8

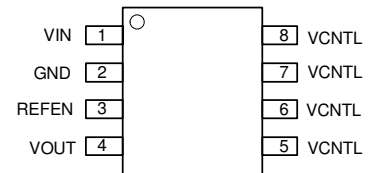
Shipped on tape and reel, 3000pcs/reel

Pin Configuration

TO-252-5L (Top View)



SO-8 (Top View)



Electrical Specifications at $T_A=25^\circ\text{C}$ (unless otherwise specified)

$V_{IN} = +2.5\text{V}$, $V_{CNTL} = +3.3\text{V}$, $V_{REFEN} = +1.25\text{V}$, $C_{OUT} = 10\mu\text{F}$ (Ceramic)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OS}	Output Offset Voltage ¹	$I_{OUT} = 0\text{A}$	-20	-5	20	mV
$ \Delta V_{LOAD} $	Load Regulation	$I_L : 0 \rightarrow 1.5\text{A}$	--	0.5	2	%
		$I_L : 1.5 \rightarrow 3\text{A}$	--	2	3	%
V_{IN}	Input Voltage Range(DDR I/II) ²	$V_{CNTL} \geq V_{IN}$	1.6	2.5/1.8	--	V
V_{CNTL}	Gate Drive Voltage Range ²	$V_{CNTL} \geq V_{IN}$	--	3.3	6	V
I_{SHDN}	Current in Shutdown	$V_{REFEN} < 0.2\text{V}, R_L = 180\Omega$	--	10	90	μA
Short Circuit Protection						
I_{LIMIT}	Current Limit	AP1250GM	--	2	--	A
		AP1250GH	--	3	--	A
I_q	Quiescent Current	$I_{OUT} = 0\text{A}$	--	1	3	mA
Over Temperature Protection						
T_{OS}	Thermal Shutdown Temperature	$3.3\text{V} < V_{CNTL} < 5\text{V}$	--	40	--	°C
Shutdown Function						
	Shutdown Threshold Trigger	Output = High	0.8	--	--	V
	Shutdown Threshold Trigger	Output = Low	--	--	0.2	V

Notes:

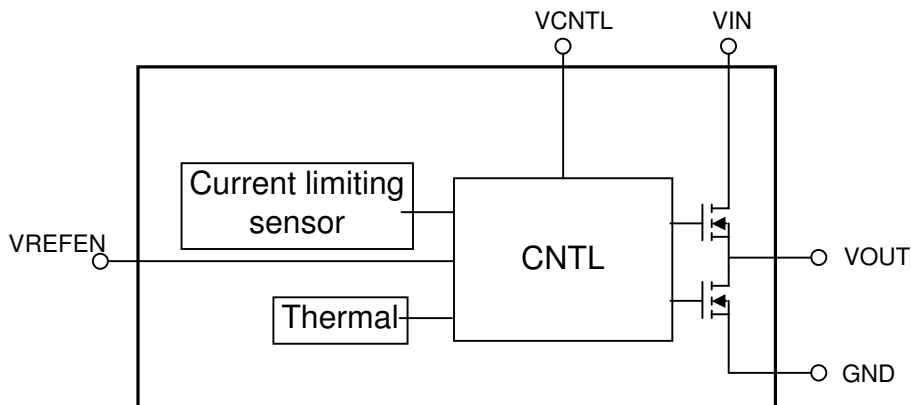
- V_{OS} is the voltage measurement V_{OUT} subtracted from V_{REFEN} .
- Keep $V_{CNTL} \geq V_{IN}$ at power on/off sequences.
- Surface mounted on 1 in² copper pad of FR4 board



Pin Descriptions

PIN SYMBOL	PIN DESCRIPTION
V_{IN}	Power Input Voltage.
GND	Ground Pin
V_{OUT}	Output Voltage
V_{CNTL}	Gate Drive Voltage
VREFEN	Reference Voltage Input and Chip Enable

Block Diagram



THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



Typical Performance Characteristics

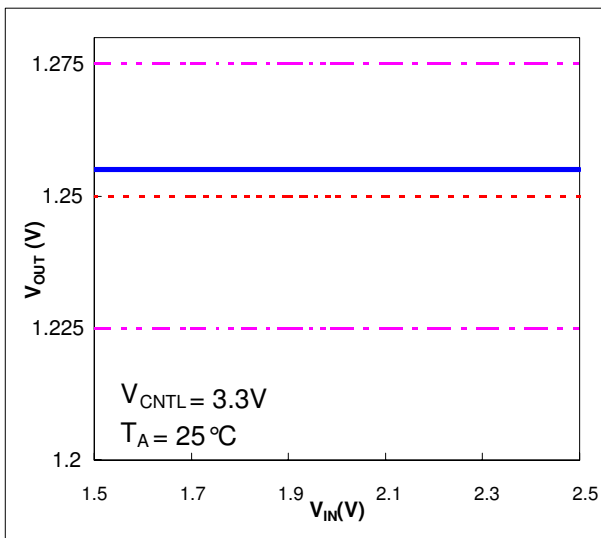


Fig 1. Line Regulation(V_{OUT} vs. V_{IN})

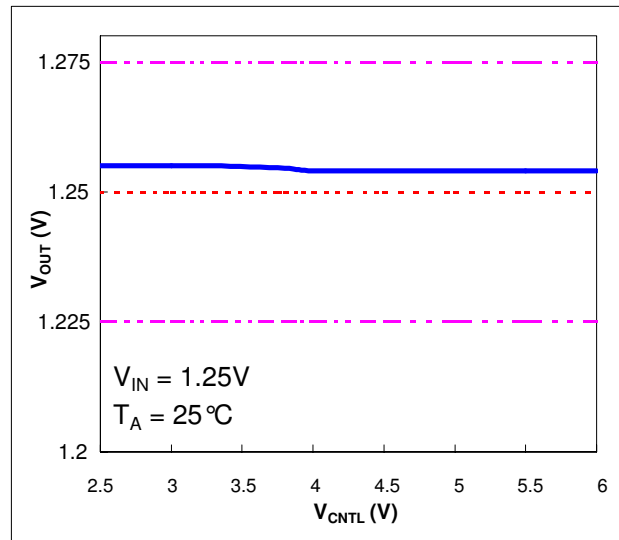


Fig 2. Line Regulation(V_{OUT} vs. V_{CNTL})

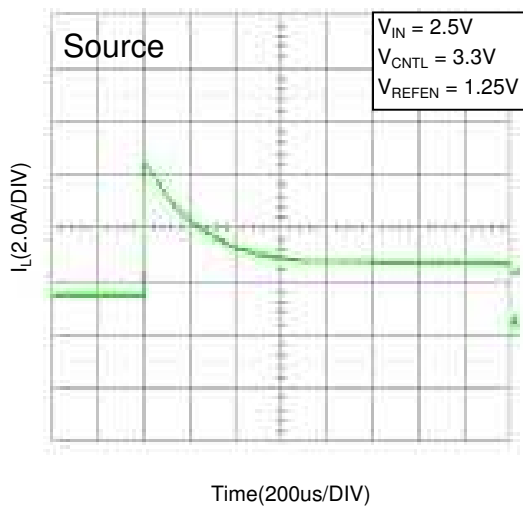


Fig 3. Output Short-Circuit Protection

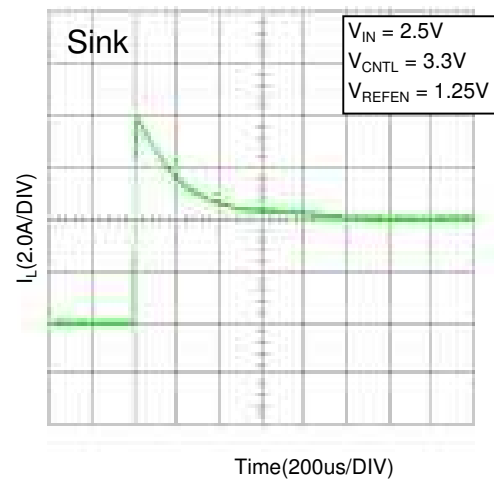


Fig 4. Output Short-Circuit Protection



Typical Performance Characteristics (continued)

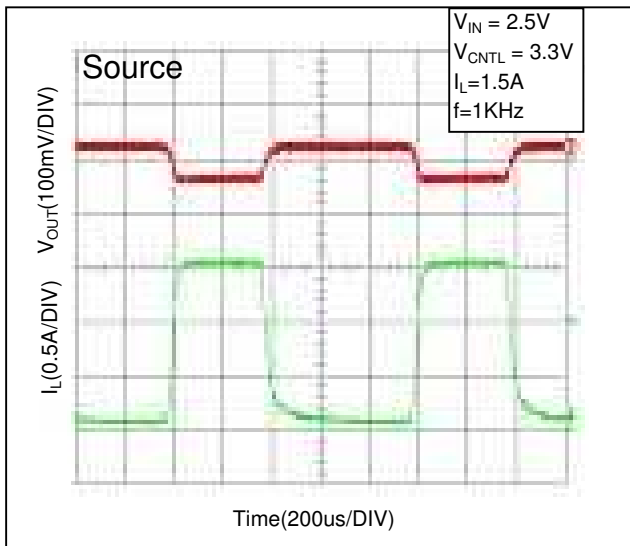


Fig 5. Transient Response

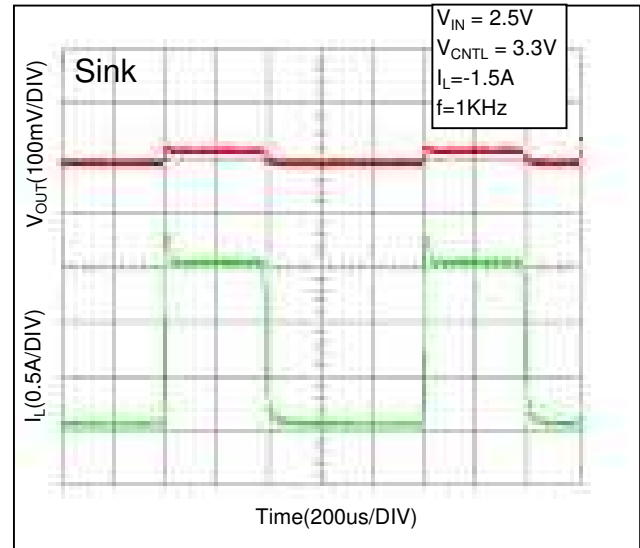


Fig 6. Transient Response

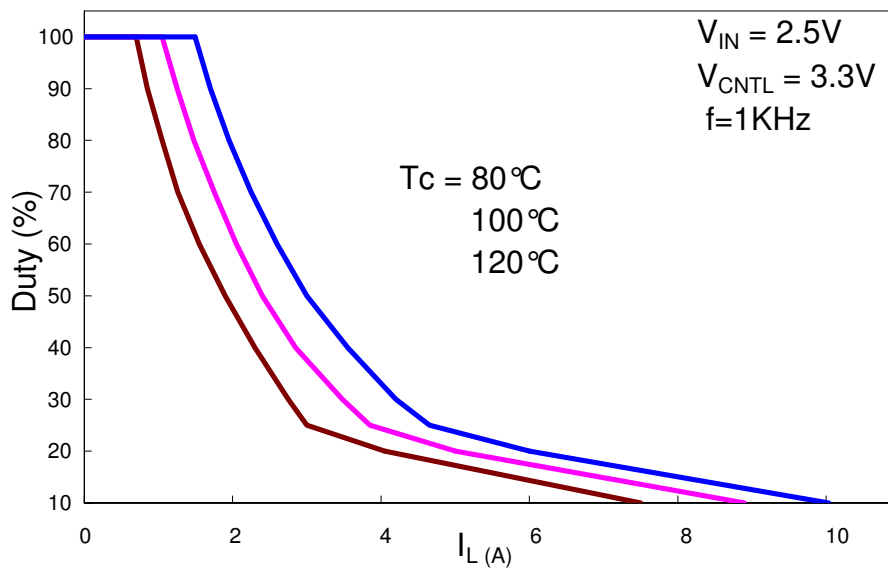
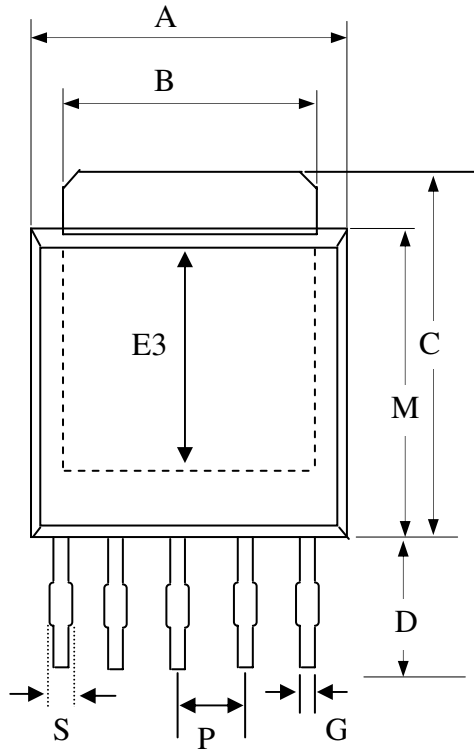


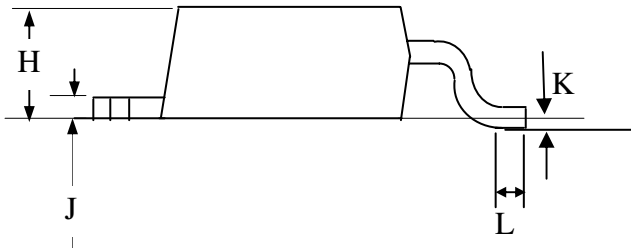
Fig 7. Safe Operating Area



Package Dimensions: SO-8

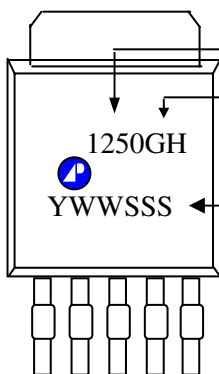


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	6.40	6.6	6.80
B	5.2	5.35	5.50
C	6.80	7.00	7.20
D	2.20	2.50	2.80
P	1.27 REF.		
S	0.50	0.65	0.80
E3	3.50	4.00	4.50
G	0.40	0.50	0.60
H	2.20	2.30	2.40
J	0.45	0.50	0.55
K	0.00	0.075	0.15
L	0.90	1.20	1.50
M	5.40	5.60	5.80



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

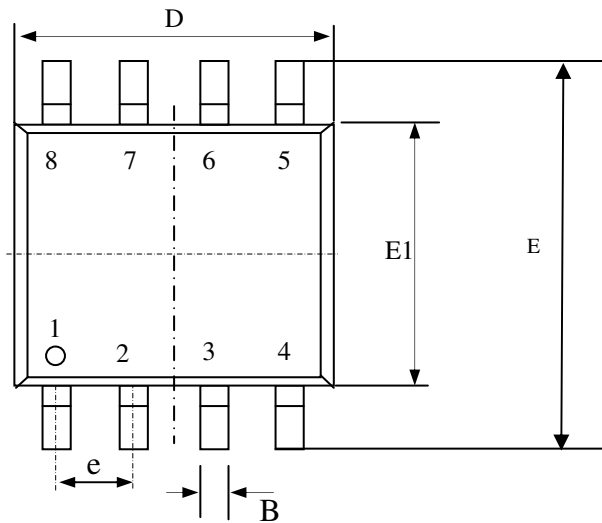
Marking Information:



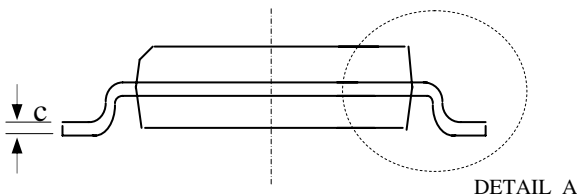
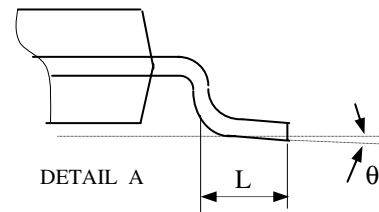
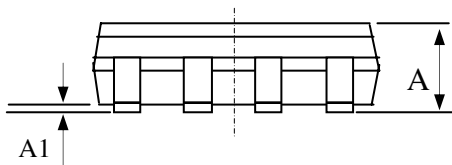
Product: AP1250
 Package: GH = RoHS-compliant halogen-free TO-252-5L
 Date/lot code (YWWSSS)
 Y: Last digit of the year
 WW: Work week
 SSS: Lot code sequence



Package Dimensions: SO-8

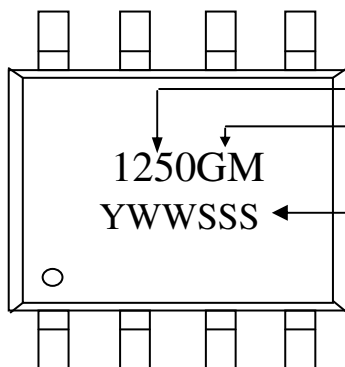


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
E	5.80	6.15	6.50
L	0.38	0.71	1.27
θ	0	4.00	8.00
e	1.27 TYP		



1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

Marking Information:



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