



**N-channel Enhancement-mode Power MOSFET**

- Simple Drive Requirement**
- SO-8 Compatible with Heatsink**
- Low On-resistance**
- RoHS-compliant, halogen-free**

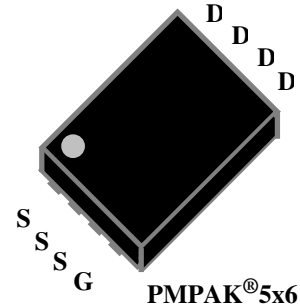


$BV_{DSS}$	40V
$R_{DS(ON)}$	9.5mΩ
$I_D$	46A

**Description**

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The PMPAK<sup>®</sup>5x6 package is specially designed for DC-DC converter applications, with a foot print that is compatible with the popular SO-8 and offers a backside heat sink and lower package profile.



**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	±20	V
$I_D$ at $T_C=25^\circ C$	Continuous Drain Current (Chip)	46	A
$I_D$ at $T_A=25^\circ C$	Continuous Drain Current <sup>3</sup>	17.5	A
$I_D$ at $T_A=70^\circ C$	Continuous Drain Current <sup>3</sup>	14	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	160	A
$P_D$ at $T_C=25^\circ C$	Total Power Dissipation	34.7	W
$P_D$ at $T_A=25^\circ C$	Total Power Dissipation	5	W
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	28.8	mJ
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	3.6	°C/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	25	°C/W

**Ordering Information**

**AP0904GMT-HF-3TR**

**RoHS-compliant halogen-free PMPAK<sup>®</sup>5x6, shipped on tape and reel (3000pcs/reel)**

PMPAK<sup>®</sup> is a registered trademark of Advanced Power Electronics Corp.



**Electrical Specifications at  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=30A$	-	-	9.5	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	-	15	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=20A$	-	45	-	S
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=40V, V_{GS}=0V$	-	-	10	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=20A$	-	9	14.4	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=20V$	-	2	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	6	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=20V$	-	6.5	-	ns
$t_r$	Rise Time	$I_D=1A$	-	6.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	20	-	ns
$t_f$	Fall Time	$R_D=20\Omega$	-	10	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	680	1080	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	160	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	95	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=20A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=10A, V_{GS}=0V,$	-	31	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	29	-	nC

**Notes:**

1. Pulse width limited by maximum junction temperature
2. Pulse test
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board,  $t \leq 10\text{sec}$ ,  $60^\circ\text{C/W}$  at steady state.
4. Starting  $T_j=25^\circ\text{C}$ ,  $V_{DD}=30V$ ,  $L=0.1\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=24A$ .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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Typical Electrical Characteristics

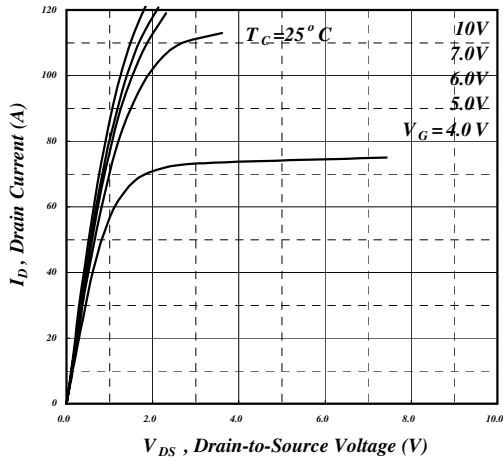


Fig 1. Typical Output Characteristics

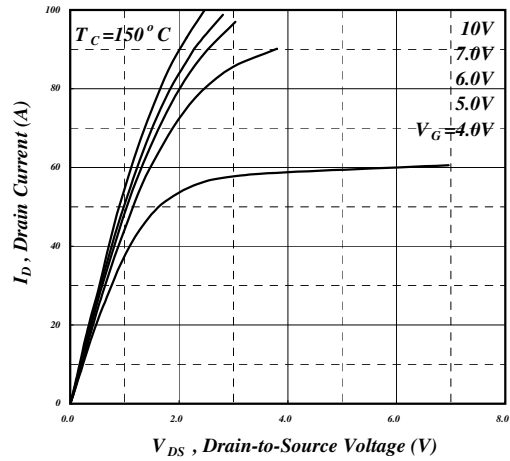


Fig 2. Typical Output Characteristics

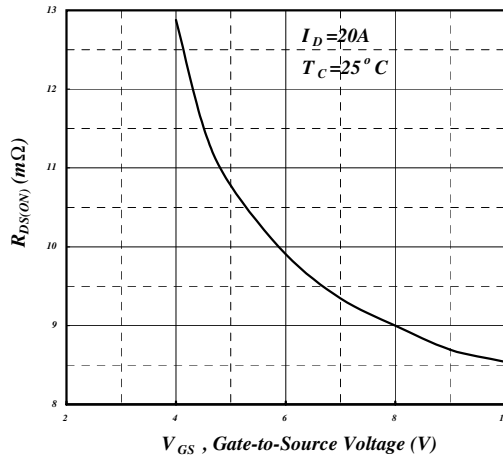


Fig 3. On-Resistance vs. Gate Voltage

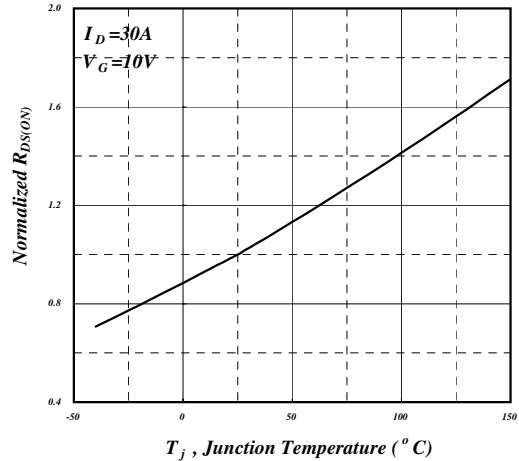


Fig 4. Normalized On-Resistance vs. Junction Temperature

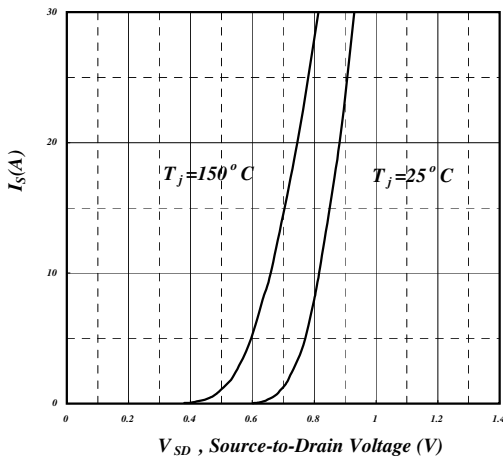


Fig 5. Forward Characteristic of Reverse Diode

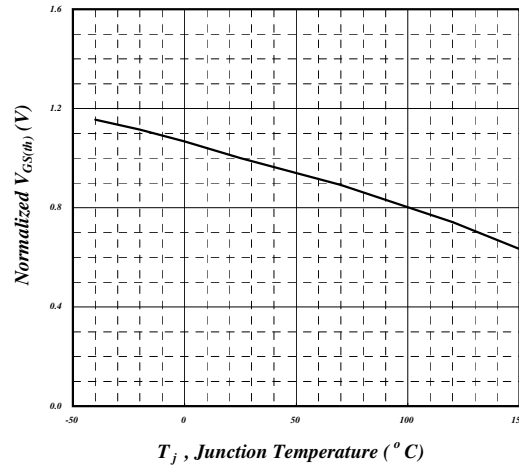


Fig 6. Gate Threshold Voltage vs. Junction Temperature



Typical Electrical Characteristics (cont.)

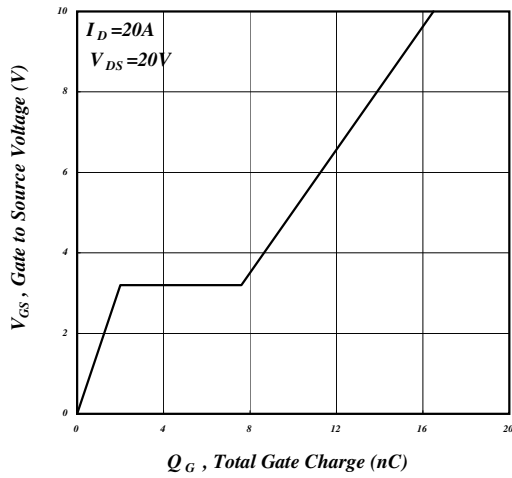


Fig 7. Gate Charge Characteristics

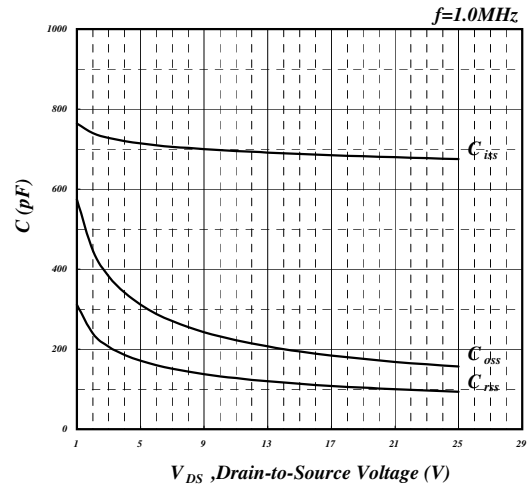


Fig 8. Typical Capacitance Characteristics

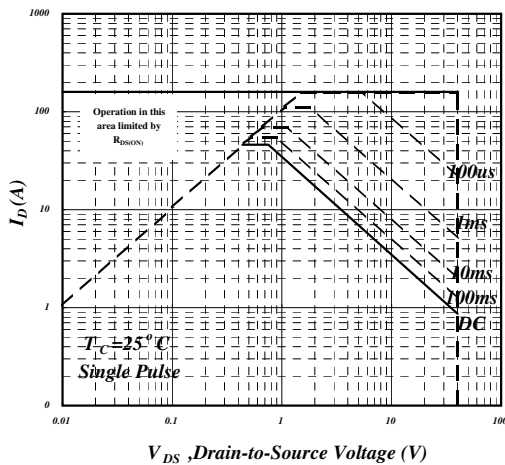


Fig 9. Maximum Safe Operating Area

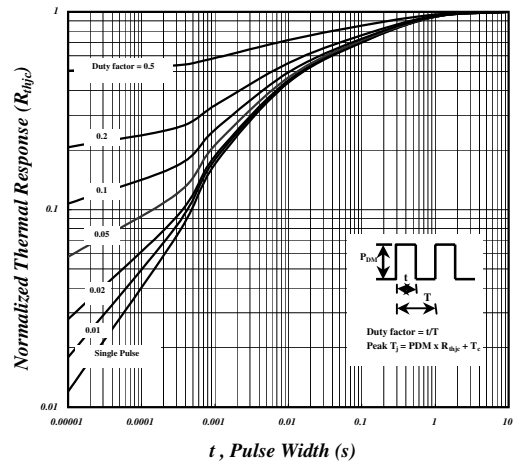


Fig 10. Effective Transient Thermal Impedance

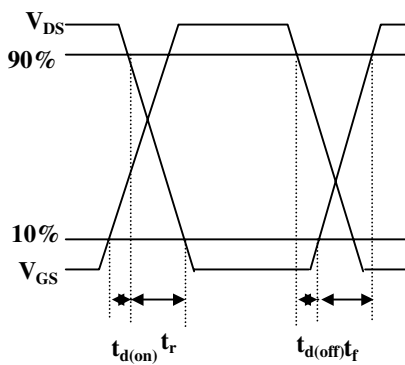


Fig 11. Switching Time Waveforms

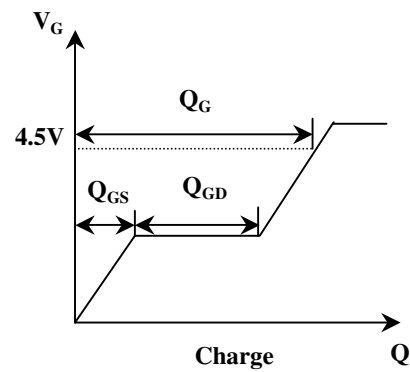
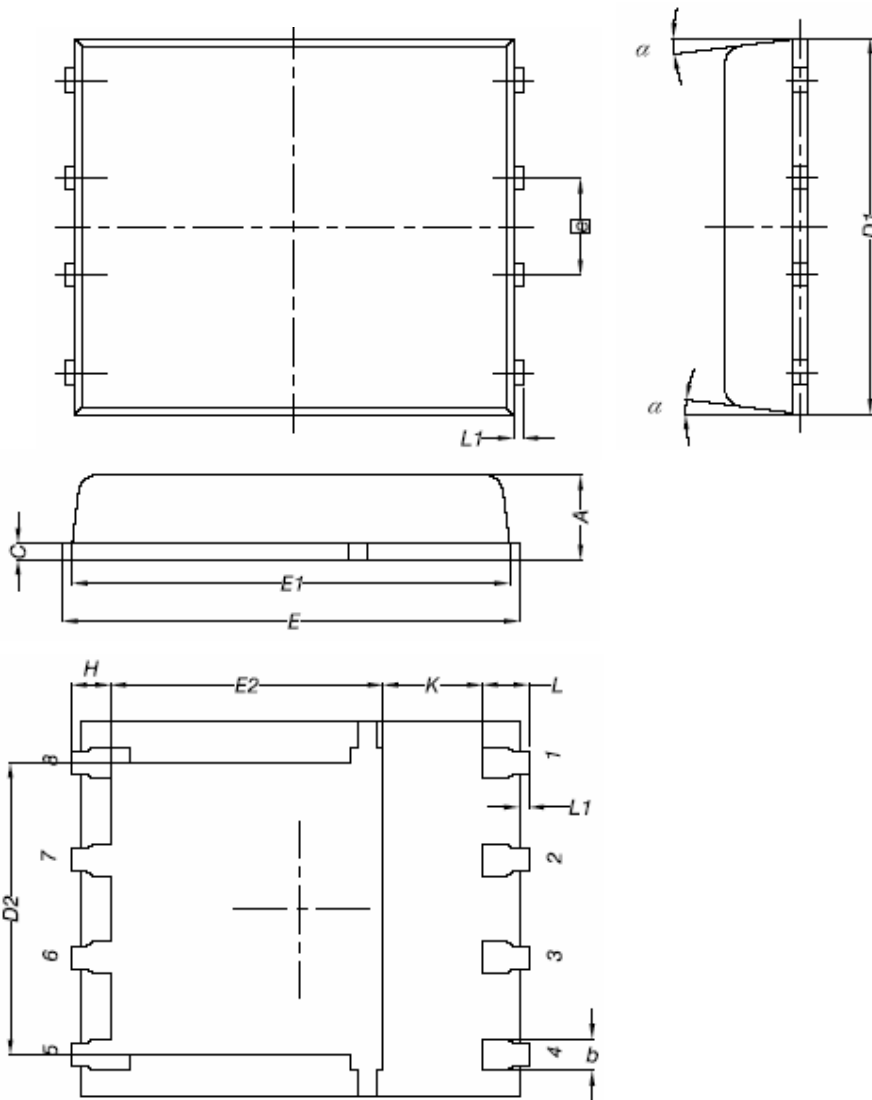


Fig 12. Gate Charge Waveform



**Package Dimensions: PMPAK<sup>®</sup>5x6**

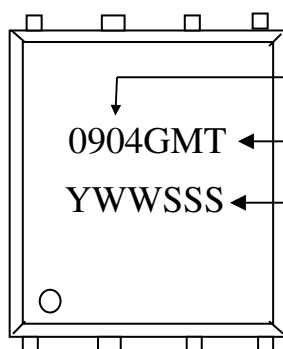


**BACKSIDE VIEW**

SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	-	-
D1	4.80	4.90	5.10
D2	-	-	4.20
E	5.90	6.00	6.10
E1 (Reference)	5.70	5.75	5.80
E2 (Reference)	3.38	3.58	3.78
e	1.27 BSC		
H	-	-	0.62
K (Reference)	0.70	-	-
L	0.51	0.61	0.71
L1	-	-	0.20
$\alpha$ (Reference)	0°	-	12°

1. All dimensions are in millimeters.
2. Dimensions do not include mold protrusions.

**Marking Information:**



Product: AP0904  
 Package code  
 GMT = RoHS-compliant halogen-free PMPAK<sup>®</sup>5x6  
 Date Code (YWWSSS)  
 Y: Last Digit Of The Year  
 WW: Work week  
 SSS: Lot code sequence