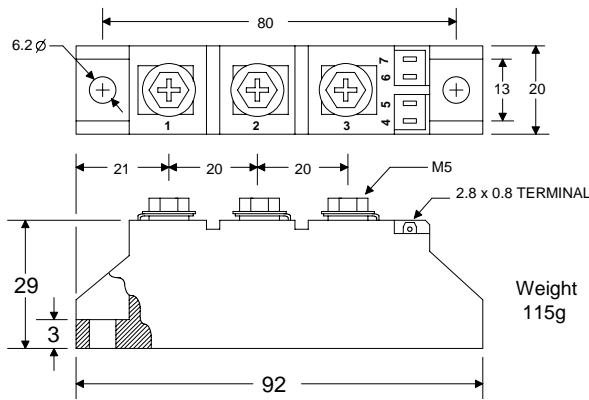
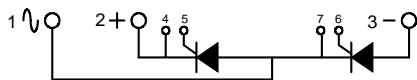


TO-240AA compatible package



Weight
115g

KT circuit



Gate Terminal	Table
4	K2
5	G2
6	G1
7	K1

Part number scheme

PS KT 110 N 16 STD
 1 2 3 4 5 6

- 1) Power Semiconductors initials
- 2) Circuit designation
- 3) Series number
- 4) Designates standard recovery time
- 5) Voltage Multiplier (example: 16 x 100 = 1600 Volts)
- 6) Proprietary suffix

Features:

- ✓ All diffused silicone junctions.
- ✓ Standard recovery time for phase control applications.
- ✓ Module package compatible with JEDEC TO-240AA.
- ✓ Thick copper base plate.
- ✓ Isolated cooling, rated up to 3500 V_{RMS}
- ✓ Easy mounting to heat sink
- ✓ Heat sink grounded.

Voltage

Parameter	Symbol	Rating	Units
Maximum Repetitive Off-State Voltage <small>Notes: 1, 3, 4, 5, 6, 7</small>	V_{DRM}	1200 ~ 1800	Volts
Maximum Repetitive Reverse Voltage <small>Notes: 1, 3, 4, 5, 6</small>	V_{RRM}	1200 ~ 1800	Volts
Maximum non repetitive Surge of Reverse Voltage <small>Notes: 2, 3, 4, 5, 6</small>	V_{RSM}	$V_{RRM} + 100$	Volts
Critical rate of rising off-state Voltage, Linear to 80% of V_{DRM} <small>Note: 2</small>	dv/dt	500	$V/\mu s$
<small>Note 1: $T_j 25^\circ C$. Note 2: $T_j 125^\circ C$. Note 3: Measured at the peak of the sine wave, Note 4: Below $0^\circ C$ derate V_{DRM} and V_{RRM} 10%. Note 5: V_{DRM} and V_{RRM} have I_{DRM}, I_{RRM} of up to 20mA. Note 6: V_{DR} and V_{RR} have typical I_{DR}, I_{RR} of 2-3mA. Note 7: For DC applications derate V_{DRM} 45%.</small>			
<small>Specifying voltage: 1400V, PSKT110N14 1800V, PSKT110N18 1200V, PSKT110N12 1600V, PSKT110N16 Above 1800V inquire about availability.</small>			

Gate

Parameter	Symbol	Rating			Units
		Temp.	Typ.	Max.	
Gate Trigger Voltage <small>Note 3</small>	V_{GT}	-20° C	0.9	2.0	Volts
		25° C	0.8		
		125° C	1		
Maximum Gate Trigger Current <small>Notes 1,3</small>	I_{GT}	50 ~ 120			mA
Minimum Forward Current to Latch on-state <small>Notes 1, 5</small>	I_L	400			mA
Maximum permissible Gate Voltage not to Trigger <small>Notes 1,3</small>	V_{GDM}	250			mV
Maximum permissible Gate Current not to Trigger <small>Notes 1, 3</small>	I_{GDM}	5			mA
Maximum peak non repetitive Gate Voltage <small>Notes 2, 3</small>	V_{GM}	5			Volts
Maximum Negative Gate Voltage <small>Notes 2, 4</small>	$-V_{GM}$	4			Volts
Maximum non repetitive Gate Current <small>Notes 2, 3</small>	I_{GM}	3			Amperes
Maximum Repetitive Gate Current <small>Notes 2, 3</small>	I_{GRM}	1			Amperes
Average Gate Power (recommended) <small>Note 2, 3</small>	$P_{G(AVE)}$	50 ~ 500			mW
<small>Note 1: $T_j 25^\circ C$. Note 2: $T_j 125^\circ C$. Note 3: Rectangular pulse, $t_b \leq 8.3$ ms. Note 4: Rectangular $-V_{DC}$ pulse, $t_b \leq 8.3$ ms. Note 5: Test conditions: $I_{DC} R_{\theta} = 12\Omega$.</small>					

Current

Parameter	Symbol	Rating	Units
Maximum, Average, On state, Current <small>Notes: 1, 2</small>	$I_{T(AVE)}$	110	Amperes
Maximum, RMS, On state, Current <small>Notes: 1, 3</small>	$I_{T(RMS)}$	175	Amperes
Maximum non repetitive, Surge, On state, Current, with no reverse voltage reapplied.	$I_{TSM} 0\% V_{RRM}$	2.1	kA
Maximum non repetitive, Surge, On state, Current, with maximum reverse voltage reapplied. <small>Notes: 2, 4</small>	$I_{TSM} 100\% V_{RRM}$	1.7	kA
Critical rate of rising On-state Current, non repetitive <small>Note: 6, 7</small>	di/dt	150	$A/\mu s$
Holding Current <small>Notes: 1, 5</small>	I_H	250	mA
Maximum On State Voltage drop at Maximum On State Current	$V_{TM} @ I_{TM}$	1.4 @ 200	V @ A
I_{DRM} = Maximum (threshold), Repetitive, Off-State, Current. <small>Note: 1</small> I_{RRM} = Maximum (threshold), Repetitive, Reverse, Current. <small>Note: 1</small>	I_{DRM} & I_{RRM}	20	mA
Fuse's absolute maximum $I^2 t$ with no reverse voltage	$I^2 t, 0\% V_{RR}$	17.9	kA
Fuse's absolute maximum $I^2 t$ with up to 100% of V_{RRM}	$I^2 t, \leq 100\% V_{RRM}$	11.6	kA
<small>Note 1: $T_j 55^\circ C$, Air Cooled Note 2: 120° Conduction, 60 Hz, Sinewave Note 3: 180° Conduction, 60 Hz, Sinewave Note 4: Test conditions $I_{DC} R_{\theta} = 12\Omega$ Note 5: Switching from $V_{DRM} < 1000V$ Note 6: In addition to 0.2μF and 20Ω snubber circuit</small>			