



**The Cardinal Cappuccino Crystal Oscillator LVDS/ LVPECL**

**Features**

- 2.5V or 3.3V supply voltage-configurable
- 750MHz to 1.5GHz LVDS and LVPECL outputs- configurable
- Better than 2Hz tuning resolution
- Low power, typically 23mA LVDS and 54mA LVPECL
- Temperature range: -40°C to +85°C
- Stability: ± 2.5ppm
- Phase Jitter (12kHz – 20MHz) .9ps RMS

**Applications**

- Multimedia
- Computing
- Networking, etc.

**Part Numbering Example: CJY E 7P L Z - A7 BR - XXX.XXX TS**

CJY	E	7P	L	Z	A7	BR	XXX.XXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CJY	L = LVDS E = LVPECL	5 = 5 X 3.2 Ceramic 7 = 5 X 7 Ceramic 5P = 5 X 3.2 Plastic 7P = 5 X 7 Plastic	S = 2.5V L = 3.3V	Z = Tape and Reel	A7 = -40°C to +85°C	BR = ± 25ppm BP = ±50ppm		TS = Tri-State

**Specification**

Waveform	LVDS/ LVPECL
Frequency	750MHz to 1.5GHz
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Supply Voltage	2.5V, 3.3V
Frequency Stability vs. Temp. Range	±25ppm/ ±50ppm
Input Current	23/54mA
Phase Jitter	.9ps Typical
Start-Up Time	10ms Max
Enable/ Disable Input Voltage	VIH ≥ 0.7VDD or No Connection, VIL ≤ 0.3VDD or Ground
Aging/ Year	±3ppm Max

**Description**

The Cardinal Cappuccino crystal oscillator is based on a high performance integrated circuit designed for use in Cardinal’s continued expanding leadership products in the programmable frequency control industry. Cardinal’s new Cappuccino design is today state of the art in oscillators. The Cappuccino line product features 10MHz to 1.5GHz with CJYL/ CJYE ranging 750MHz to 1.5GHz Output, 2.5V or 3.3V Supply Voltage, LVDS/ LVPECL commercial -20°C to +70°C and industrial temperature range -40°C to +85°C.

Cardinal’s new CJYL/ CJYE series is competitively priced and has the lowest typical power consumption 23/54mA LVDS/ LVPECL (70% less power than the Fox XpressO™ oscillator), lowest jitter and best phase noise over 10kHz to 20MHz vs. the traditional fixed frequency quartz oscillators and Surface Acoustic Wave oscillators. Cardinal’s programming centers utilize modern robotics, for testing, programming and 100% final testing as we do with all our programmable offerings. The Cardinal CJYL/ CJYE series line is offered in both ceramic and low cost plastic industry standard packages.

Cardinal’s Cappuccino line fits in all applications requiring a reference frequency including Multimedia, Computing, Networking, consumer etc.

**Absolute Maximum Ratings**

Item	Symbol	Condition	Unit
Input Voltage	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.5	V
Output Voltage	V <sub>O</sub>	-0.5 to V <sub>DD</sub> + 0.5	V
Positive Supply Voltage	V <sub>DD</sub>	4.2	V
Storage Temperature		-55 to +125	°C

**DC Electric Characteristics (T = 25°C)**

Unless stated otherwise, the data presented here was taken over the following parameters, V<sub>DD</sub> = 3.3V ± 10% or 2.5V ± 5%, Ta = -40°C to +85°C (industrial)

Item		Symbol	Specification			
			Min	Typ	Max	Units
Power Supply (V <sub>DD</sub> , GND pins)	Power Supply Voltage	V <sub>DD</sub>	2.97	3.3	3.63	V
		V <sub>DD</sub>	2.375	2.5	2.625	V
	LVDS I <sub>DD</sub>	I <sub>DD</sub>		23		mA
	LVPECL I <sub>DD</sub>	I <sub>DD</sub>		54		mA
	Current w/Output Disabled	I <sub>OED</sub>		16		mA
	Rise Time	T <sub>VDD</sub>	100			µS



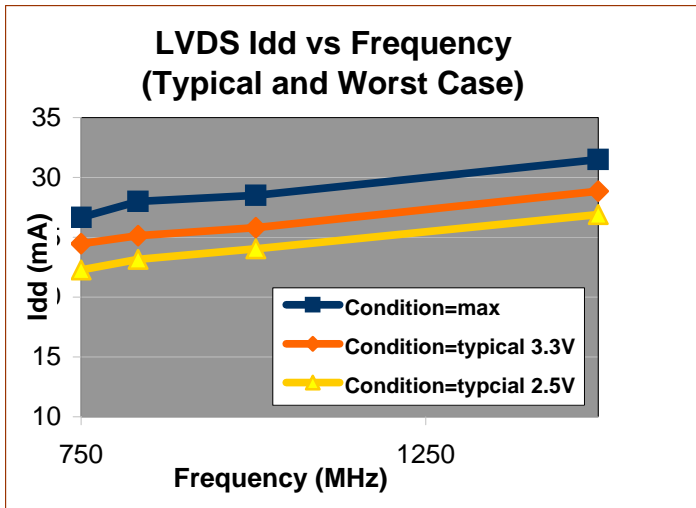
Item	Symbol	Specification				
		Min	Typ	Max	Units	
<b>AC Characteristics</b>						
<b>Outputs</b>						
LVDS (OUT, nOUT)	Frequency Range	$F_{LVDS}$	750		1500	MHz
	Stability		-25		+25	ppm
	Operating Temperature		-40		+85	°C
	Differential Output Voltage	$V_{OD}$	175	350		mV
	$V_{OD}$ Magnitude Change	$\Delta V_{OD}$			50	mV
	Offset Voltage	$V_{OS}$		1.25		V
	$V_{OS}$ Magnitude	$\Delta V_{OS}$			50	mV
	Duty Cycle	$DODC_{LVDS}$	45		55	%
	Rise Time	$t_R$	125		350	ps
	Fall Time	$t_F$	150		350	ps
LVPECL (OUT, nOUT)	Frequency Range	$F_{LVPECL}$	750		1500	MHz
	Stability		-25		+25	ppm
	Operating Temperature		-40		+85	°C
	Output High Voltage	$V_{OH}$	$V_{DD} - 1.03$		$V_{DD} - .6$	V
	Output Low Voltage	$V_{OL}$	$V_{DD} - 1.85$		$V_{DD} - 1.6$	V
	Differential Duty Cycle	$DODC_{LVPECL}$	45		55	%
	Rise Time	$t_R$	150		250	ps
	Fall Time	$t_F$	150		250	ps
OE Turn On Time (<50MHz)		$OE_{LOW/HIGH}$			200	ns
OE Turn On Time (>50MHz)		$OE_{LOW/HIGH}$			100	ns
OE Turn Off Time		$OE_{HIGH/LOW}$			50	ns
Jitter	Phase Jitter (12kHz to 20MHz)	$t_{jit}$	0.4	0.9	1.5	ps rms
	Period Jitter	$t_{RMS, DIFF}$		3	4.5	ps
		$t_{p-p, DIFF}$			30	45



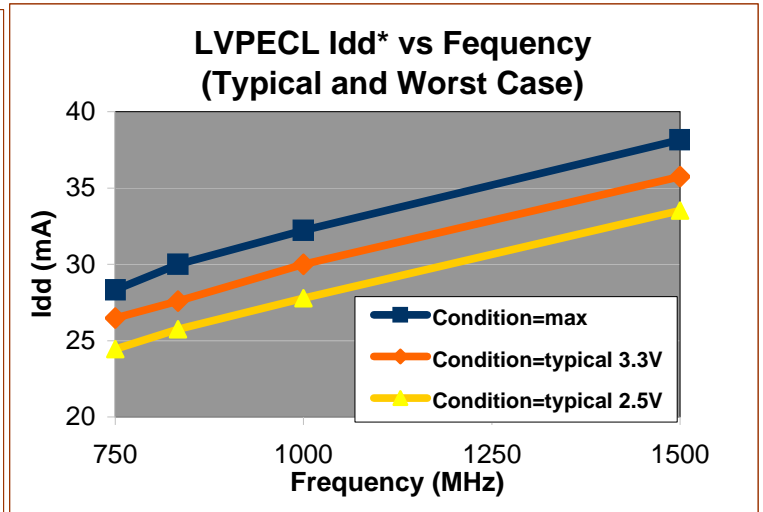
**Performance Characteristic Curves**

Unless otherwise specified, data is characterized over temperature range -40°C to +85°C and voltage range 2.2V - 3.63V.

$I_{DD}$  vs.  $V_{DD}$



**Figure 1.** LVDS  $I_{DD}$  vs. Frequency,  $V_{DD}$ .



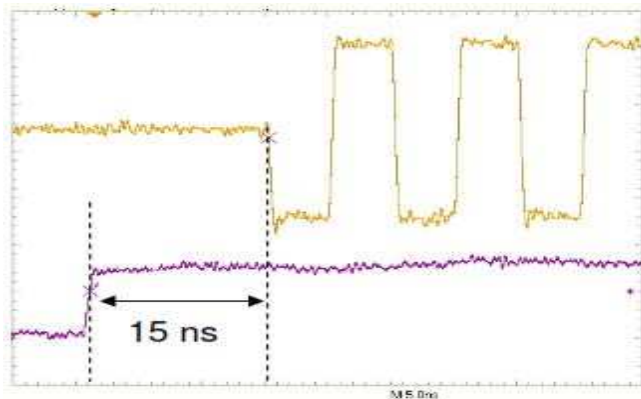
**Figure 2.** LVPECL  $I_{DD}$  vs. Frequency,  $V_{DD}$ .

Note: LVPECL  $I_{DD}$  does not include output load current.  
Add 32 mA to include output load current

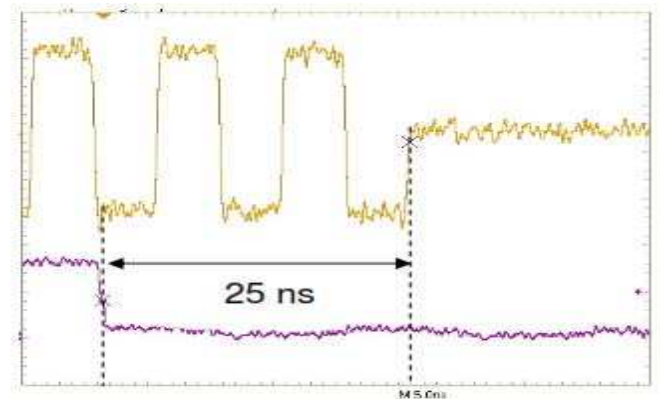
**OE Turn-on and Turn-off Times**

Notes:

- These measurements were all performed with an AC coupled output so that leakage currents do not affect the timing of the measurement. This results in all outputs floating to the midpoint of the signal levels when off.
- When LVDS is disabled the output goes to the common mode voltage (approximately 1.25V).
- When LVPECL is disabled the output goes to tri-state level which floats to  $V_{ol}$ .



**Figure 3.** 2.5V LVDS OE Enabled Time



**Figure 4.** 2.5V LVDS OE Disabled Time

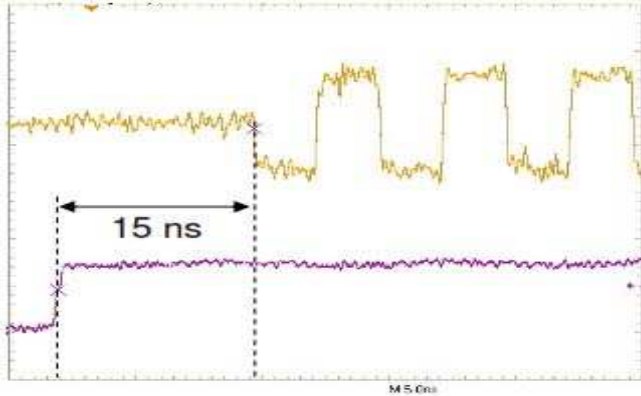


Figure 5. 3.3V LVDS OE Enabled Time

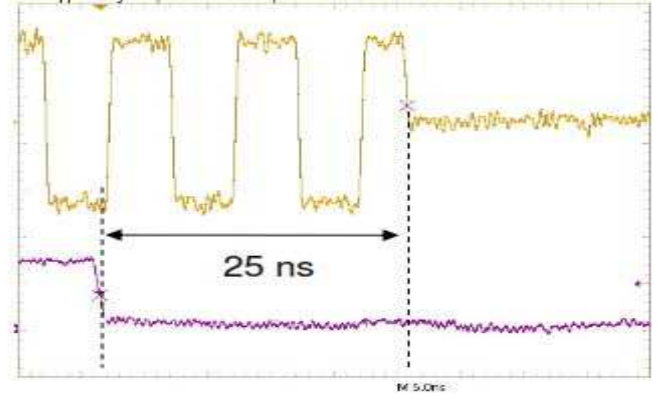


Figure 6. 3.3V LVDS OE Disabled Time

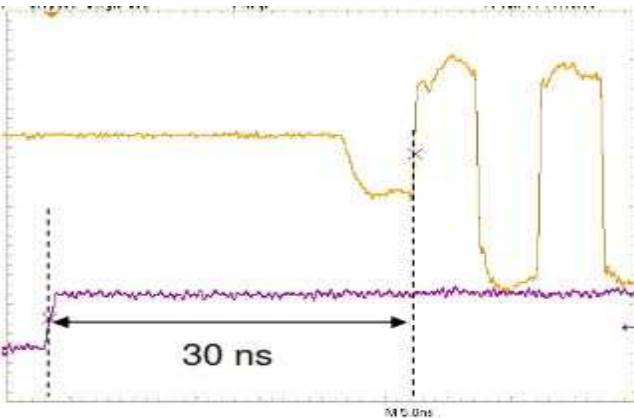


Figure 7. 2.5V LVPECL OE Enabled Time

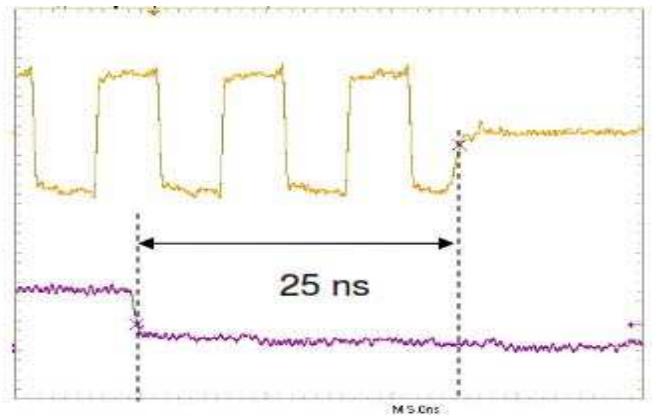


Figure 8. 2.5V LVPECL OE Disabled Time

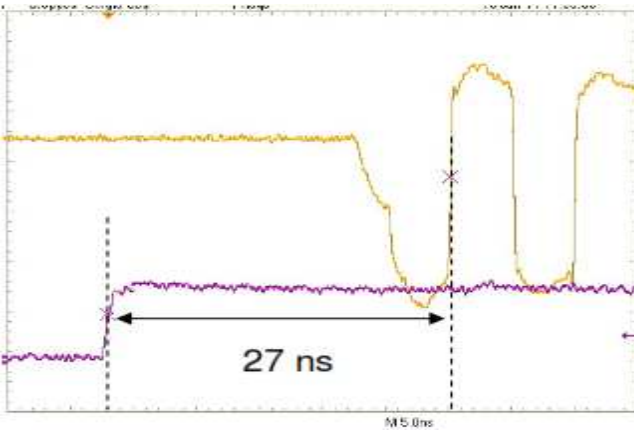


Figure 9. 3.3V LVPECL OE Enabled Time

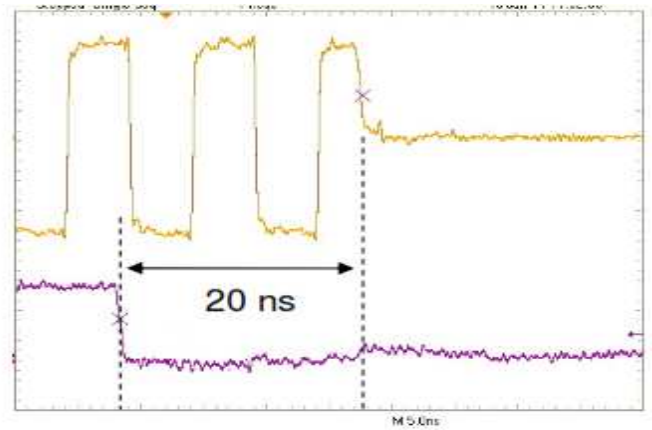
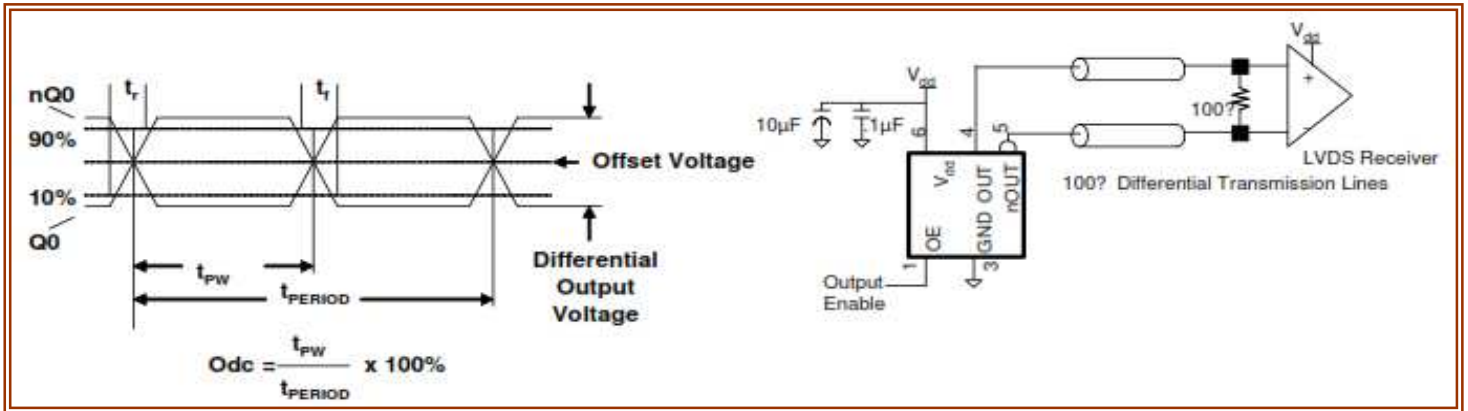


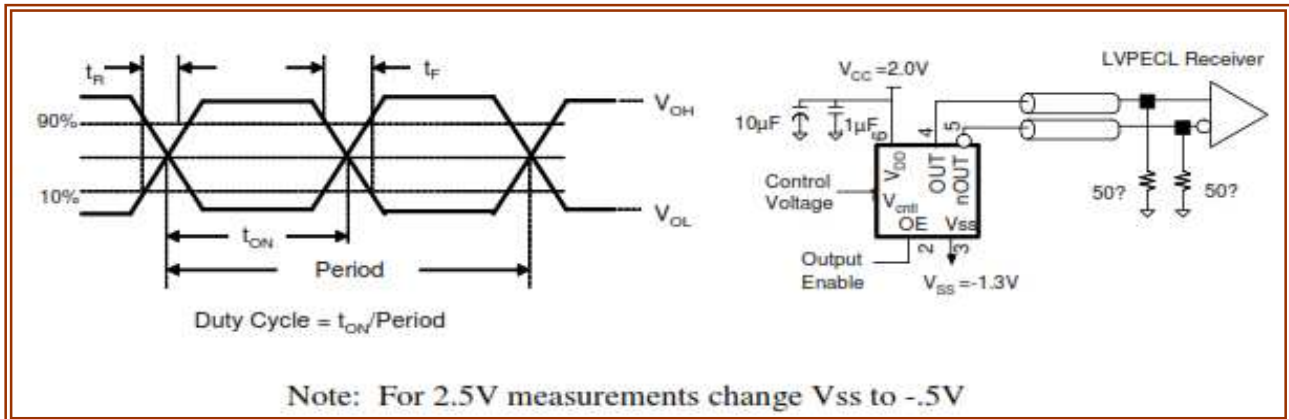
Figure 10. 3.3V LVPECL OE Disabled Time

**Waveform Measurements**

The following figures are descriptions for how the waveforms are measured for the datasheet applications.



**Figure 11.** 3.3V or 2.5V LVDS waveform measurement test setup



Note: For 2.5V measurements change Vss to -.5V

**Figure 12.** 3.3V LVPECL waveform measurement test setup

Application Information

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts offered are recommended only as guidelines.

OUT and nOUT are low impedance following outputs that generate LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 13 and 14 present two different designs. They are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designer simulate to guarantee compatibility across all printed circuit and clock component process variations.

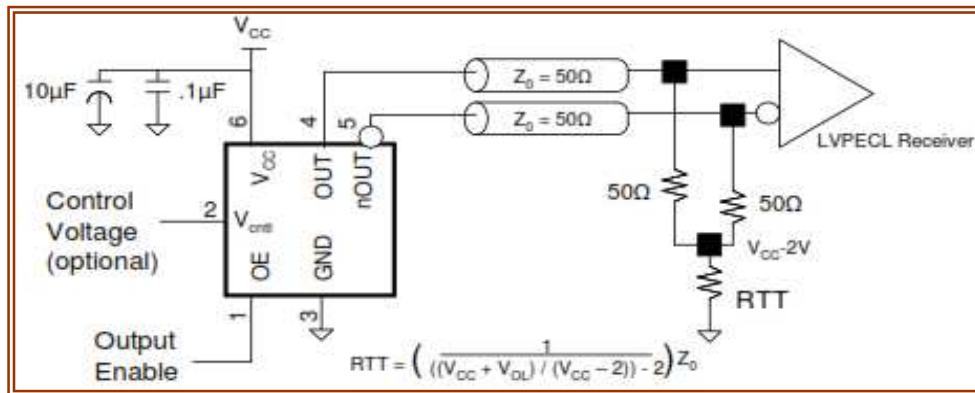


Figure 13. 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

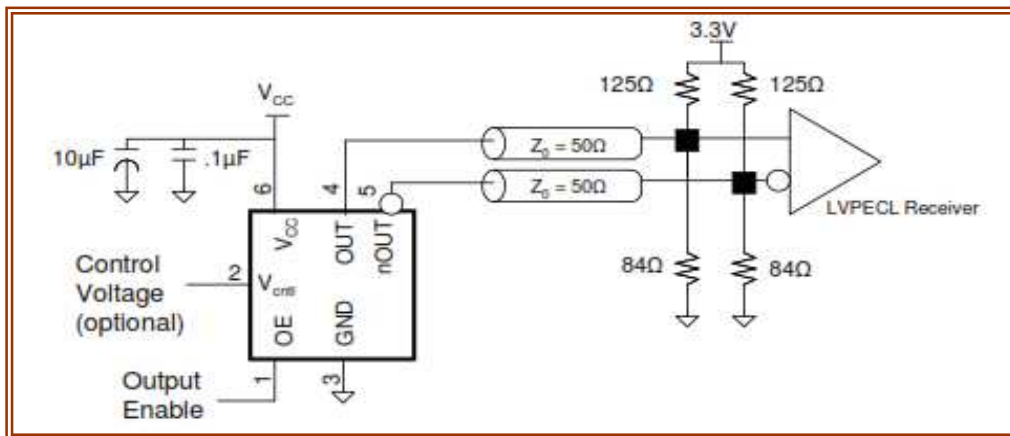
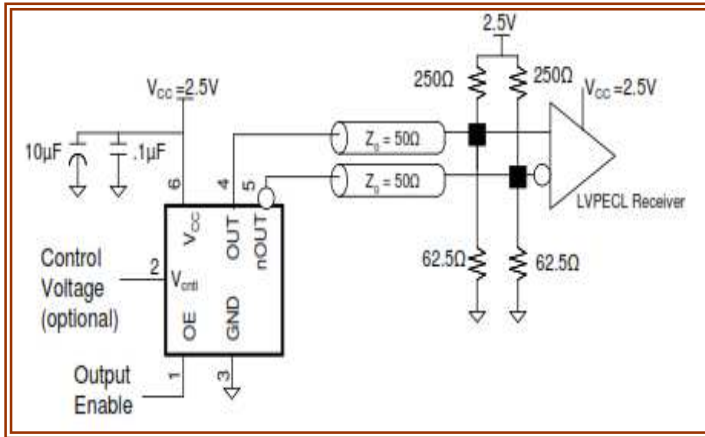


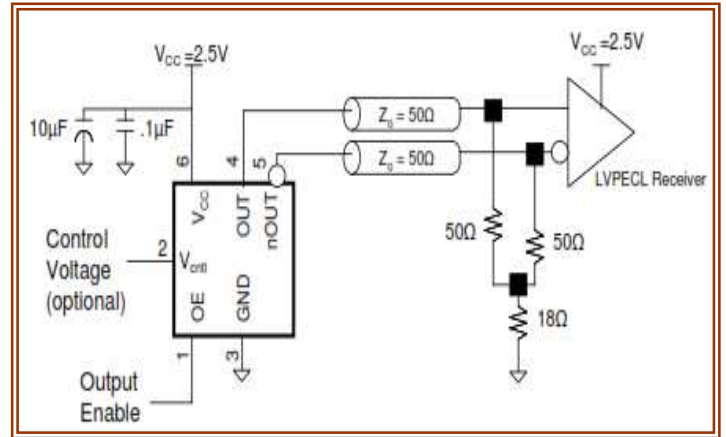
Figure 14. Alternate 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

**Termination for 2.5V LVPECL Output**

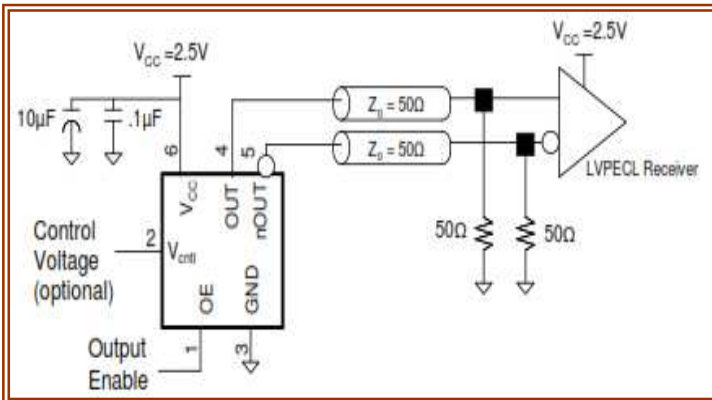
Figure 15-17 shows examples of termination for 2.5V LVPECL drivers. These terminations are equivalent to terminating 50Ω to VCC-2V. For VCC = 2.5V, the VCC-2V is very close to ground level. The 18Ω in Figure 16 can be eliminated and termination is shown in Figure 17.



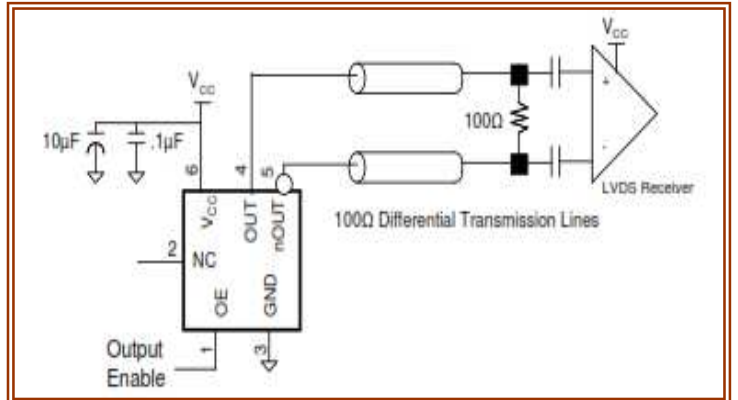
**Figure 15.** 2.5V LVPECL XO Drive Termination Example



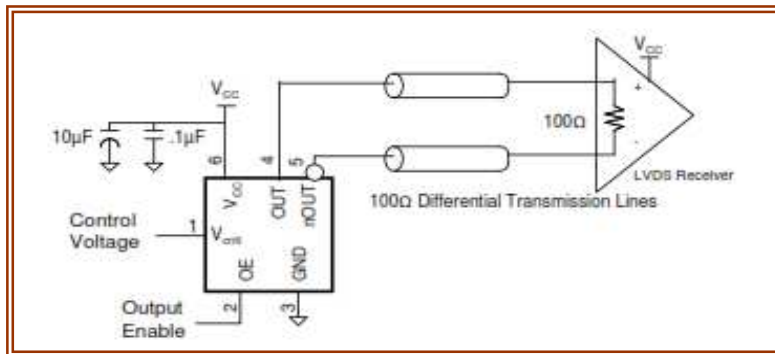
**Figure 16.** Alternate 2.5V LVPECL XO Drive Termination Example



**Figure 17.** Alternate 2.5V LVPECL XO Drive Termination Example



**Figure 18.** Termination for 3.3V and 2.5V LVDS Output

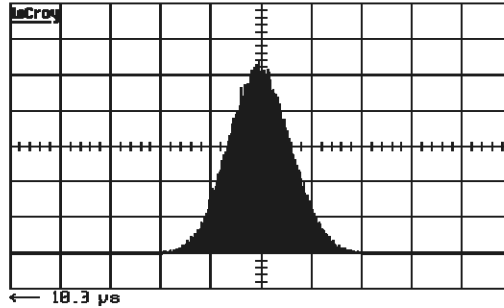


**Figure 19.** 3.3V and 2.5V LVDS XO Application Schematic & Power Supply Decoupling

### Phase Noise and Jitter

11-Feb-13  
22:46:11

Hp01v(2)  
5 ps  
200 #  
←8%/→8%  
in 155480



p01v(2) 6.430 ns  
low(D) 6.41447 ns  
high(D) 6.44472 ns  
range(D) 30.250 ps  
sigma(D) 3.054 ps

1 μs  
1 trig only  
2 83mV 500 ns  
3 disabled  
4 trig only

2 DC -13mV

SING. CLOCK

Select  
Measurement  
View

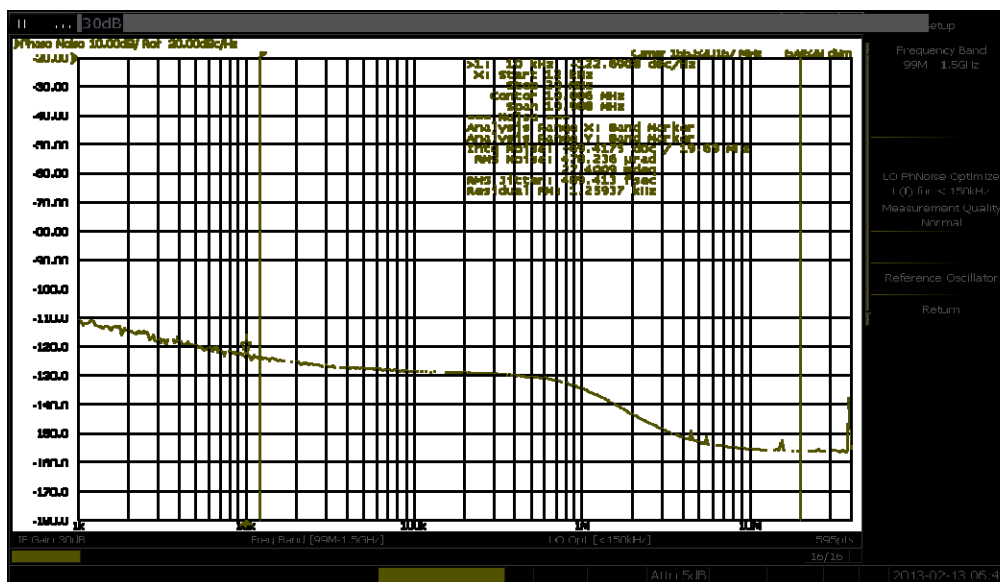
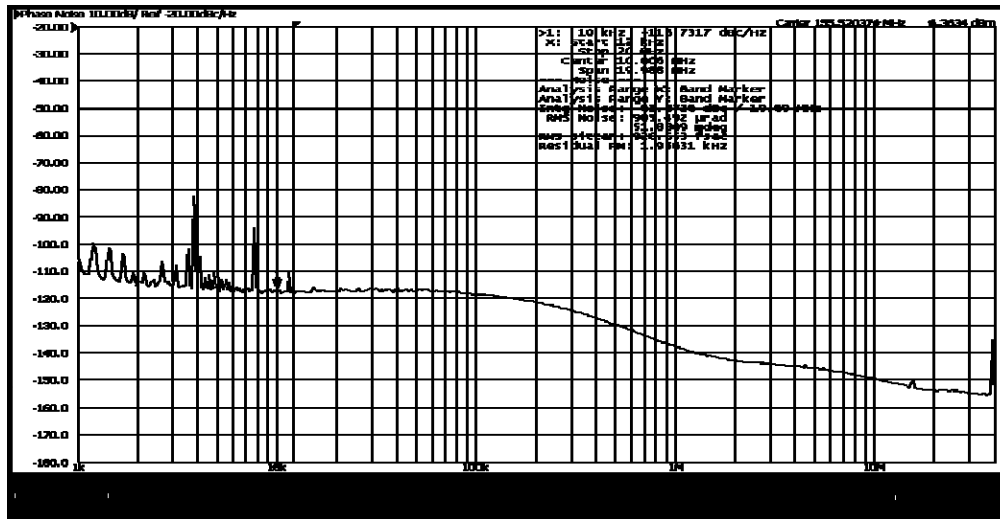
acquire mode  
Single

acquire  
18.00 μs

00  
ACQUISITION

8 GS/s

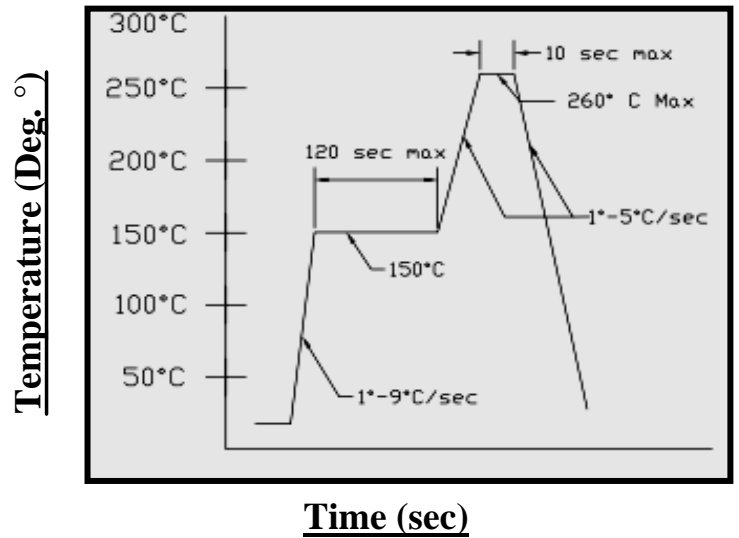
STOPPED



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Web: www.cardinalxtal.com

Recommended Solder Profile for  
 Cardinal Components, Inc.  
 Package Infrared Reflow.  
 Do Not Use Ultrasonic-Wave Soldering or  
 Wave Solder with Package Immersed in Solder  
 Damage to Crystal will result.



**Reliability**

Cardinal Components Inc., qualification includes aging at various extreme temperatures, shocks and vibration, temperature cycling, and IR reflow simulation. The Cappuccino family meets the following qualification tests:

Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/ JEDEC J-STD-020, MSL1

**Handling Precautions**

Although ESD protection circuitry has been designed into the Cappuccino proper precautions should be taken when handling and mounting. Cardinal employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

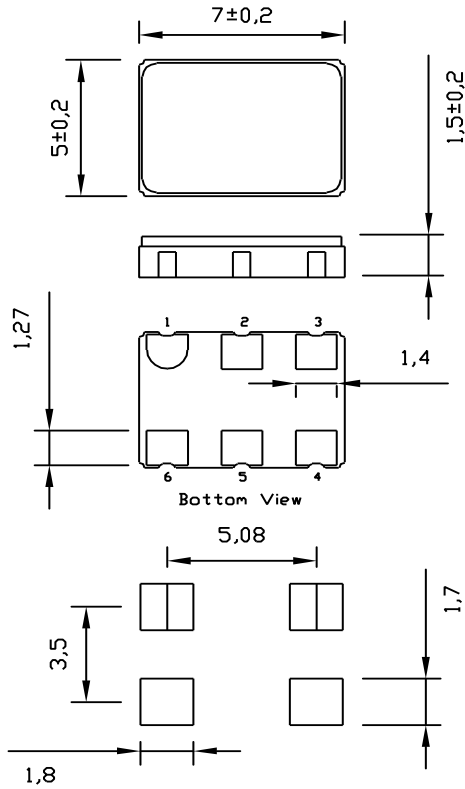
ESD Ratings		
Model	Minimum	Conditions
Human Body Model	1000V	MIL-STD-883, Method 3015
Charged Device Model	900V	JEDEC, JESD22-C101
Machine Model	200V	JEDEC, JESD22-A115-A



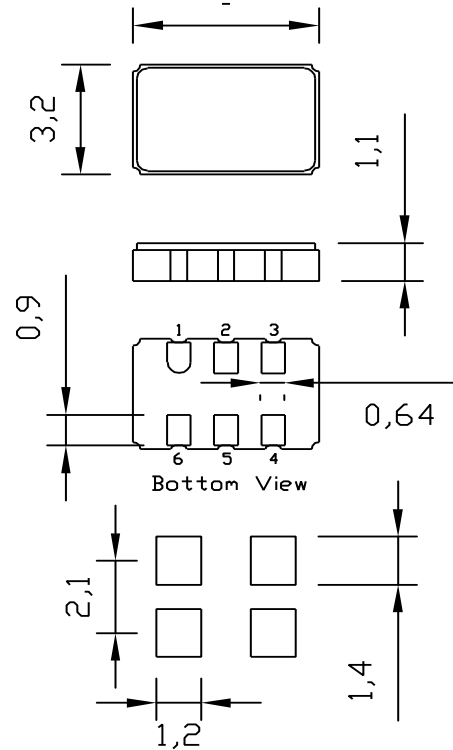
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**Style 7: 5x7mm Ceramic**



**Style 5: 5x3.2mm Ceramic**



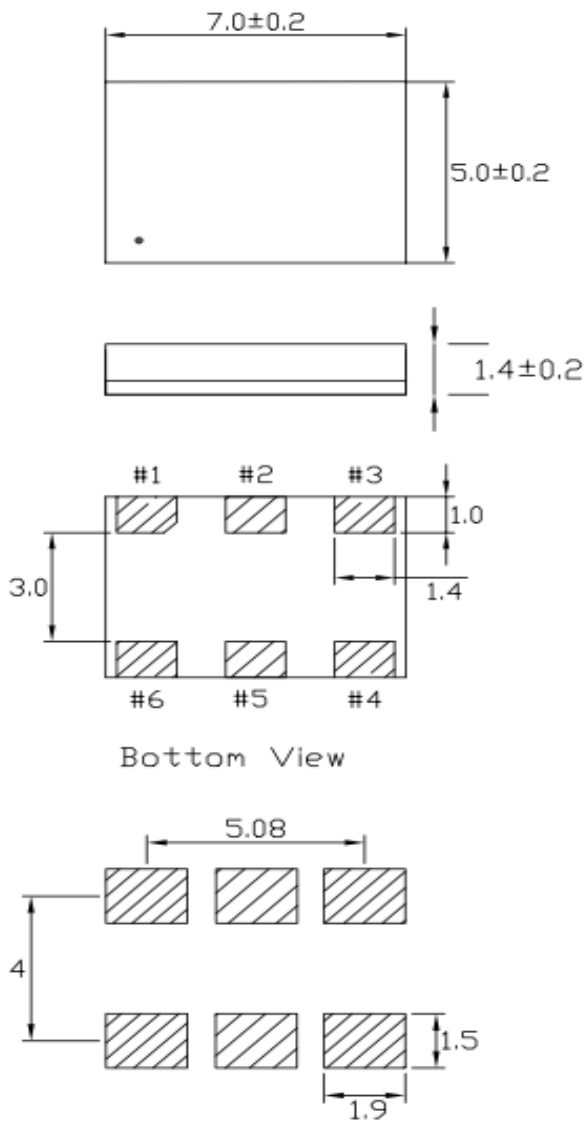
**6 Pad LVDS/LVPECL**

Pin 1	OE
Pin 2	Do Not Connect
Pin 3	GND
Pin 4	OUT
Pin 5	nOUT
Pin 6	V <sub>DD</sub>

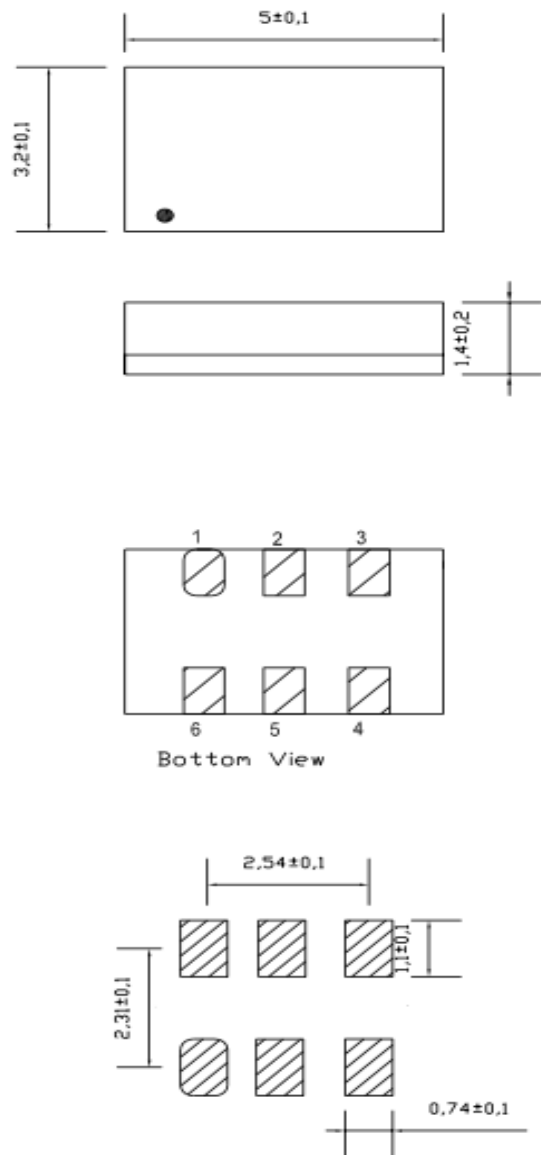
**6 Pad LVDS/LVPECL**

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Pin 6	V <sub>DD</sub>

**Style 7P: 5x7mm Plastic**



**Style 5P: 5x3.2mm Plastic**



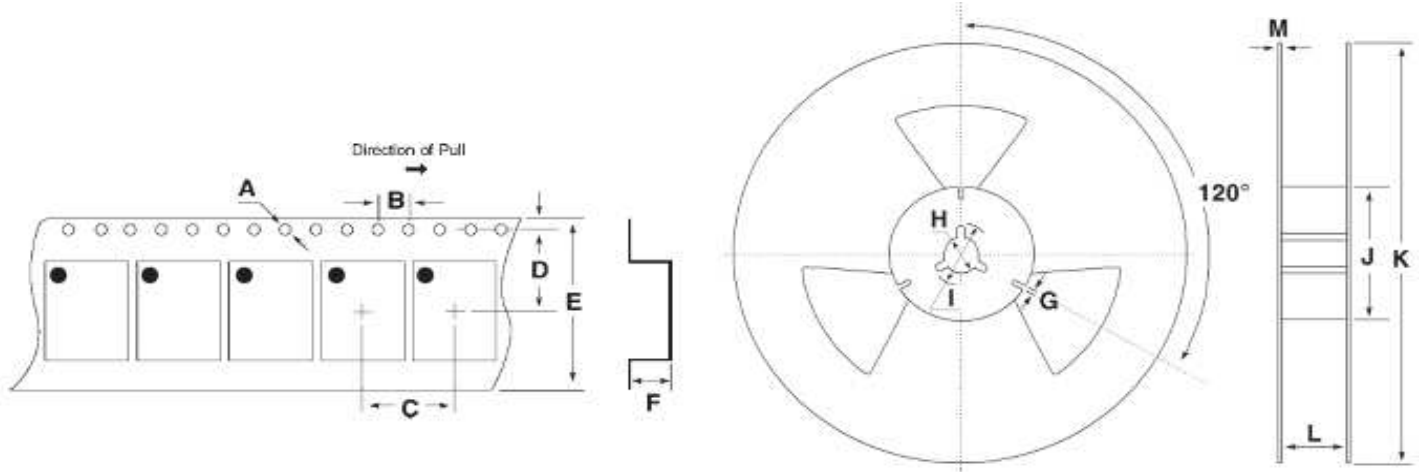
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**6 Pad LVDS/LVPECL**

Pin 1	OE
Pin 2	Do Not Connect
Pin 3	GND
Pin 4	OUT
Pin 5	nOUT
Pin 6	V <sub>DD</sub>

**Tape and Reel Specifications**



**Tape Specifications (mm)**

Model	A	B	C	D	E	F	STD QTY *
CJYL/ CJYE	1.5	4.0	8.0	9	16.0	1.8	1,000

**Reel Specifications (mm)**

Model	G	H	I	J	K	L	M
CJYL/ CJYE	2.0	13	21	60	180	17.5	1.0