CARDINAL COMPONENTS

Programable HCMOS Oscillator

Platinum Series CAMs

- *Extra Small Packaging Style*
- *Low Jitter*
- *Low Phase Noise*
- *Immediate Delivery*

Pb
RoHS COMPLIANT 2002 / 95 / EC

Part Numbering Example: CAMs C 3 Q Z - A5 B6 - XXX.XXXX TS

CAMs	C	3	Q	Z	A5	B6	XXX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	PACKAGING OPTIONS	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CAMs	C=HCMOS	3 = 3.2 X 2.5 Ceramic	Q = 1.8 V	Blank = Bulk	Blank = 0°C +70°C	B6 = ±100 ppm	1.5~133.000 MHz	TS = Tri-State
		5 = 5.0 X 3.2 Ceramic	S = 2.5 V	T = Tube	A5 = -20°C +70°C	BP = ±50 ppm		PD= Power Down
		7 = 5.0 X 7.0 Ceramic	L = 3.3 V	Z = Tape and Reel	A7 = -40°C +85°C	BR = ±25 ppm		NC = No Connect

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	1.500		133.000	MHz
Available Stability Options:	-100 -50 -25		100 50 25	ppm ppm ppm
Supply Voltage Options: (1.5–133 MHz)	2.97 2.25 1.62	3.3 2.5 1.8	3.63 2.97 1.98	V
Operating Temperature Range Options:	0 -20 -40		+70 +70 +85	°C °C °C
Storage Temperature:	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V/2.5V			±5	

Output Level:	HCMOS
Packaging:	Tape and Reel (1K per Reel) Tube

Operating Conditions:

Description	Min	Max	Unit
Vdd Rise Time:	100		µS
HCMOS Max Capacitive Load on outputs for CMOS levels Frequency: < 40 MHz Frequency: 40–133 MHz		 25 15	 pF pF

- *Extra Small Packaging Styles*
- *Low Jitter*
- *Low Phase Noise*
- *Immediate Delivery*

Electrical Characteristics

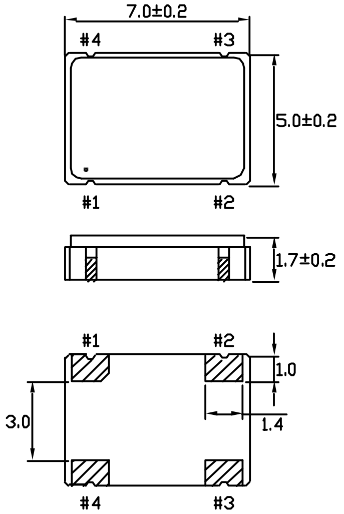
Description	TEST CONDITIONS	Min	Typ	Max	Unit
Input Characteristics (Pin 1): V_{IL}, Low–Level Input Voltage TO DISABLE OUTPUT				0.2Vdd	V
V_{IH}, High–Level Input Voltage TO ENABLE OUTPUT OR open		0.7VddV			
I_{IL}, Input Low Current I_{IH}, Input High Current	V_{IN} = 0V V_{IN} =Vdd			80 10	µA µA
Output Characteristics: V_{OL}, Low–Level Output Voltage	8 mA I_{OL}			0.4	V
V_{OHCMOS}, High-level HCMOS Voltage	-8 mA I_{OL}	Vdd-0.4			V
Power Supply Current: **(Loaded)**	1.8V Vdd, OUTPUT FREQ ≤ 133 MHz			15	mA
Tri-State Internal Pull-up:	Output Active when pin 1 high	50	70	90	kΩ
Tri-State Leakage Current:	TS option, Pin 1 low			20	µA
Power Down Current:	PD option, Pin 1 low			10	µA

"Tristate internal pull up. Output active when high"

Output Clock Switching Characteristics

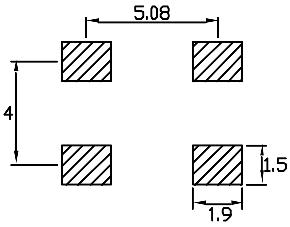
Description	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle: HCMOS @ Vdd/2		45		55	%
Output Clock Rise/Fall:	0.2–0.8Vdd, C_L = 15		2		nS
Start Up Time:	From power on		3	10	mS
RMS Period Jitter:			7	10	pS
RMS Integrated Jitter:	12kHz to 20MHz		30		pS
Phase Noise:	@ 10kHz			-90	dBc/Hz

Style 7 5x7 Ceramic SMD

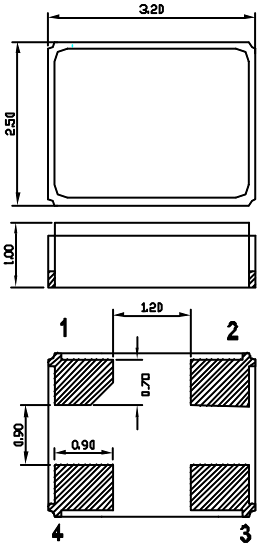


PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Recommended Solder Pad Layout

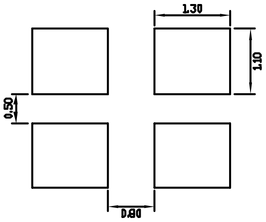


Style 3 3.2x2.5 Ceramic SMD

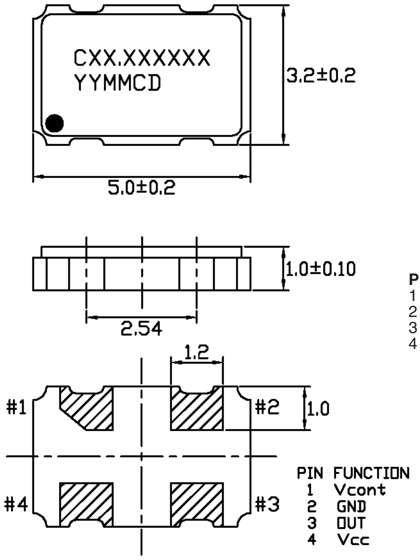


PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Recommended Solder Pad Layout

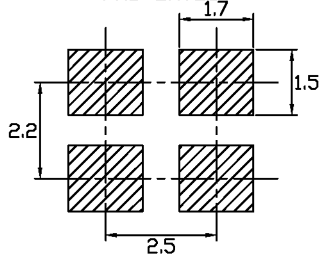


Style 5 5x3.2 Ceramic SMD



PIN FUNCTION
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

Recommended Solder Pad Layout



Note: *Bypass Vdd to GND with a 0.01µF capacitor*