

Factory Prog. 4 Output PECL Oscillator

- Full Custom Multi-Frequency Programmable Osc
- Reduced EMI by turning off unused output
- Factory Programmable
- Differential PECL Output
- Industry-standard packaging saves on board space
- Mult. outputs 1 pkg vs. mult. osc & assoc. comp.
- Lower system cost

Applications

- High-end multimedia
- Communications
- Industrial
- A/D converters
- Consumer Applications
- Product differentiation
- Low-power applications

Series **CCE4E**



Part Numbering Example: CCE4E 1A 200.0 - 150.0 / 125.0

CCE4E	1A	200	150	125
SERIES	PACKAGE STYLE	FREQUENCY P/P-	FREQUENCY A	FREQUENCY B
	1A=14 pin dip 9=9.6x11.4 SMD	100-400 MHz PECL	0.2 - 200 MHz	0.2 - 200 MHz

Specifications:	Min	Typ	Max	Unit
Frequency Range:				
Output PECL +	100		400	MHz
Output PECL -	100		400	MHz
Output A CMOS	0.2		200	MHz
Output B CMOS	0.2		200	MHz
Available Stability Options:	-50		50	ppm
Supply Voltage:	3.135	3.3	3.465	V
Operating Temperature Range Options:	-40		85	°C
Storage Temperature:	-55		125	°C
Duty Cycle:	40 45		60 55	% %
Start-Up Time:		3	10	mS
Aging (PPM/1st Year): Ta=25C, Vdd=3.3V			±5	
Static Discharge Voltage Mil-Std 883, method 3015	2000			V
Output Load: * CMOS, < 40 MHz CMOS, ≥ 40 MHz			30 15	pF pF
Output Level:	PECL/CMOS			
Packaging:	25 / Tube Tape & Reel			14 pin SMD

Notes: Recommended .01 µF bypass capacitor from Vcc to GND. Capacitor should be as close to oscillator as possible.
* LV PECL outputs require an external termination network



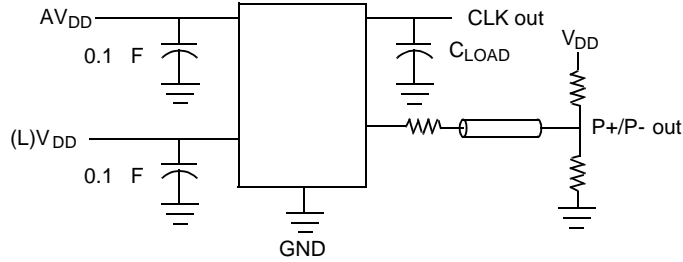
Electrical Characteristics

DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
Ioh	Output High Current	Voh = (L)Vdd - 0.5, (L)Vdd = 3.3 V	12	24		mA
Iol	Output Low Current	Vol = .5, (L)Vdd = 3.3 V	12	24		mA
Vih	High Level Input Voltage	CMOS levels, % of Vdd	0.7			V
Vil	Low-Level Input Voltage	CMOS levels, % of Vdd			0.3	V
Iih	Input High Current	Vin = AVdd - 0.3 V		<1	10	μA
Iil	Input Low Current	Vin = + 0.3 V		<1	10	μA
Ioz	Output Leakage Current	tri-state outputs			10	μA
Idd	Total Power Supply Current	Example 1: 1 PECL output @155.52 MHz 1 CMOS output @19.44 MHz 1 CMOS output @38.88 MHz		26		mA
		Example 2: 1 PECL output @400 MHz 1 CMOS output @106.25 MHz 1 CMOS output @53.125 MHz		48		mA
Idds	Shutdown Power Supply Curr	Shutdown active		5	20	μA

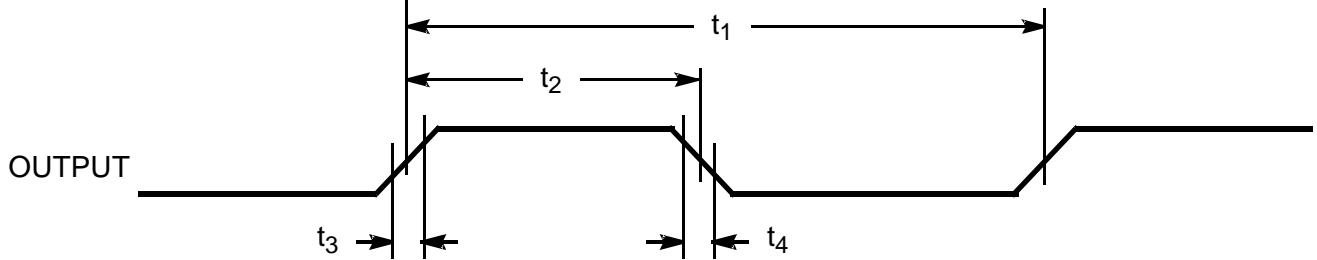
Output Clock Switching Characteristics

DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
1/t1	Output Frequency	Clock output limit, CMOS, Commercial	0.2		200	MHz
		Clock output limit, PECL, Commercial	100		400	MHz
t3	Rising Edge Slew Rate	Output clock rise time, 20% – 80% Vdd	0.75	1.4		nS
t4	Falling Edge Slew Rate	Output clock fall time, 20% – 80% Vdd	0.75	1.4		nS
t5	Output tri-state timing after SD/OE switches	Time for output to enter/leave tri-state mode		150	300	nS
t6	Clock Jitter measured at Vdd/2	Peak-to-Peak period jitter, CLK outputs		200		pS
v7	P+/P- Crossing Point	Crossing point ref. to Vdd/2, bal res. net	-0.2	0	0.2	V

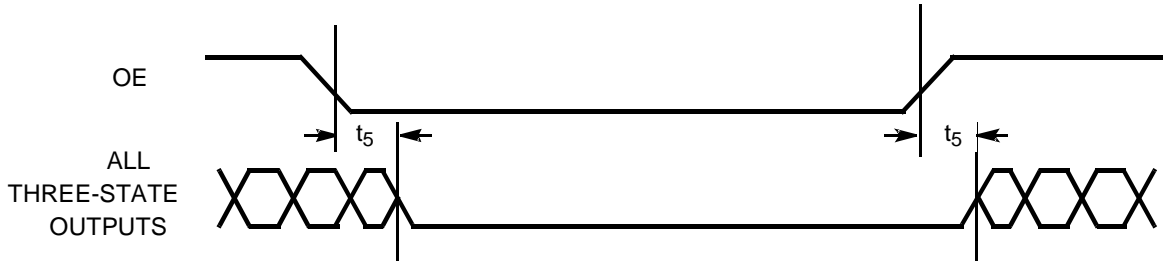
TEST CIRCUIT



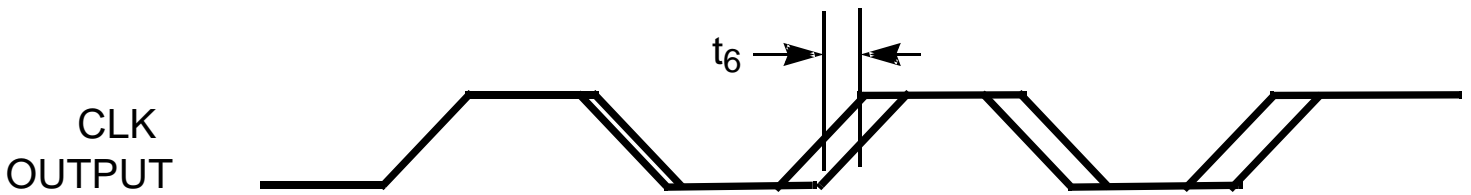
ALL OUTPUTS, DUTY CYCLE, RISE/FALL TIME



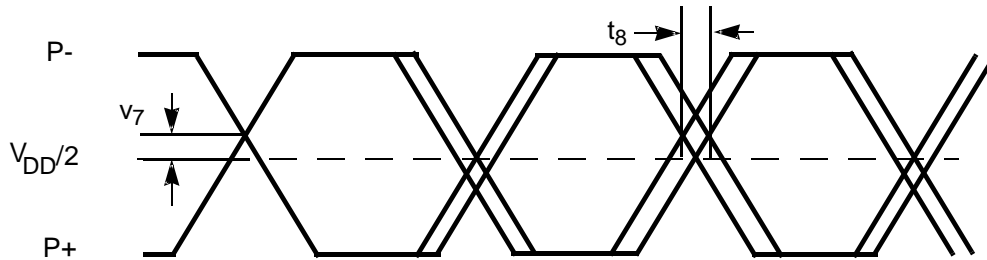
OUTPUT 3-STATE TIMING



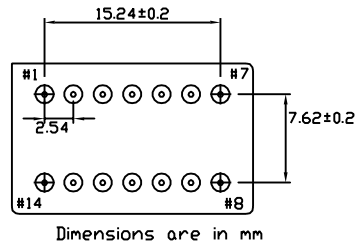
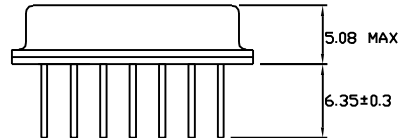
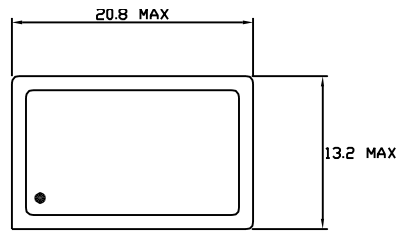
CLK OUTPUT JITTER



P+/P- CROSSING POINT AND JITTER



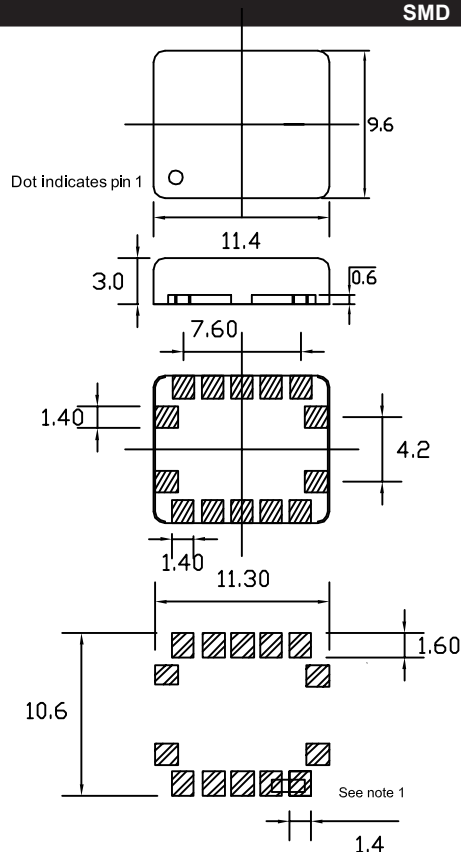
DIP



PIN FUNCTION

- PIN 1 OE (CONNECT TO VDD)
- PIN 2 SUSPEND (CONNECT TO GND)
- PIN 3 VDD
- PIN 4 FACTORY USE (MAKE NO CONNECTION)
- PIN 5 CONNECT TO PIN 6
- PIN 6 CONNECT TO PIN 5
- PIN 7 GND
- PIN 8 FACTORY USE (MAKE NO CONNECTION)
- PIN 9 PECL - OUTPUT
- PIN10 PECL + OUTPUT
- PIN 11 FACTORY USE (MAKE NO CONNECTION)
- PIN 12 FACTORY USE (MAKE NO CONNECTION)
- PIN 13 CLK A OUTPUT
- PIN 14 CLK B OUTPUT

SMD



PIN FUNCTION

- PIN 1 FACTORY USE (MAKE NO CONNECTION)
- PIN 2 OE
- PIN 3 VDD
- PIN 4 FACTORY USE (MAKE NO CONNECTION)
- PIN 5 CONNECT TO PIN 6
- PIN 6 CONNECT TO PIN 5
- PIN 7 GND
- PIN 8 FACTORY USE (MAKE NO CONNECTION)
- PIN 9 PECL - OUTPUT
- PIN10 PECL + OUTPUT
- PIN 11 FACTORY USE (MAKE NO CONNECTION)
- PIN 12 FACTORY USE (MAKE NO CONNECTION)
- PIN 13 CLK A OUTPUT
- PIN 14 CLK B OUTPUT

Dimensions in mm
Recommended solder pad layout

Note1:
For proper operation pin 5 must be connected to pin 6

