Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF110P05J
SFF110P05M
SFF110P05S1

DESIGNER'S DATA SHEET

RADIATION TOLERANT
110 AMP , 50 Volts, 14 mΩ
Avalanche Rated P-MOSFET

Part Number / Ordering Information[1/]

SFF110P05 ___ ___ ___

Screening[2/]
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Option
__ = Straight Leads
DB = Down Bend
UB = Up Bend

Package[3/]
M = TO-254
J = TO-257
S1 = SMD1

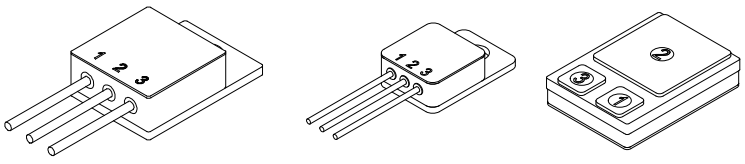
Features:
- Rugged Trench Technology
- Lowest ON-resistance in the industry: 10mΩ typ
- Radiation tolerant: less than 0.5V typical gate threshold shift @ TID= 100kRAD
- SEU and SEGR resistant to LET 38
- Avalanche rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	-50	V
Gate - Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited) @ 25ºC	TO-257 TO-254 SMD1	I_{D1}	30 55 85	A
Max. Instantaneous Drain Current (Tj limited) T_C = 25ºC	TO-257, TO-254 SMD1	I_{D2} I_{D3}	80 110	A
Max. Avalanche current	@ L = 0.1 mH	I_{AS}	70	A
Single Pulse Avalanche Energy	@ L = 0.1 mH	E_{AS}	1000	mJ
Total Power Dissipation @ T_C = 25ºC	TO-257, TO-254 SMD1	P_D	90 125	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	ºC
Maximum Thermal Resistance (Junction to Case)	TO-257, TO-254 SMD1	$R_{\theta JC}$	1.4 1 (typ.0.5)	ºC/W

NOTES:
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Maximum current limited by package configuration
4/ Unless otherwise specified, all electrical characteristics @25°C.

TO-254 **TO-257** **SMD1**



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Electrical Characteristics[4/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	BV_{DSS}	-50	—	—	V
Drain to Source On State Resistance	V_{GS} = -10V, I_D = -70A, Tj = 25°C V_{GS} = 10V, I_D = -70A, Tj =125°C V_{GS} = 10V, I_D = -70A, Tj = 150°C	$R_{DS(on)}$	— — —	9 14 15	14 22 —	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -0.25mA, Tj = 25°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj = 125°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj = -55°C	$V_{GS(th)}$	-2.0 2.0 —	— — —	-4.0 — —	V
Gate to Source Leakage	V_{GS} = ±20V, Tj = 25°C V_{GS} = ±20V, Tj = 125°C	I_{GSS}	— —	10 30	±100 —	nA
Zero Gate Voltage Drain Current	V_{DS} = -50V, V_{GS} = 0V, T_j = 25°C V_{DS} = -50V, V_{GS} = 0V, T_j = 125°C	I_{DSS}	— —		-10 -750	µA µA
Forward Transconductance	V_{DS} = -10V, I_D = -70A, T_j = 25°C V_{DS} = -10V, I_D = -70A, T_j = -40°C V_{DS} = -10V, I_D = -70A, T_j = 125°C	g_{fs}	40	70 85 63	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = -10V V_{DS} = -25V I_D = -70A	Q_g Q_{gs} Q_{gd}	— — —	200 50 65	350 - -	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = -10V V_{DS} = -30V I_D = -50A R_G = 1.0Ω, pw= 3us	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	30 35 40 25	45 75 100 75	nsec
Diode Forward Voltage	I_F = -70A, V_{GS} = 0V	V_{SD}	—	-	1.3	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	I_F = -70A, di/dt = -100A/usec	t_{rr} Q_{rr}	— —	55 60	250 —	nsec nC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	13,500 1650 650	— — —	pF

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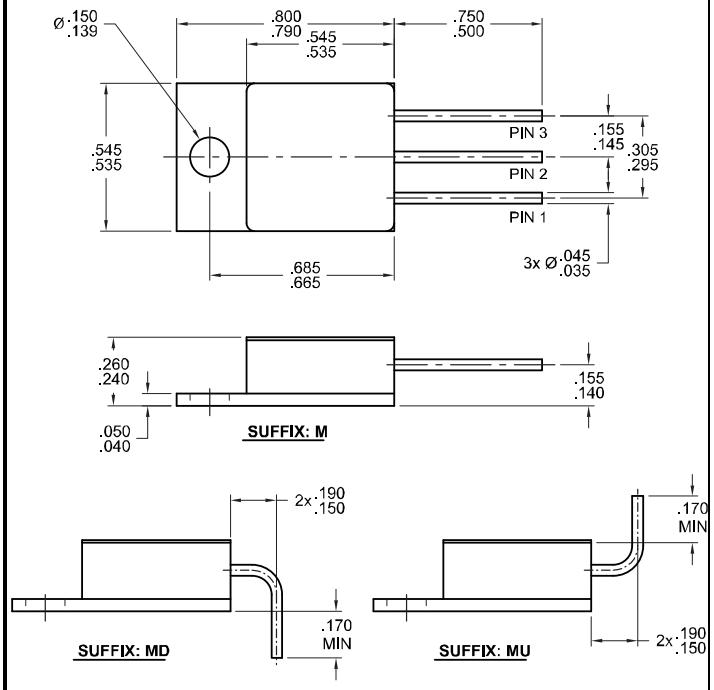
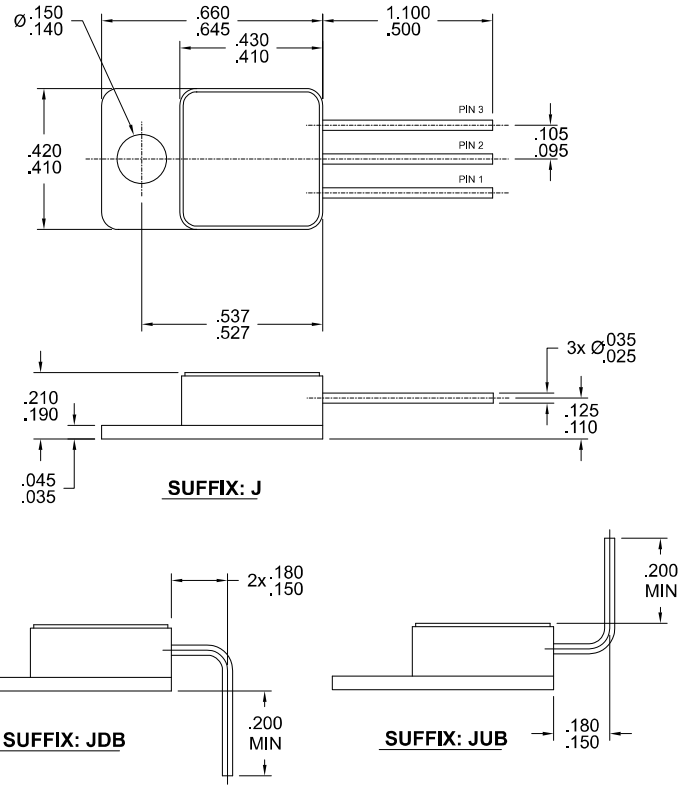
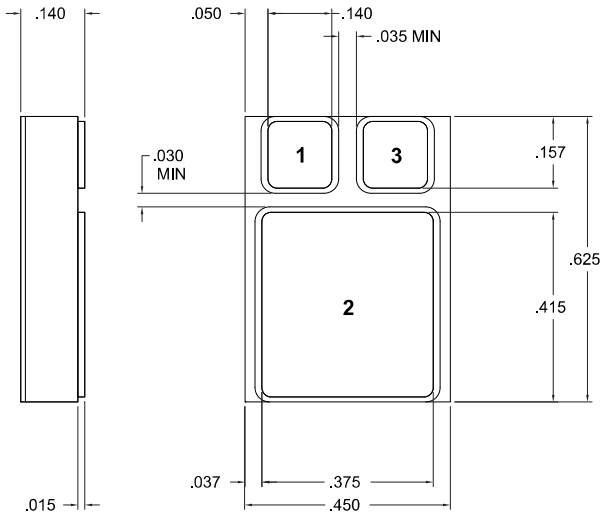
TO-254 (M)



TO-254 (J)



SMD1 (S1)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-257 (J)	Pin 1	Pin 2	Pin 3
SMD1 (S1)	Pin 2	Pin 1	Pin 3

Available Part Numbers:

SFF110P05M, SFF110P05MDB, SFF110P05MUB,
SFF110P05J, SFF110P05JDB, SFF110P05JUB,
SFF110P05S1