



Solid State Devices, Inc.

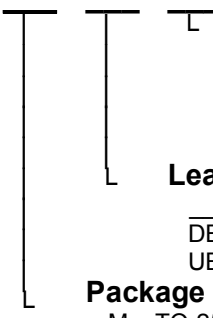
14701 Firestone Blvd * La Mirada, Ca 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFF50N30M
SFF50N30Z

50 AMP , 300 Volts, 50 mΩ
Avalanche Rated N-channel
MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}
SFF50N30



Screening ^{2/}

— = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

Lead Option ^{3/}

— = Straight Leads
 DB = Down Bend
 UB = Up Bend

Package ^{3/ 4/}

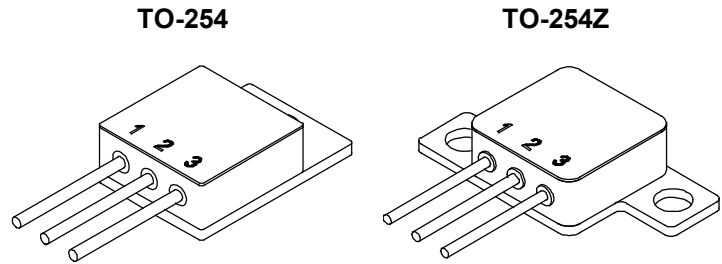
M = TO-254
 Z = TO-254Z

- Features:**
- Rugged poly-Si gate
 - Lowest ON-resistance in the industry
 - Avalanche rated
 - Hermetically Sealed, Isolated Package
 - Low Total Gate Charge
 - Fast Switching
 - TX, TXV, S-Level screening available
 - Improved ($R_{DS(ON)}$, Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	300	V
Gate – Source Voltage	continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	50	A
Max. Instantaneous Drain Current (Tj limited)	@ $T_C = 25^\circ C$ @ $T_C = 125^\circ C$	I_{D2} I_{D3}	50 35	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	50	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} E_{AR}	1500 50	mJ
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.0 (typ.0.75)	$^\circ C / W$

NOTES:

- *Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.
- 1/ For ordering information, price, and availability - contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ For package outlines / lead bending options / pinout configurations - contact factory.
- 4/ Maximum current limited by package configuration
- 5/ Unless otherwise specified, all electrical characteristics @25°C.





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SFF50N30M SFF50N30Z

Electrical Characteristics ^{SI}	Symbol	Min	Typ	Max	Units	
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	300	310	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 35A, T_J = 25^\circ C$	$R_{DS(on)}$	—	50	60	mΩ
	$V_{GS} = 10V, I_D = 35A, T_J = 125^\circ C$		—	110	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1.0mA, T_J = 25^\circ C$	$V_{GS(th)}$	2.5	4.0	5.0	V
	$V_{DS} = V_{GS}, I_D = 1.0mA, T_J = 125^\circ C$		1.5	3.0	—	
	$V_{DS} = V_{GS}, I_D = 1.0mA, T_J = -55^\circ C$		—	5.0	6	
Gate to Source Leakage	$V_{GS} = \pm 20V, T_J = 25^\circ C$	I_{GSS}	—	10	±100	nA
	$V_{GS} = \pm 20V, T_J = 125^\circ C$		—	30	—	
Zero Gate Voltage Drain Current	$V_{DS} = 300V, V_{GS} = 0V, T_J = 25^\circ C$	I_{DSS}	—	0.01	25	μA
	$V_{DS} = 300V, V_{GS} = 0V, T_J = 125^\circ C$		—	5.0	250	
Forward Transconductance	$V_{DS} = 10V, I_D = 35A, T_J = 25^\circ C$	g_{fs}	20	33	—	Mho
Total Gate Charge Gate to Source Charge Gate to Drain Charge	$V_{GS} = 10V$	Q_g Q_{gs} Q_{gd}	—	140	250	nC
	$V_{DS} = 150V$		—	50	—	
	$I_D = 35A$		—	60	—	
Turn on Delay Time Rise Time Turn off Delay Time Fall Time	$V_{GS} = 10V$	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	—	40	50	nsec
	$V_{DS} = 150V$		—	40	50	
	$I_D = 50A$		—	110	125	
	$R_G = 4.0\Omega, pw = 3\mu s$		—	40	50	
Diode Forward Voltage	$I_F = 50A, V_{GS} = 0V$	V_{SD}	—	0.95	1.5	V
Diode Reverse Recovery Time Reverse Recovery Charge	$I_F = 10A, di/dt = 100A/\mu s$	t_{rr} Q_{rr}	—	180	200	nsec
			—	1.3	—	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss} C_{oss} C_{rss}	—	5000	—	pF
Output Capacitance	$V_{DS} = 25V$		—	750	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$		—	145	—	

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

