Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
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SFF116N10M
SFF116N10Z

DESIGNER'S DATA SHEET

116 AMP , 100 Volts, 15 mΩ Avalanche Rated N-channel MOSFET

Part Number / Ordering Information [1/]

SFF116N10 ___ ___ ___

- ___ **Screening** [2/]
  - __ = Not Screened
  - TX = TX Level
  - TXV = TXV Level
  - S = S Level
- ___ **Lead Option** [3/]
  - __ = Straight Leads
  - DB = Down Bend
  - UB = Up Bend
- ___ **Package** [3/ 4/]
  - M = TO-254
  - Z = TO-254Z

Features:

- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	100	V
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC	I_{D1}	55	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC @ T_C = 175ºC	I_{D2} I_{D3}	116 80	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	60	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} E_{AR}	2500 80	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	150	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +175	ºC
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.0 (typ.0.75)	ºC /W

NOTES:

*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.

1/ For ordering information, price, and availability - contact factory.

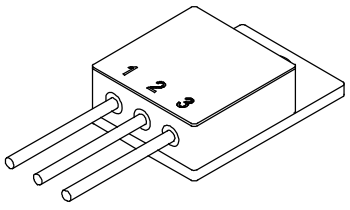
2/ Screening based on MIL-PRF-19500. Screening flows available on request.

3/ For package outlines / lead bending options / pinout configurations - contact factory.

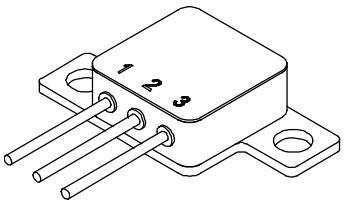
4/ Maximum current limited by package configuration

5/ Unless otherwise specified, all electrical characteristics @25°C.

TO-254



TO-254Z



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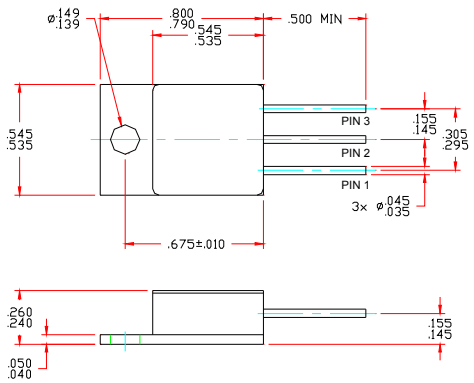
Electrical Characteristics [5/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	BV_{DSS}	100	110	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 50A, Tj= 25°C V_{GS} = 10V, I_D = 50A, Tj=125°C V_{GS} = 10V, I_D = 50A, Tj= 150°C	$R_{DS(on)}$	— — —	10 16 20	15 25 —	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.0mA, Tj= 25°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj= 125°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj= -55°C	$V_{GS(th)}$	3.0 2.0 —	4.5 3.5 5.0	5.0 — 6	V
Gate to Source Leakage	V_{GS} = ±20V, Tj= 25°C V_{GS} = ±20V, Tj= 125°C	I_{GSS}	— —	10 30	±100 —	nA
Zero Gate Voltage Drain Current	V_{DS} = 100V, V_{GS} = 0V, T_j = 25°C V_{DS} = 100V, V_{GS} = 0V, T_j = 125°C V_{DS} = 100V, V_{GS} = 0V, T_j = 175°C	I_{DSS}	— — —	0.01 2.5 25	25 250 —	µA µA µA
Forward Transconductance	V_{DS} = 15V, I_D = 35A, T_j = 25°C	g_{fs}	10	60	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 12V V_{DS} = 35V I_D = 50A	Q_g Q_{gs} Q_{gd}	— — —	125 35 65	250 75 120	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 11V V_{DS} = 50V I_D = 35A R_G = 2.35Ω, pw= 3us	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	39 67 80 67	50 80 100 80	nsec
Diode Forward Voltage	I_F = 35A, V_{GS} = 0V	V_{SD}	—	0.82	1.2	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	I_F = 50A, di/dt = 100A/usec	t_{rr} Q_{rr}	— —	240 0.85	300 —	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	4800 2050 600	— — —	pF

Available Part Numbers:

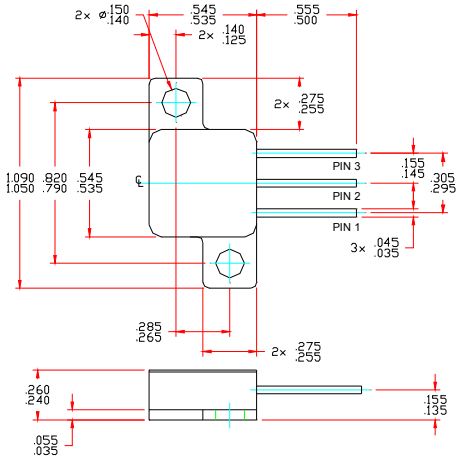
Consult Factory

PIN ASSIGNMENT (Standard)			
Package	**Drain**	**Source**	**Gate**
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

TO254 (M)



TO254Z (Z)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0037B | **DOC**