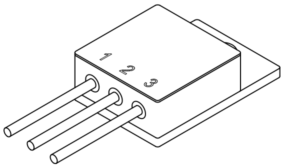
Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

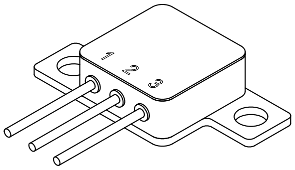
SFF44N50M
SFF44N50Z

DESIGNER'S DATA SHEET

TO-254



TO-254Z



Note 1: maximum current limited by package configuration

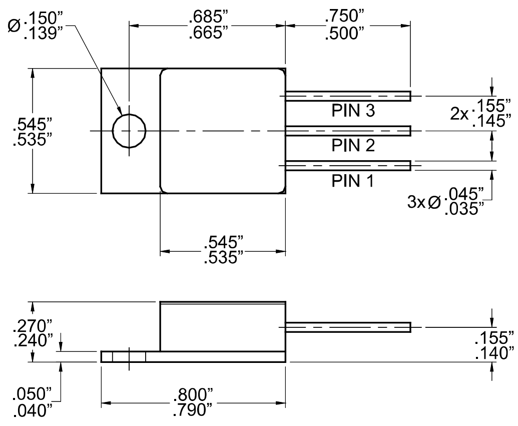
25 AMP , 500 Volts, 110 mΩ Avalanche Rated N-channel MOSFET

Features:

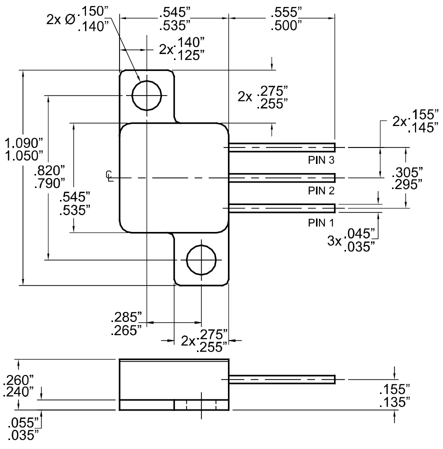
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	500	**V**
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	**V**
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC @ T_C = 125ºC	I_{D1} I_{D2}	25 12	**A**
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC	I_{D3}	35	**A**
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	20	**A**
Single / Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} / E_{AR}	1100 / 1	**mJ**
Total Power Dissipation	@ T_C = 25ºC	P_D	125	**W**
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	**ºC**
Maximum Thermal Resistance	(Junction to Case)	**Rjc**	1.0 (typ.0.75)	**ºC /W**

TO254
(M)



TO254Z
(Z)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: FT0030A**	**DOC**

SFF44N50M
SFF44N50Z

Electrical Characteristics [4]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	500	530	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 20A, Tj= 25°C	$R_{DS(on)}$	—	100	110	mΩ
	V_{GS} = 10V, I_D = 12A, Tj=125°C		—	230	—	
	V_{GS} = 10V, I_D = 20A, Tj= 150°C		—	270	—	
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.8mA, Tj= 25°C	$V_{GS(th)}$	2.1	3.0	3.9	V
	V_{DS} = V_{GS}, I_D = 250μA, Tj= 25°C		—	2.7	—	
	V_{DS} = V_{GS}, I_D = 250μA, Tj= -55°C		—	3.2	—	
	V_{DS} = V_{GS}, I_D = 250μA, Tj= 125°C		—	1.9	—	
Gate to Source Leakage	V_{GS} = ±20V, Tj= 25°C	I_{GSS}	—	10	±100	nA
	V_{GS} = ±20V, Tj= 125°C		—	30	—	
Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V, T_j = 25°C	I_{DSS}	—	0.01	25	μA
	V_{DS} = 500V, V_{GS} = 0V, T_j = 125°C		—	2.0	—	μA
	V_{DS} = 500V, V_{GS} = 0V, T_j = 150°C		—	10	250	μA
Forward Transconductance	V_{DS} = 10V, I_D = 20A, T_j = 25°C	g_{fs}	10	30	—	Mho
Total Gate Charge	V_{GS} = 10V	Q_g	—	175	—	nC
Gate to Source Charge	V_{DS} = 380V	Q_{gs}	—	28	—	
Gate to Drain Charge	I_D = 32A	Q_{gd}	—	80	—	
Turn on Delay Time	V_{GS} = 10V	$t_{d(on)}$	—	30	—	nsec
Rise Time	V_{DS} = 380V	t_r	—	10	—	
Turn off Delay Time	I_D = 32A	$t_{d(off)}$	—	70	—	
Fall Time	R_G = 2.7Ω, pw= 3us	t_f	—	10	—	
Diode Forward Voltage	I_F = 32A, V_{GS} = 0V	V_{SD}	—	1.0	1.5	V
Diode Reverse Recovery Time	I_F = 32A, di/dt = 100A/usec	t_{rr}	—	540	—	nsec
Peak Reverse Recovery Current		$I_{RM(rec)}$	—	45	—	A
Reverse Recovery Charge		Q_{rr}	—	12	—	μC
Input Capacitance	V_{GS} = 0V	C_{iss}	—	4500	—	pF
Output Capacitance	V_{DS} = 25V	C_{oss}	—	540	—	
Reverse Transfer Capacitance	f = 1 MHz	C_{rss}	—	100	—	

NOTES:

* Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines / lead bending options / pinout configurations Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3