



PRELIMINARY

SFF120-28Q

SOLID STATE DEVICES, INC.

14005 Stage Road * Santa Fe Springs, Ca 90670
Phone: (562) 404-4474 * Fax: (562) 404-1773

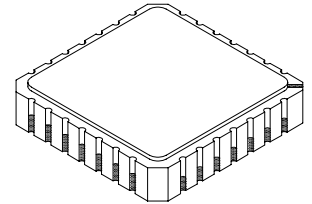
DESIGNER'S DATA SHEET

FEATURES:

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces 4x IRF120 Types in One Package

9.2 AMPS
100 VOLTS
0.35Ω
QUAD N-CHANNEL
POWER MOSFET

28 PIN CLCC



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	100	Volts
Gate to Source Voltage	V _{GS}	±20	Volts
Continuous Drain Current	I _D	9.2	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case (All Four)	R _{θJC}	10	°C/W
Total Device Dissipation		@ TC = 25°C @ TC = 70°C	Watts
		12.5 9.5	

PACKAGE OUTLINE: 28

PIN OUT:

MOSFET 1

DRAIN: 5, 6, 7
GATE: 1
SOURCE: 2, 3, 4

MOSFET 2

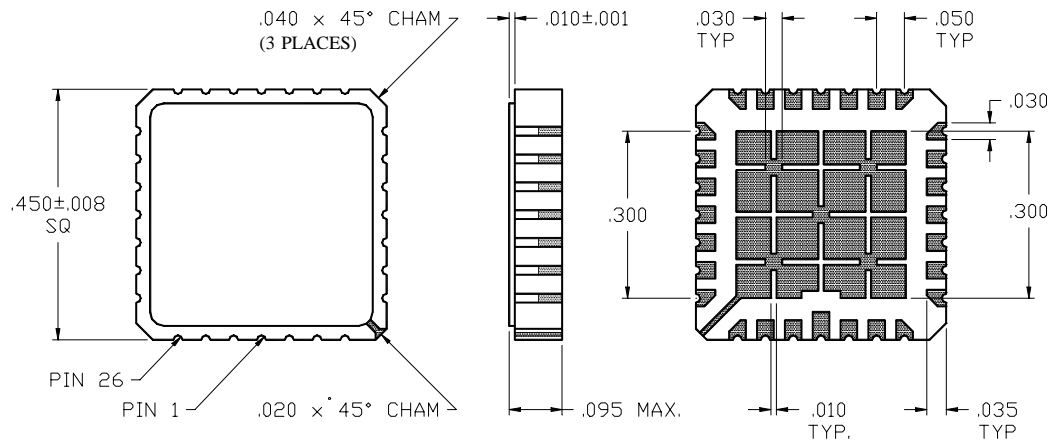
DRAIN: 9, 10, 11
GATE: 8
SOURCE: 12, 13, 14

MOSFET 3

DRAIN: 19, 20, 21
GATE: 15
SOURCE: 16, 17, 18

MOSFET 4

DRAIN: 23, 24, 25
GATE: 22
SOURCE: 26, 27, 28



NOTE: All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)

NOTE: All specifications are subject to change without notification. SCDs for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00225B

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ELECTRICAL CHARACTERISTICS @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 250\mu\text{A}$)		BV_{DSS}	100	-	-	V
Drain to Source ON State Resistance ($V_{GS} = 10\text{ V}$, 60% of Rated ID)		$R_{DS(on)}$	-	-	0.35	Ω
ON State Drain Current ($V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $V_{GS} = 10\text{ V}$)		$I_D(on)$	9.2	-	-	A
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$)		$V_{GS(th)}$	2.0	-	4.0	V
Forward Transconductance ($V_{DS} > I_D(on) \times R_{DS(on)}$ Max, $I_{DS} = 60\%$ rated ID)		g_{fs}	2.7	4.1	-	S(O)
Zero Gate Voltage Drain Current ($V_{DS} = \text{max rated Voltage}$, $V_{GS} = 0\text{V}$) ($V_{DS} = 80\%$ rated V_{DS} , $V_{GS} = 0\text{V}$, $T_A = 125^\circ\text{C}$)		I_{DSS}	-	-	25 250	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V_{GS}	I_{GSS}	-	-	+100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	$V_{GS} = 10\text{ V}$ 80% rated V_{DS} 60% rated ID	Q_g Q_{gs} Q_{gd}	-	10.7 2.9 5.1	16 4.4 7.7	nC
Turn on Delay Time Rise Time Turn off DELAY Time Fall Time	$V_{DD} = 50\%$ rated V_{DS} 50% rated ID $R_G = 18\ \Omega$	$t_d(on)$ t_r $t_d(off)$ t_f	-	13 30 19 20	20 45 29 30	nsec
Diode Forward Voltage ($I_S = \text{rated } I_D$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$)		V_{SD}	-	-	2.5	V
Diode Reverse Recovery Time Reverse Recovery Charge	$T_J = 25^\circ\text{C}$ $I_F = \text{rated } I_D$ $di/dt = 100\text{A}/\mu\text{sec}$	t_{rr} Q_{RR}	55 0.25	140 0.65	260 1.3	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{GS} = 0\text{ Volts}$ $V_{DS} = 25\text{ Volts}$ $f = 1\text{ MHz}$	C_{iss} C_{oss} C_{rss}	-	350 130 36	- - -	pF

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

NOTES: