



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
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SFR9130S.5

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFR9130 S.5



Screening ^{2/}

— = Not Screened

TX = TX Level

TXV = TXV Level

S = S Level

Package ^{3/}

S.5 = SMD.5

RADIATION TOLERANT
26 AMP, 100 Volts, 90 mΩ
Avalanche Rated P-MOSFET

Features:

- Rugged Trench Technology
- Low ON-resistance: 57mΩ typ
- Radiation tolerant: less than 0.5V typical gate threshold shift @ TID= 100kRAD
- SEU and SEGR resistant to LET 38
- Avalanche rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge, Fast Switching
- Replacement for IRF9130 types
- TX, TXV, S-Level screening available

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V _{DSS}	-100	V
Gate – Source Voltage, continuous		V _{GS}	±15	V
Gate – Source Voltage, transient			±25	
Max. Continuous Drain Current (package limited)	@ T _C = 25°C	I _{D1}	26	A
	@ T _C = 100°C	I _{D2}	17	
Max. Avalanche current	@ L= 5.0 mH	I _{AR}	26	A
Max. Continuous Drain Current (Tj limited)	@ Tj= 150 °C	I _{DM}	27	A
Single Pulse Avalanche Energy	@ L= 5.0 mH	E _{AS}	300	mJ
Total Power Dissipation	@ T _C = 25°C	P _D	83	W
Operating & Storage Temperature		T _{OP} & T _{STG}	-55 to +150	°C
Maximum Thermal Resistance (Junction to Case)		R _{θJC}	1.5 (typ 0.5)	°C/W

NOTES:

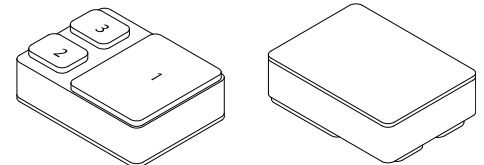
*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @25°C.

SMD.5 (S.5)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0045B

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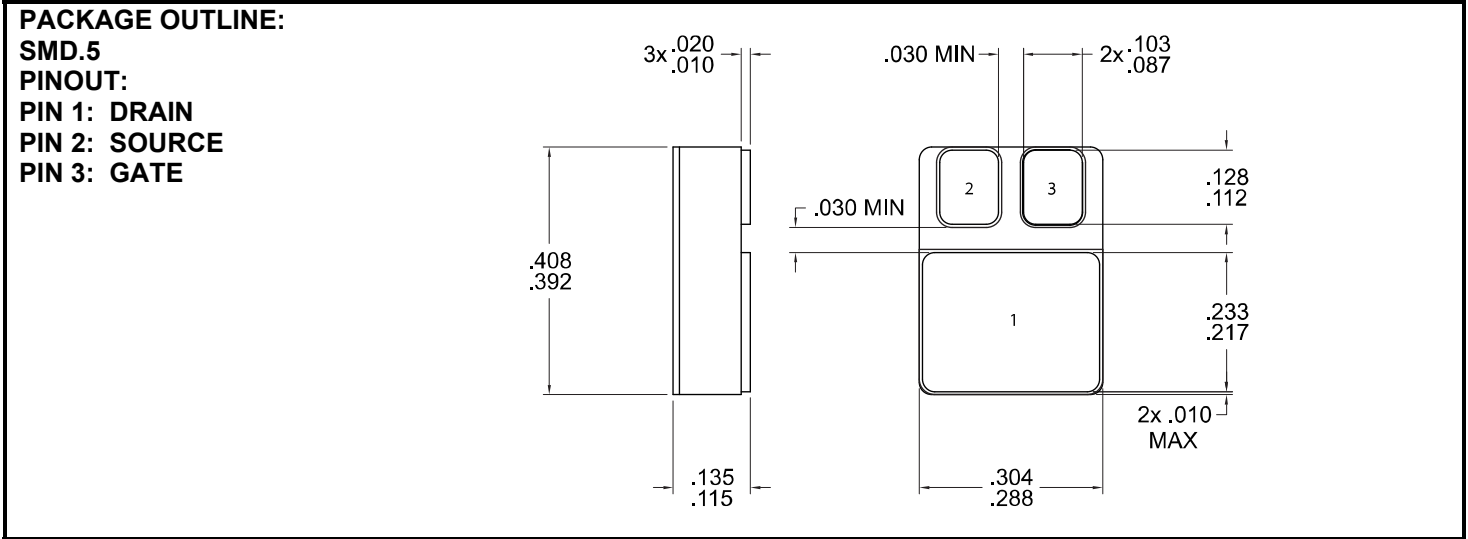


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Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 0.25 \text{ mA}$	BV_{DSS}	-100	-115	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 13A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 13A, T_j = 125^\circ C$	$R_{DS(on)}$	—	57 100	90 —	mΩ
Gate Threshold Voltage	$V_{DS} = 5V, I_D = 250\mu A, T_j = 25^\circ C$ $V_{DS} = 5V, I_D = 250\mu A, T_j = 125^\circ C$ $V_{DS} = 5V, I_D = 250\mu A, T_j = -55^\circ C$	$V_{GS(th)}$	-2.0 -1.0 —	-3.2 -2.5 -3.6	-4.0 — -5.0	V
Gate to Source Leakage	$V_{GS} = \pm 15V, T_j = 25^\circ C$ $V_{GS} = \pm 15V, T_j = 125^\circ C$	I_{GSS}	—	1 10	± 50 ± 200	nA
Zero Gate Voltage Drain Current	$V_{DS} = -100V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = -100V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	—	0.01 5	10 250	μA μA
Forward Transconductance	$V_{DS} = 10V, I_D = 10A, T_j = 25^\circ C$	g_{fs}	—	15	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	23	40	nC
Gate to Source Charge	$V_{DS} = 80V$	Q_{gs}	—	8.5	—	
Gate to Drain Charge	$I_D = 10A$	Q_{gd}	—	5	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	65	100	nsec
Rise Time	$V_{DS} = 50V$	t_r	—	25	50	
Turn off Delay Time	$I_D = 10A$	$t_{d(off)}$	—	75	150	
Fall Time	$R_G = 10\Omega$	t_f	—	30	50	
Diode Forward Voltage	$I_F = 10A, V_{GS} = 0V$	V_{SD}	—	0.85	1.5	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr}	—	60	85	nsec
Peak Reverse Recovery Current		Q_{rr}	—	150	—	nC
Reverse Recovery Charge						
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	3500	4000	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	300	400	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	110	200	



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