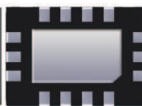


# LOW JITTER PIN CONFIGURABLE LVDS-CMOS DUAL OUTPUT ULTRA MINIATURE PURE SILICON™ CLOCK OSCILLATOR

ASEMDLC



Life Size   
3.2 x 2.5 x 0.85 mm

**ASEMDLC**

Moisture Sensitivity Level – MSL 1



**RoHS**  
Compliant

## FEATURES:

- Ultra Miniature Pure Silicon™ Clock Oscillator
- Pin Configurable LVDS-CMOS Dual output
- Low Jitter (Period Jitter RMS 2.5ps typical)
- Low Integrated Phase Jitter 2ps max
- Tight Stability +/-10ppm -40 to +85C
- Excellent Shock & Vibration Immunity

## APPLICATIONS:

- Consumer Electronics
- Storage Area Networks
- SATA, SAS, Fibre Channel
- Passive Optical Networks
- EPON, 10G-EPON, GPON, 10G-PON
- Ethernet
- 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express

Low Jitter  
Pin Configurable  
LVDS-CMOS Dual Output  
3G MEMS

## STANDARD SPECIFICATIONS:

### Pre-programmed Output Frequency Configuration

Ordering Info	Freq (MHz)	Freq Select Bits [FS2, FS1, FS0] – Default is [111]							
		000	001	010	011	100	101	110	<b>111</b>
Frequency Configuration 1	f <sub>OUT1</sub> (LVDS)	74.25	74.25	156.25	150	125	125	100	<b>100</b>
	f <sub>OUT2</sub> (CMOS)	27	33.333	125	125	25	50	50	<b>75</b>
Custom Configuration	f <sub>OUT1</sub>	Contact Abracon for customized configurations							

Frequency select bits [FS2, FS1, FS0] are weakly tied high so if left floated, the default setting will be [111] and the device will output the associated frequency highlighted in Bold. If other frequency combinations are required, please contact Abracon for customized configuration. Please see the configurable frequency range in the section 2.0

### Key Electrical Specifications

Parameters	Minimum	Typical	Maximum	Units	Notes	
Configurable frequency range	LVDS	10	----	460	MHz	Commercial, Industrial temp range
	CMOS	10	----	170		
Operating Temperature	-20	----	+70	°C	See options	
Storage Temperature	-55	----	+150	°C		
Overall Frequency Stability* <sup>1</sup>	-50	----	+50	ppm	See options	
Supply Voltage (V <sub>dd</sub> )	+2.25	----	+3.6	V		
Startup Time	----	----	5	ms		
Enable Time	----	----	20	ns		
Disable Time	----	----	5	ns		
Disable Current	----	21	23	mA		
Tri-state Function (Standby/Disable)	"1" (VIH ≥ 0.75*V <sub>dd</sub> ) or Open: Oscillation "0" (VIL < 0.25*V <sub>dd</sub> ) : Hi Z			V	40kΩ pull-up resistor embedded	
Aging	-5.0	----	+5.0	ppm	First year	
Supply Current (I <sub>dd</sub> )	----	49	----	mA	LVDS output: RL=100Ω, F01=125MHz CMOS output: CL=15pF, F02=75MHz	

\*1. Frequency stability includes frequency variations due to initial tolerance, temp. and power supply voltage

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CERTIFIED

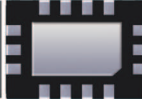


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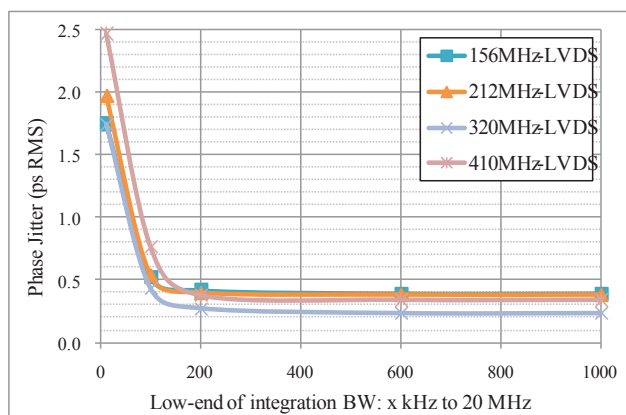


## Key Electrical Specifications (continued)

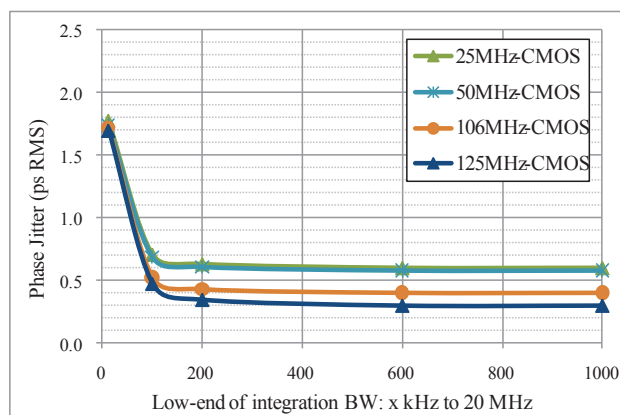
LVDS Output (Fout1)						
Output Offset Voltage		1.125	-----	1.40	V	RL=100 Ω, Differential
Delta Offset Voltage		-----	-----	50	mV	
Peak to Peak Output Swing		-----	350	-----	mV	Single-Ended
Rise Time	Tr	-----	200	-----	ps	RL=50 Ω, CL=2pF
Fall Time	Tf	-----	200	-----	ps	20%/80%*VDD
Duty Cycle		48	-----	52	%	Differential
Period Jitter RMS (J <sub>PER</sub> )		-----	2.5	-----	ps	F01= 125MHz
Integrated Phase Jitter (J <sub>PH</sub> )		-----	0.28	2	ps	200kHz ~ 20MHz, 156.25MHz
		-----	0.40	2		100kHz ~ 20MHz, 156.25MHz
		-----	1.70	2		12kHz ~ 20MHz, 156.25MHz

CMOS Output (Fout2)						
Output Logic Level	V <sub>OH</sub>	0.9*V <sub>dd</sub>	-----	-----	V	I=±6mA
	V <sub>OL</sub>	-----	-----	0.1*V <sub>dd</sub>		
Rise Time	Tr	-----	1.1	2.0	ns	CL=15pF
Fall Time	Tf	-----	1.3	2.0	ns	20%/80%*VDD
Duty Cycle		45	-----	55	%	
Period Jitter RMS (J <sub>PER</sub> )		-----	3.0	-----	ps	F01= 125MHz
Integrated Phase Jitter (J <sub>PH</sub> )		-----	0.30	2	ps	200kHz ~ 20MHz, 125MHz
		-----	0.38	2		100kHz ~ 20MHz, 125MHz
		-----	1.70	2		12kHz ~ 20MHz, 125MHz

## PHASE JITTER



LVDS



CMOS

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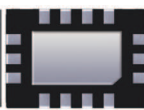


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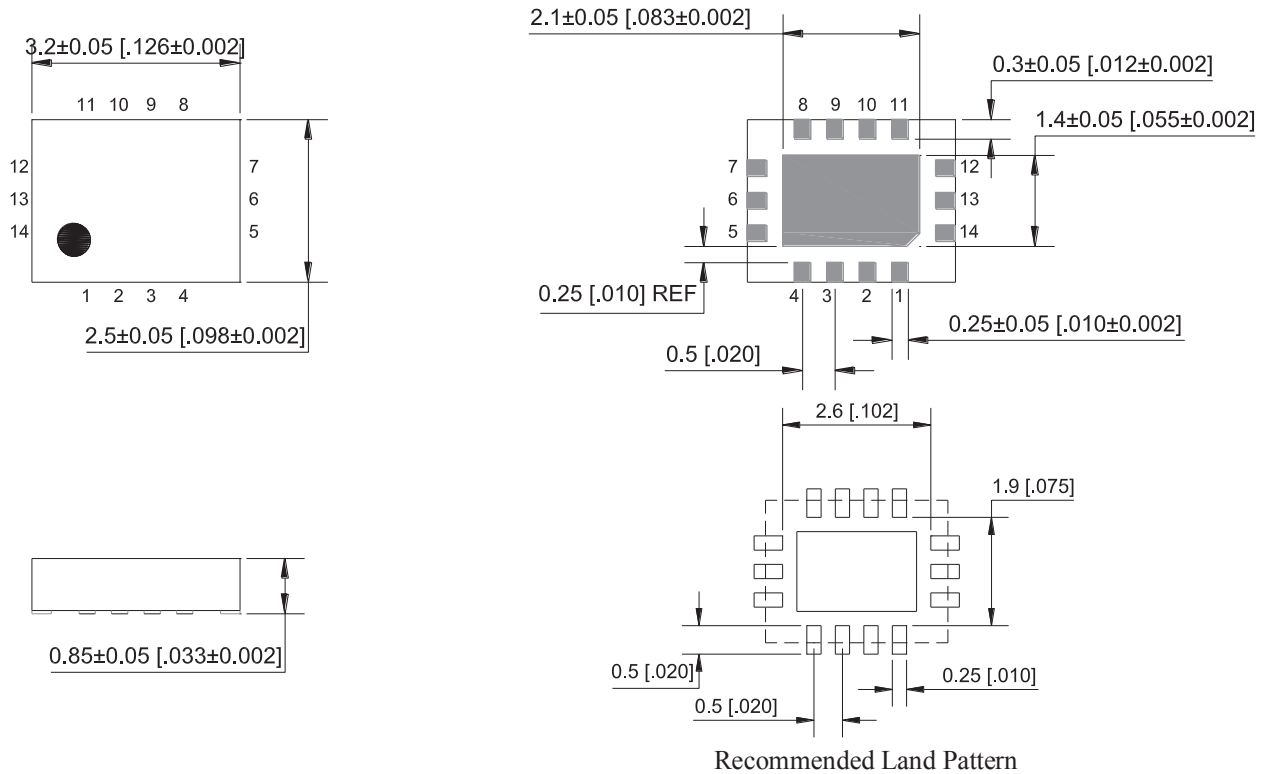


Life Size   
 3.2 x 2.5 x 0.85 mm

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## MECHANICAL DIMENSIONS



Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables (tri-state) them when low
2	NC	NA	Leave unconnected or grounded
3	OS0	I	Least significant bit for output drive strength selection for CMOS
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Middle bit for frequency selection
7	FS2	I	Most significant bit for frequency selection
8	Output1+	O	Positive LVDS Output 1
9	Output1-	O	Negative LVDS Output 1
10	OS1	I	Middle bit for output drive strength selection for CMOS
11	Output 2	O	CMOS output
12	VDD2	Power	Power Supply 2 for CMOS Output
13	VDD	Power	Power Supply
14	OS2	I	Most significant bit for output drive strength selection for CMOS

Dimensions: mm (inches)

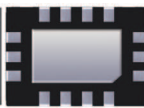
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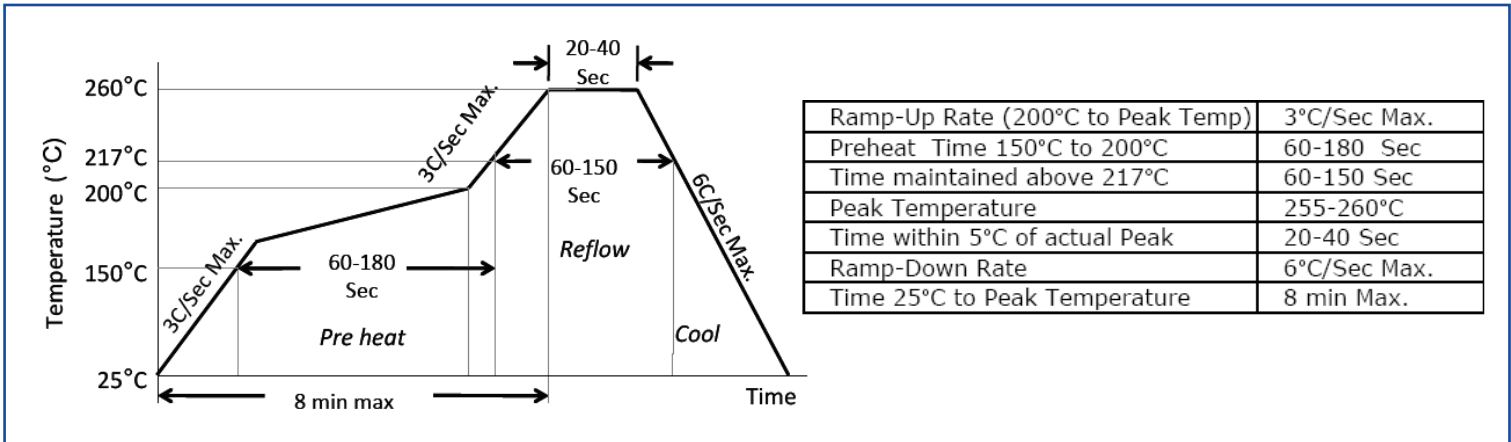


Life Size  
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ASEMDLC

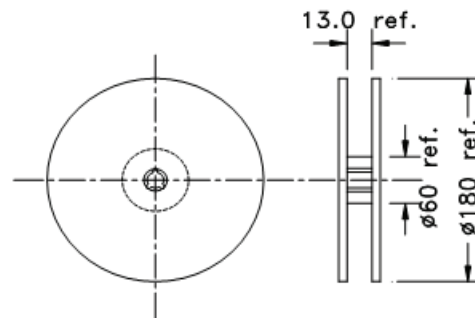
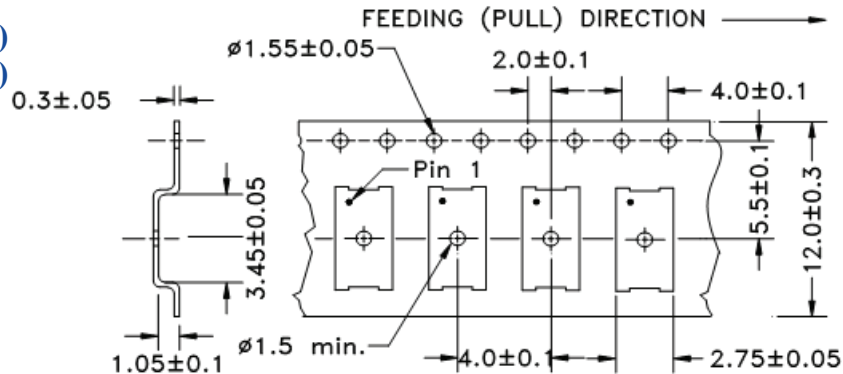


## REFLOW PROFILE

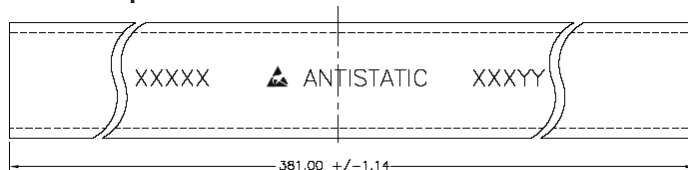


## REFLOW PROFILE

T= 1,000pcs/reel (D=180mm)  
T3= 3,000pcs/reel (D=180mm)  
T5= 5,000pcs/reel (D=330mm)



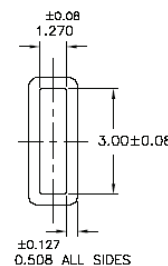
Tube: 110 pcs/tube



Unit orientation in tube:



Dimensions: mm



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Life Size   
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## ➤ ABSOLUTE MAXIMUM RATINGS

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V <sub>dd</sub> +0.3	V	
Junction Temp.	-----	+150	°C	
Storage Temp.	-55	+150	°C	
Soldering Temp.	-----	+260	°C	40sec max
ESD			V	
HBM		4,000		
MM		400		
CDM		1,500		

## ➤ OPTIONS AND PART IDENTIFICATION:

(left blank if standard)

ASEMDLC -  -  -

Operating Temp.
Blank: -20°C ~ +70°C
L: -40°C ~ +85°C

Overall Freq. Stability
Blank: ±50ppm
Y: ±10ppm
R: ±25 ppm

Packaging
Blank: Tube (110pcs / Tube)
T: Tape & Reel (1kpcs / reel)
T3: Tape & Reel (3kpcs / reel)
T5: Tape & Reel (5kpcs / reel)

Frequency Combination	Freq (MHz)	Freq Select Bits [FS2, FS1, FS0] – Default is [111]							
		000	001	010	011	100	101	110	111
<b>Standard Configuration</b>	f <sub>OUT1</sub> (LVDS)	74.25	74.25	156.25	150	125	125	100	<b>100</b>
	f <sub>OUT2</sub> (CMOS)	27	33.333	125	125	25	50	50	<b>75</b>
Custom Configuration	f <sub>OUT1</sub>	Contact Abracon for customized configurations							
	f <sub>OUT2</sub>								

Default condition: Frequency select bits [FS2, FS1, FS0] are all left floated. FS2, FS1, FS0 are pulled high [111]  
Frequency combination and default frequency is customized upon request. Please contact Abracon for the frequency combinations.

## ➤ CONFIGURABLE CMOS OUTPUT STRENGTH (TR/TF)

CMOS Output (Tr/Tf) are configurable by the control pins OS2, OS1 and OS0. The combinations are described in the table below.

	Output Drive Strength Bits [OS2, OS1, OS0] - Default [111]							
	000	001	010	011	100	101	110	111
Tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	<b>1.1</b>
Tf (ns)	2.5	2.4	2.4	2	1.8	1.6	1.3	<b>1.3</b>

