Silicon-BasedTechnology

Ultra High-Speed PBSRAM

64K× 64 SYNCHRONOUS PIPELINED-BURST CMOS SRAM

Preliminary

FEATURES:

- ■Single 3.3V -5% and +10% power supply
- ■Fast clock access time: 3.75ns/133MHz , 4ns/125MHz , 5ns/100MHz
- ■Two clocked chip enable/one clocked chip disable operation
- ■LVTTL compatible outputs
- ■128-pin PQFP and TQFP package
- ■Synchronous pipelined-operation
- ■Internally self-timed WRITE cycle
- ■BYTE WRITE and GLOBAL WRITE control
- ■WRITE pass-through capability
- ■Burst control pin (interleaved or linear burst)
- ■ZZ snooze mode control

GENERAL DESCRIPTION:

The SB61S64K64A is a series of 4,194,304-bit synchronous pipelined-burst CMOS SRAM organized as 65,536 words by 64 bits and is fabricated by using advanced high-performance and high-reliability 3P2M CMOS technology with memory cell using 4 transistors and two high-value resistors.

The SB61S64K64A integrates 65,536× 64 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK) . The synchronous inputs include addresses, data inputs, address-pipelining chip enable ($\overline{CE}$) , burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$) , byte-write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BW5}$, $\overline{BW6}$, $\overline{BW7}$, $\overline{BW8}$ and $\overline{BWE}$), and global write enable($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the data outputs (I/O) enabled by $\overline{OE}$. Addresses and chip enables are registered with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$) . Addresses, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four-bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written, in which $\overline{BW1}$ controls I/O1-I/O8；$\overline{BW2}$ controls I/O9-I/O16；$\overline{BW3}$ controls I/O17-I/O24；$\overline{BW4}$ controls I/O25-I/O32；$\overline{BW5}$ controls I/O33-I/O40；$\overline{BW6}$ controls I/O41-I/O48；$\overline{BW7}$ controls I/O49-I/O56；$\overline{BW8}$ controls I/O57-I/O64. $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BW5}$, $\overline{BW6}$, $\overline{BW7}$ and $\overline{BW8}$ can be active only with $\overline{BWE}$ being LOW, and $\overline{GW}$ being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the immediate next READ cycle. This device also incorporates pipelined enable circuit for easy depth expansion without system performance-penalty.

The SB61S64K64A operates with a +3.3V power supply. All inputs and outputs are LVTTL-compatible. The device is ideally suited for applications in high-performance PC systems using K6-2, K-6 ⅢCPUs and for systems that can be benefited from a wide synchronous data bus.

ORDER INFORMATION:

PART NO.	Clock Access Time /Clock Frequency	PACKAGE
SB61S64K64A-5	5ns/100MHz	128-Pins PQFP/TQFP
SB61S64K64A-4	4ns/125MHz	128-Pins PQFP/TQFP
SB61S64K64A-3.75	3.75ns/133MHz	128-Pins PQFP/TQFP

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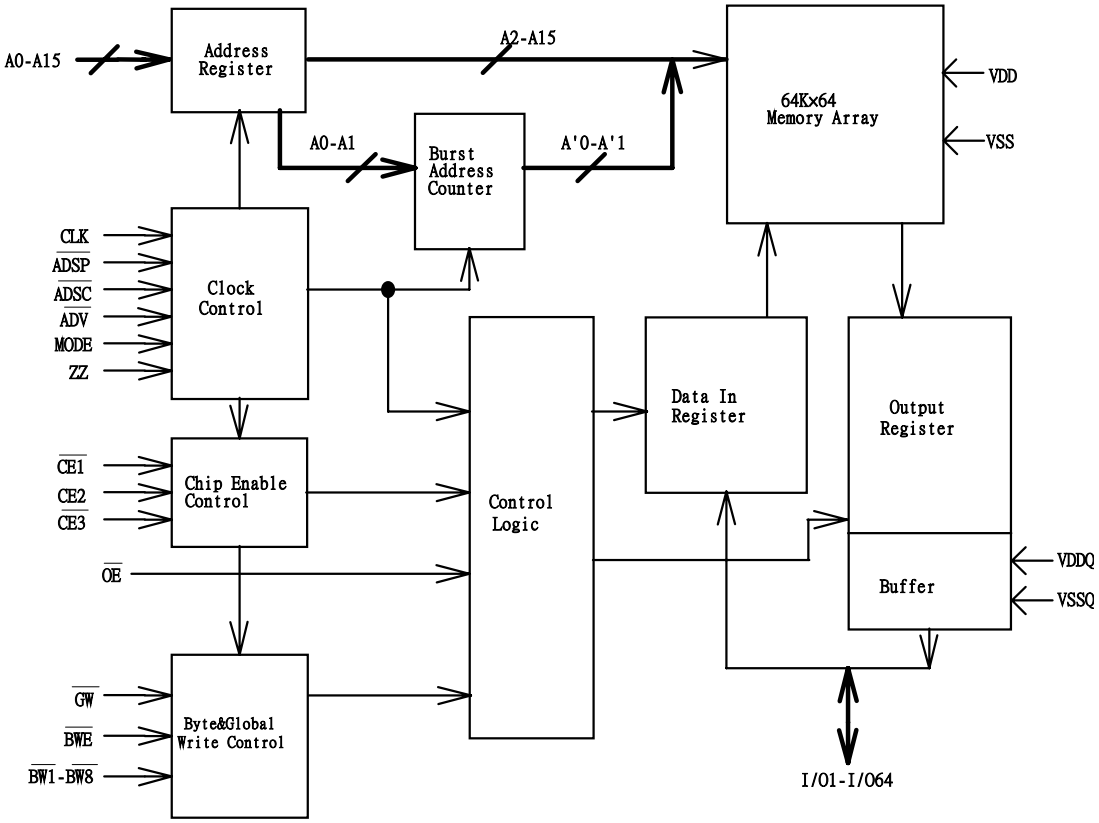
FUNCTIONAL BLOCK DIAGRAM:



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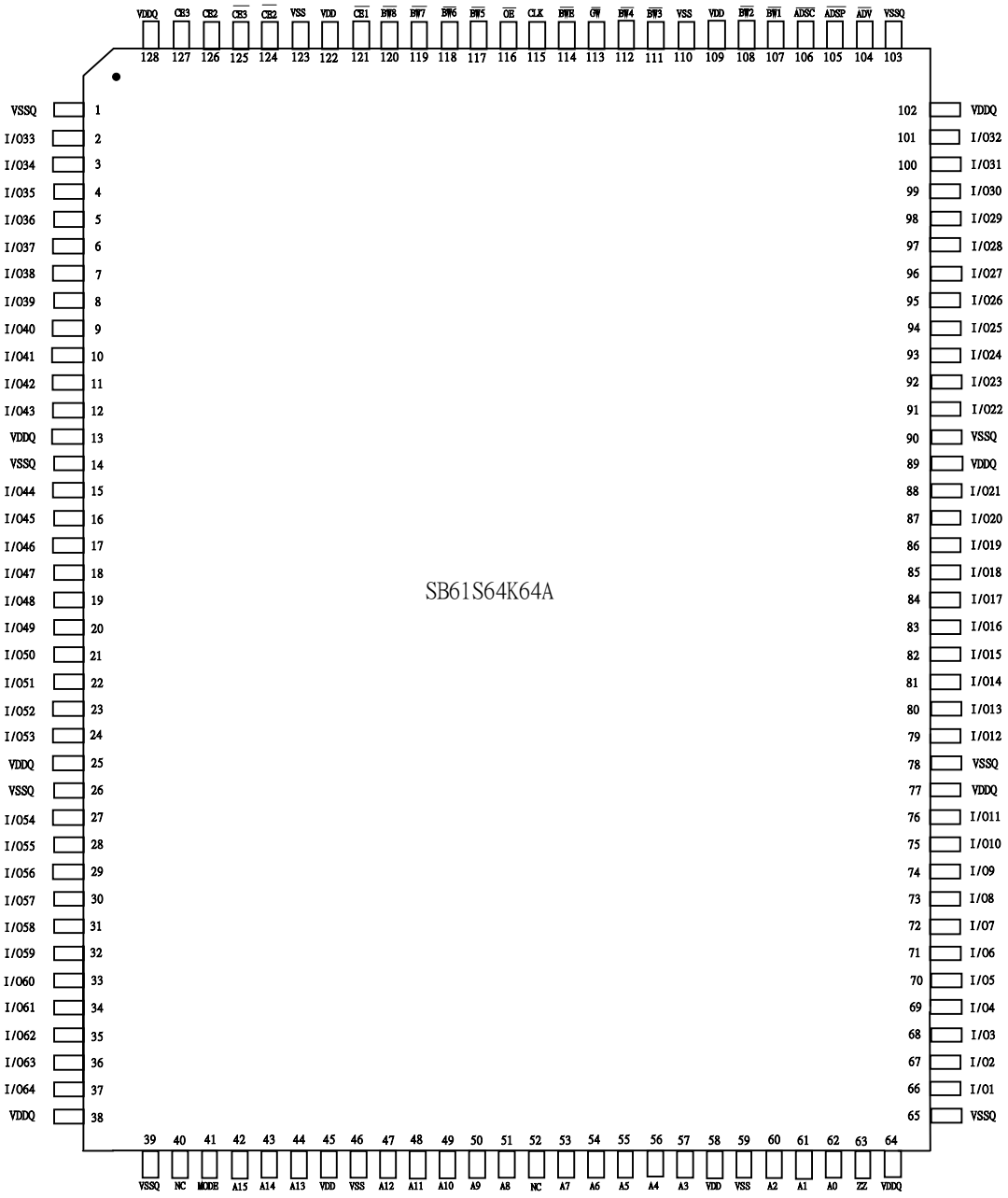
PIN CONFIGURATION:



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PIN DESCRIPTION:

QFP PIN	SYMBOL	DESCRIPTION
42-44,47-51, 53-57,60-62	A0-A15	Synchronous Address Inputs
115	CLK	Clock Input
105	$\overline{ADSP}$	Synchronous Address Status Processor Input
106	$\overline{ADSC}$	Synchronous Address Status Control Input
104	$\overline{ADV}$	Synchronous Burst Address Advance Input
121,124,125, 126,127	$\overline{CE1}$,CE2,$\overline{CE3}$,CE2,CE3	Synchronous Chip Enable Inputs
116	$\overline{OE}$	Asynchronous Output Enable Input
113	$\overline{GW}$	Synchronous Global Write Enable Input
114	$\overline{BWE}$	Synchronous Byte Write Enable Input
107,108, 111,112, 117-120	$\overline{BW1}$ -$\overline{BW8}$	Synchronous Byte Write Input
41	MODE	Asynchronous Burst Sequence Select Input(Low for linear burst ; High for interleaved burst)
63	ZZ	Asynchronous Power Down State Input (Snooze Enable)
66-76,79-88, 91-101,2-12, 15-24,27-37	I/O1-I/O64	Synchronous Data Inputs , Synchronous/Asynchronous Data Outputs
45,58,109, 122	VDD	Power Supply
46,59,110, 123	VSS	Ground
13,25,38,64, 77,89,102, 128	VDDQ	Output Buffer Power Supply
1,14,26,39, 65,78,90,103	VSSQ	Output Buffer Ground
40,52	NC	No Connection

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TRUTH TABLE:

OPERATION	ADDRESS USED	$\overline{CE1}$	$\overline{CE2}$	CE2	$\overline{CE3}$	CE3	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	X	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	X	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	X	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	X	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	X	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	X	X	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	X	H	X	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	X	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	X	X	H	H	L	X	L-H	D

Notes:1. X means "don't care." H means logic HIGH. Lmeans logic LOW. WRITE=L means that ($\overline{BWE}$ + $\overline{BW1}$ * $\overline{BW2}$ * $\overline{BW3}$ * $\overline{BW4}$ * $\overline{BW5}$ * $\overline{BW6}$ * $\overline{BW7}$ * $\overline{BW8}$) * $\overline{GW}$ is equal to LOW. WRITE =H means that ($\overline{BWE}$ + $\overline{BW1}$ * $\overline{BW2}$ * $\overline{BW3}$ * $\overline{BW4}$ * $\overline{BW5}$ * $\overline{BW6}$ * $\overline{BW7}$ * $\overline{BW8}$) * $\overline{GW}$ is equal to HIGH.

2. $\overline{BW1}$ enables write to I/O1-I/O8 ; $\overline{BW2}$ enables write to I/O9-I/O16 ; $\overline{BW3}$ enables write to I/O17-I/O24 ; $\overline{BW4}$ enables write to I/O25-I/O32 ; $\overline{BW5}$ enables write to I/O33-I/O40 ; $\overline{BW6}$ enables write to I/O41-I/O48 ; $\overline{BW7}$ enables write to I/O49-I/O56 ; $\overline{BW8}$ enables write to I/O57-I/O64.

3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

4. Suspending burst generates the wait cycle.

5. For a write operation following a read operation , $\overline{OE}$ must be high before the input data required setup time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.

6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

7. $\overline{ADSP}$ =LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR WRITE:

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	$\overline{BW5}$	$\overline{BW6}$	$\overline{BW7}$	$\overline{BW8}$
READ	H	H	X	X	X	X	X	X	X	X
READ	H	L	H	H	H	H	H	H	H	H
WRITE one byte	H	L	L	H	H	H	H	H	H	H
WRITE all bytes	H	L	L	L	L	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X	X	X	X	X

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INTERLEAVED-BURST ADDRESS TABLE(MODE=NC/VDD):

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

LINEAR-BURST ADDRESS TABLE(MODE=GND) :

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

PASS-THROUGH TRUTH TABLE:

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWN}$	OPERATION	$\overline{CE}$	$\overline{BWN}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle,all bytes Address=A(n-1). data=D(n-1)	All L[2,3]	READ cycle. Register A(n). Q=D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle,all bytes Address=A(n-1). data=D(n-1)	All L[2,3]	READ cycle. Register A(n). Q=HIGH-Z	L	H	H	Read D(n)
Initiate WRITE cycle,one byte Address=A(n-1). data=D(n-1)	One L[2,3]	READ cycle. Register A(n). Q=D(n-1) for one byte	L	H	L	Read D(n)
Initiate WRITE cycle,all bytes Address=A(n-1). data=D(n-1)	All L[2]	Deselect cycle Q=HIGH-Z	H	X	X	No carry-over from previous cycle

Note：1. The previous cycle may be any cycle (non-burst,burst,or wait)and the next cycle is read cycle(non-burst,burst,or wait).

2. $\overline{BWE}$ is LOW for individual byte WRITE.

3. $\overline{GW}$ is LOW, yielding the same result for all-byte WRITE operation.

ABSOLUTE MAXIMUM RATINGS:

PARAMETERS	RATING	UNIT
Voltage on Vcc Supply Relative to Vss	-0.5 to +4.6	V
V_{IN}	-0.5 to +6	V
Storage Temperature(plastic)	-55 to +150	℃
Junction Temperature	+150	℃
Power Dissipation	1.6	W
Short Circuit Output Current	100	mA

Note：Stresses greater than those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and the functional operation of the device at these or any other conditions above those indicated in this specification is not implied.Exposure to the absolute maximum rating conditions for extended periods may affect device reliability, resulting in device performance degradation.

DC ELECTRICAL CHARACTERISTICS:

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(V_{DD} = 3.3V-5% and + 10% , T_A = 0℃ to 70℃)

PARAMETERS	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTES
Input High(Logic 1) Voltage	V_{IH}		2.0	5.5	V	1,2
Input Low(Logic 0) Voltage	V_{IL}		-0.3	0.8	V	1,2
Input Leakage Current	IL_I	OV≦V_{IN}≦VDD	-1	1	μA	14
Output Leakage Current	IL_O	Output(s) disabled. OV≦V_{out}≦VDD	-1	1	μA	
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH}= -4mA	2.4	-	V	1,11
Output Low Voltage	V_{OL}	I_{OL}= 8mA	-	0.4	V	1,11
Supply Voltage	VDD		3.1	3.6	V	1
I/O Supply Voltage(3.3V I/O)	VDDQ		3.1	3.6	V	1
I/O Supply Voltage(2.5V I/O)	VDDQ		2.4	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	A-3.75	A-4	A-5	UNIT	NOTE
Power Supply Current Operating	Device selected：all inputs≦V_{IL} or ≧ V_{IH} cycle time≧t_{KC} MIN；VDD=MAX；outputs open	IDD	180	440	400	360	mA	3,12, 13
Power Supply Current Idle	Device selected：$\overline{ADSC}$,$\overline{ADSP}$,$\overline{ADV}$, $\overline{GW}$,$\overline{BWE}$ ≧V_{IH}, all other inputs≦V_{IL} or ≧V_{IH} VDD = MAX； cycle time≧t_{KC}MIN；outputs open	I_{SB1}	30	80	70	60	mA	12,13
CMOS Standby	Device selected：VDD = MAX； all inputs≦Vss + 0.2 or≧VDD -0.2； all inputs static；CLK frequency = 0	I_{SB2}	2	20	20	20	mA	12,13
TTL Standby	Device selected：all inputs≦V_{IL} or ≧V_{IH} all inputs static；VDD = MAX； CLK frequency = 0	I_{SB3}	15	40	40	40	mA	12,13
Clock Running	Device selected： all inputs≦V_{IL} or ≧V_{IH}；VDD = MAX； CLK cycle time≧t_{KC} MIN	I_{SB4}	30	80	70	60	mA	12,13
Power-Down Mode Current	ZZ≧VDD - 0.2	I_{ZZ}	1	10	10	10	mA	12,13

CAPACITANCE(T_A = 25℃, f=1MHz) :

PARAMETERS	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance	C_{IN}	3	4	pF	4
Input/Output Capacitance	$C_{I/O}$	6	7	pF	4

AC ELECTRICAL CHARACTERISTICS:
(VDD = 3.3V-5% and + 10%,T_A=0℃ to 70℃)

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PARAMETERS	SYM	A-3.5/ 133MHz		A-4/ 125MHz		A-5/ 100MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock cycle time	t_{KC}	7.5	-	8	-	10	-	ns	-
Clock HIGH time	t_{KH}	3	-	3.5	-	4	-	ns	-
Clock LOW time	t_{KL}	3	-	3.5	-	4	-	ns	-
Output Times									
Clock to output valid	t_{KQ}	-	3.75	-	4	-	5	ns	-
Clock to output invalid	t_{KQX}	2	-	2	-	2	-	ns	-
Clock to output in Low-Z	t_{KQLZ}	2	-	2	-	3	-	ns	6,7
Clock to output in High-Z	t_{KQHZ}	-	3.75	-	4	-	5	ns	6,7
$\overline{OE}$ to output valid	t_{OEQ}	-	3.75	-	4	-	5	ns	9
$\overline{OE}$ to output in Low-Z	t_{OELZ}	0	-	0	-	0	-	ns	6,7
$\overline{OE}$ to output in High-Z	t_{OEHZ}	-	3	-	3	-	4	ns	6,7
Setup Times									
Address setup	t_{AS}	2.0	-	2.2	-	2.5	-	ns	10
Address status setup	t_{ADSS}	2.0	-	2.2	-	2.5	-	ns	10
Address advance setup	t_{ADVS}	2.0	-	2.2	-	2.5	-	ns	10
Write setup	t_{WS}	2.0	-	2.2	-	2.5	-	ns	10
Data setup	t_{DS}	2.0	-	2.2	-	2.5	-	ns	10
Chip enable setup	t_{CES}	2.0	-	2.2	-	2.5	-	ns	10
Hold Times									
Address hold	t_{AH}	0.5	-	0.5	-	0.5	-	ns	10
Address status hold	t_{ADSH}	0.5	-	0.5	-	0.5	-	ns	10
Address advance hold	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns	10
Write hold	t_{WH}	0.5	-	0.5	-	0.5	-	ns	10
Data hold	t_{DH}	0.5	-	0.5	-	0.5	-	ns	10
Chip enable hold	t_{CEH}	0.5	-	0.5	-	0.5	-	ns	10
ZZ standby	t_{ZZS}	-	100	-	100	-	100	ns	16
ZZ recovery	t_{ZZREC}	100	-	100	-	100	-	ns	16

AC TEST CONDITIONS:

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS:

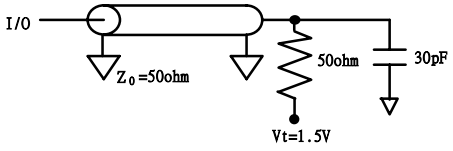

Fig.1 Output load equivalent

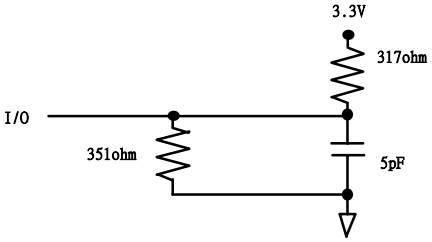

Fig.2 Output load equivalent

NOTES:

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1. All voltages are referenced to Vss.
2. Overshoot： $V_{IH} \leqq +0.6V$ for $t \leqq t_{KC}/2$.
   Undershoot： $V_{IH} \leqq -2.0V$ for $t \leqq t_{KC}/2$.
3. IDD is given without output current.IDD increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading shown in Fig.1 unless otherwise noted.
6. Output loading is specified with C_L=5pF shown in Fig.2.
7. At any given temperature and voltage condition , t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
8. A READ cycle is defined when all byte-write enables are HIGH or $\overline{ADSP}$ is LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. $\overline{OE}$ is a "don't care" when a byte-write enable is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold times , except for "don't care" as defined in the truth table.
11. AC I/O curves are available upon request.
12. "Device Deselected" means the device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means the device is active.
13. Typical values are measured at 3.3V, 25℃ and 20ns cycle time.
14. Capacitance derating applies to capacitance different from the load capacitance shown in Fig.1.
15. Capacitance derating applies to capacitance different from the load capacitance shown in Fig.1.
16. The assertion-off ZZ allows the SRAM to enter a low power state than when deselected within the time specified.

TIMING WAVEFORMS：

READ CYCLE

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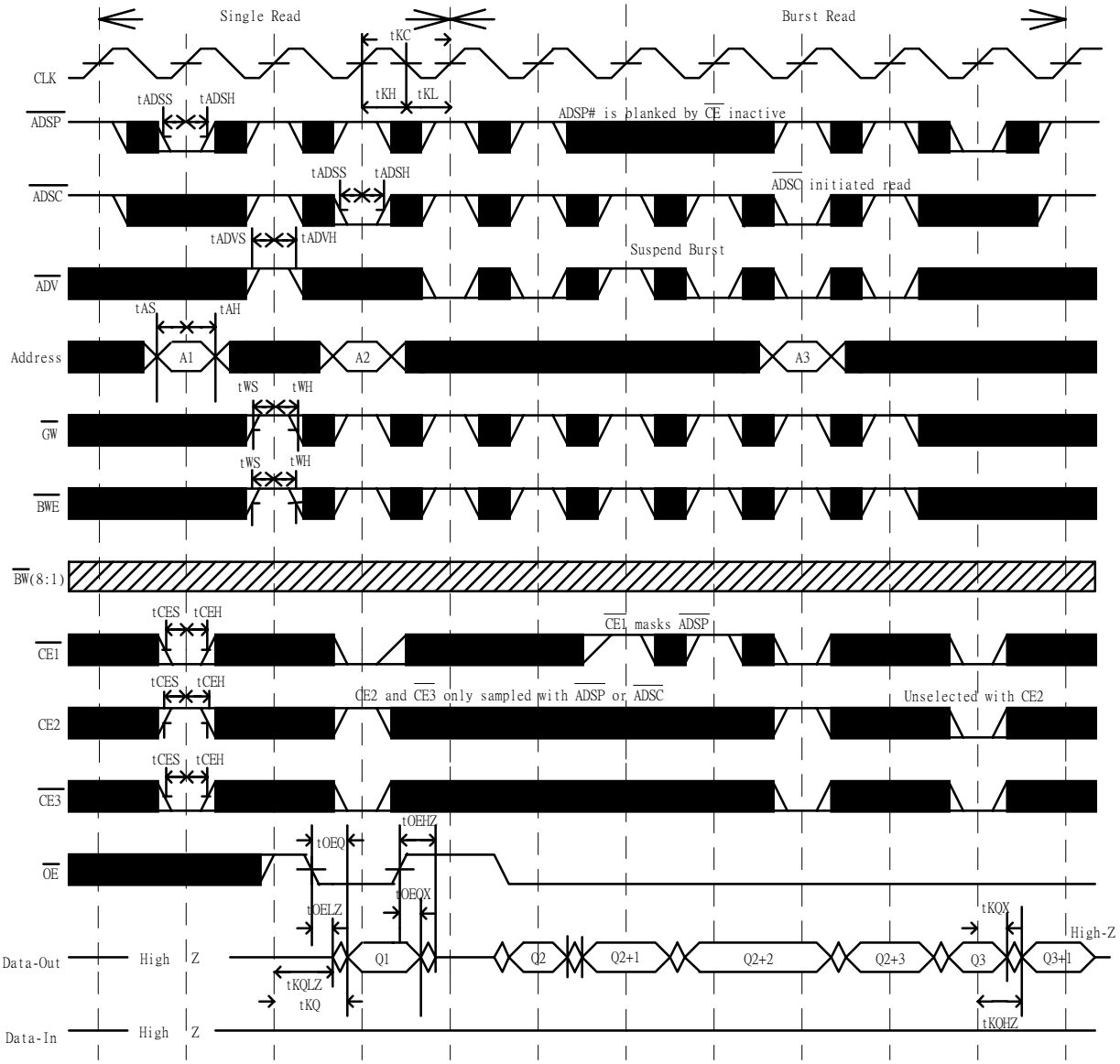

WRITE CYCLE

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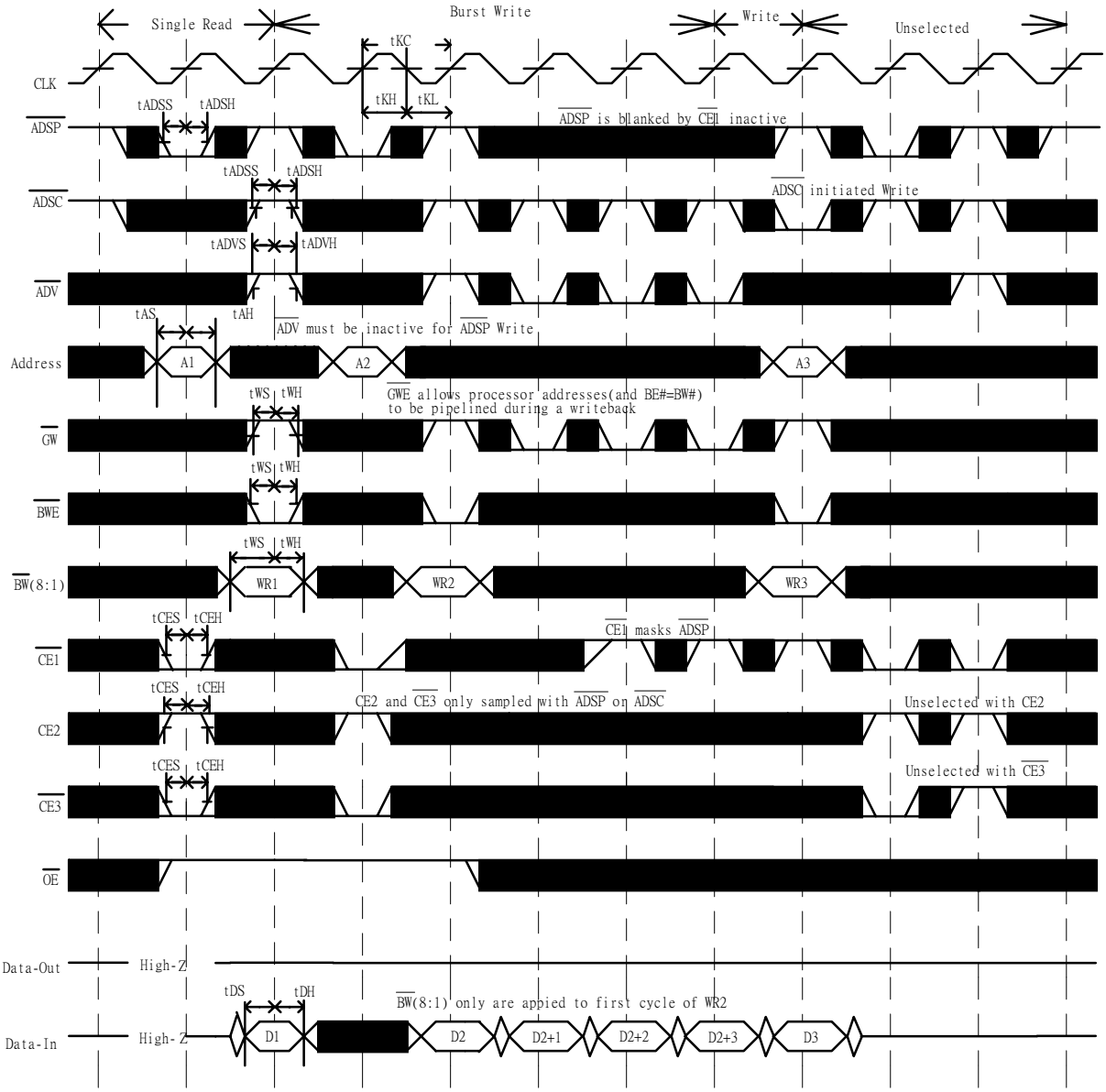
Ultra High-Speed PBSRAM

64K× 64 SYNCHRONOUS PIPELINED-BURST CMOS SRAM

Preliminary



Silicon-Based Technology Corporation

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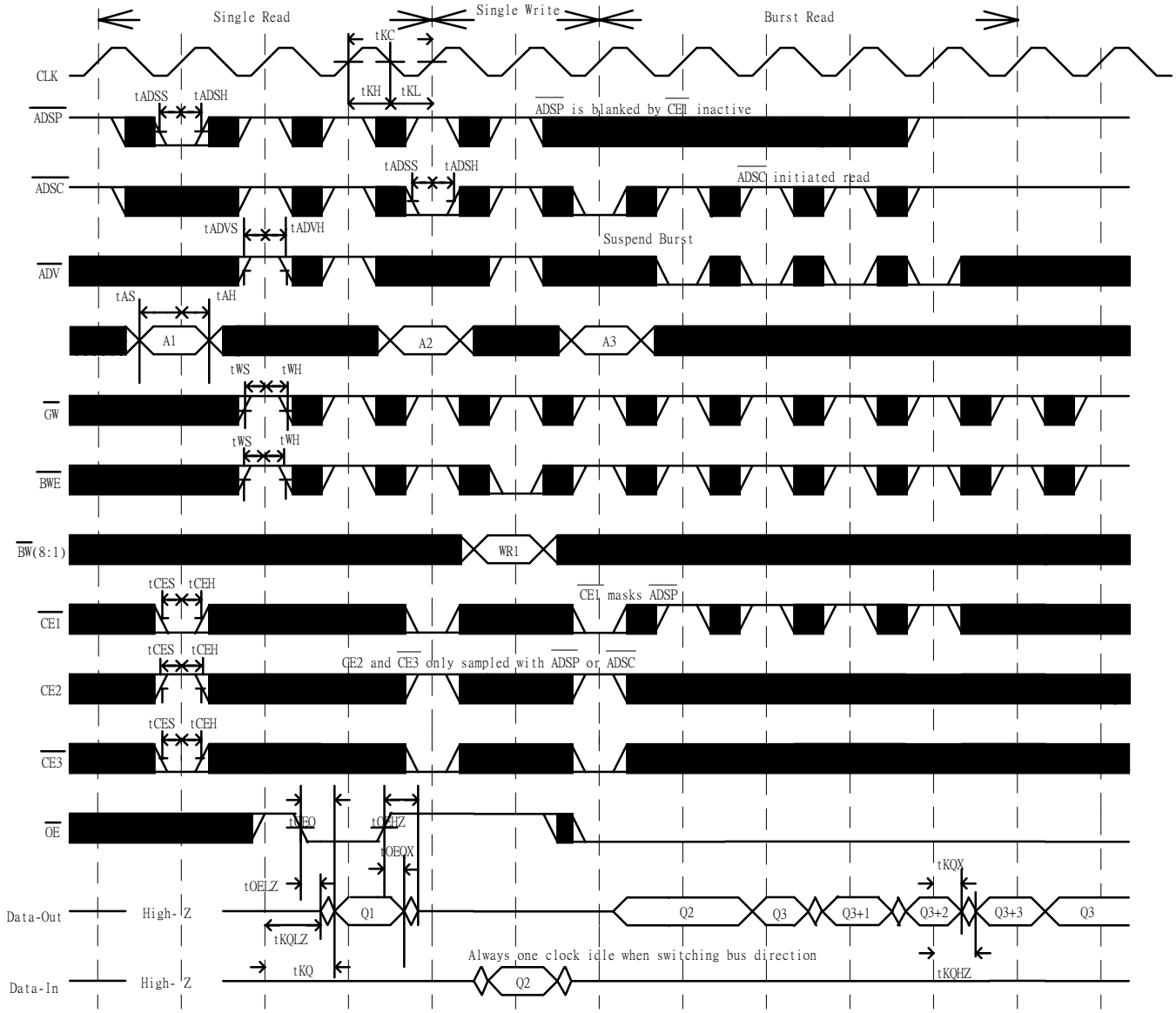
READ/WRITE CYCLE



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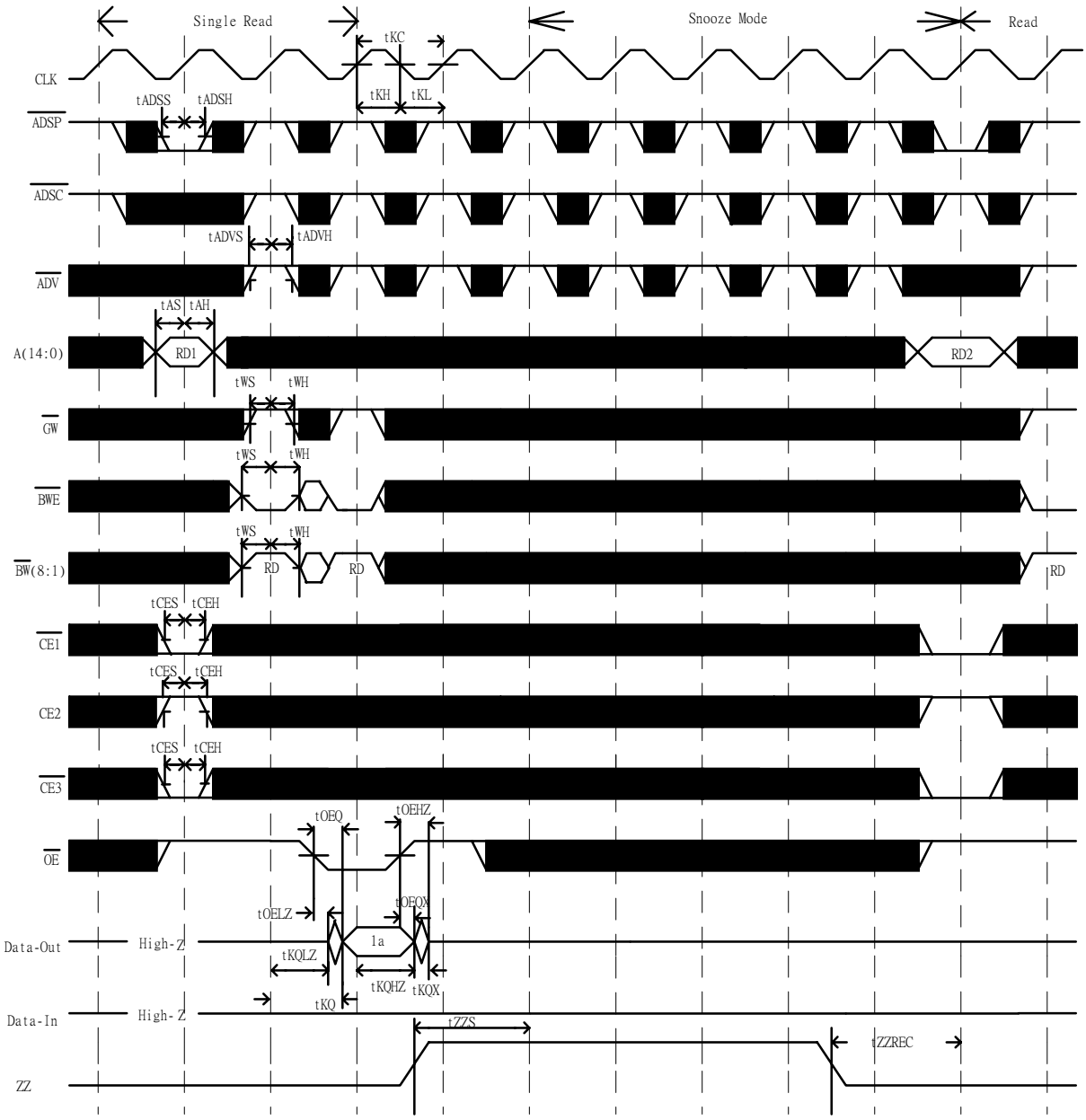
ZZ TIMING



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