Silicon-Based Technology

Very High Speed and Low Power Memory

SB61S1024B

32K× 32 BURST-PIPELINED CMOS SYNCHRONOUS SRAM

PRELIMINARY

Description:

The SB61S1024B series products are 32,768-words by 32-bits burst-pipelined CMOS synchronous SRAMs fabricated with advanced 8" wafer submicron CMOS technology. Using advanced synchronous peripheral circuits and a 2-bit burst counter, the SB61S1024B series products exhibit very high-speed performance with single +3.3-volt power supply. Application areas include data SRAM for both high-performance PCs or workstation, and buffer memory for communication and networking systems. The SB61S1024B is packed in 100-pin QFP/TQFP packages.

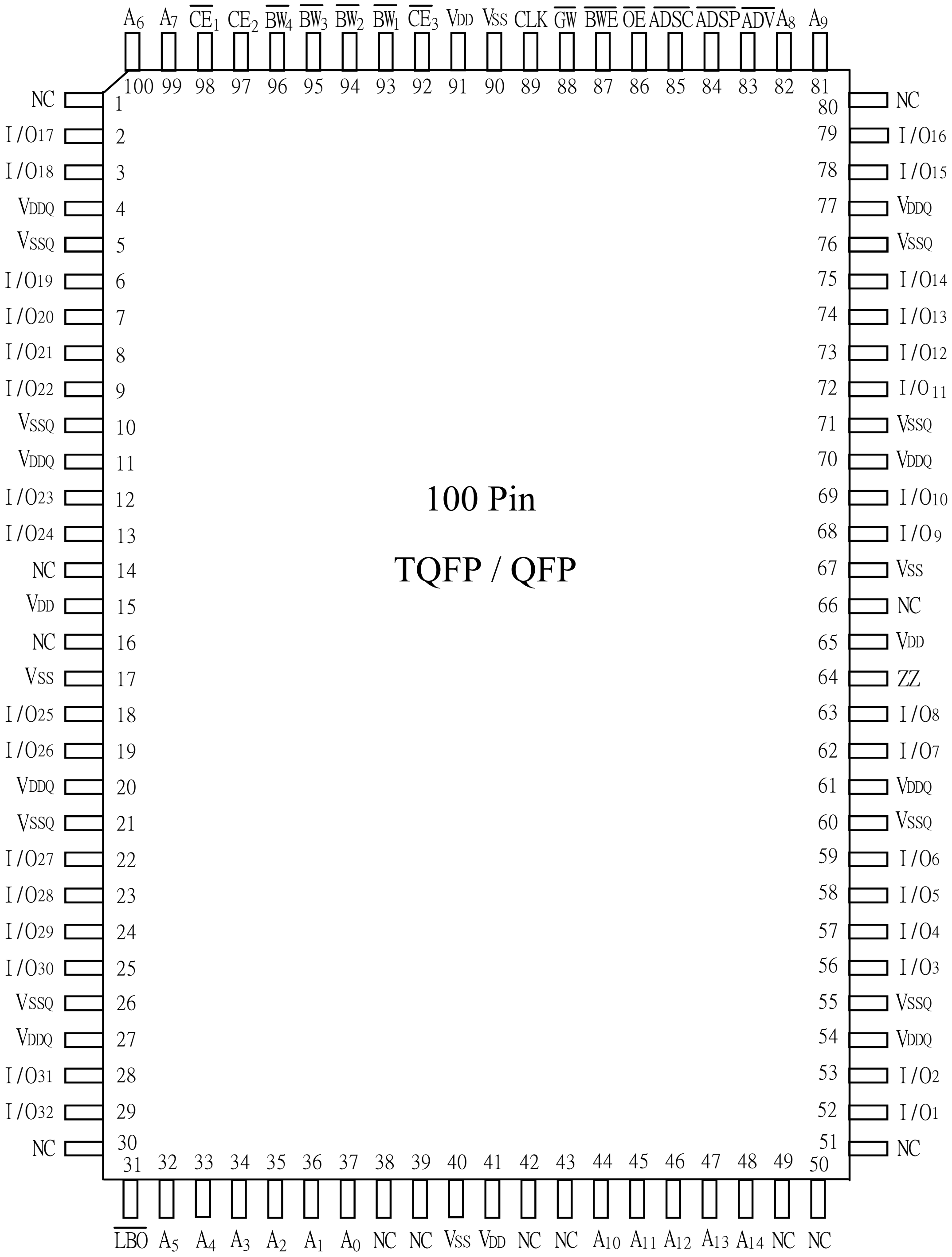
Features:

- Synchronous operation
- Single +3.3-volt power supply
- LVTTL-compatible inputs and outputs
- Very high-speed clock access time: 4/4.5/5 nsec (Max.) for 133M/117M/100MHz clock frequency
- Burst Read/Write for burst and linear burst sequence
- Fully Registered inputs and outputs for pipelined operation
- Asynchronous output enable
- Separate byte write enable and global write enable
- Three chip enables for easy depth expansion
- 2T2T operation feasible for 512K byte and 1M byte data RAM extension
- Power down control provided
- 100-pin QFP/TQFP packages

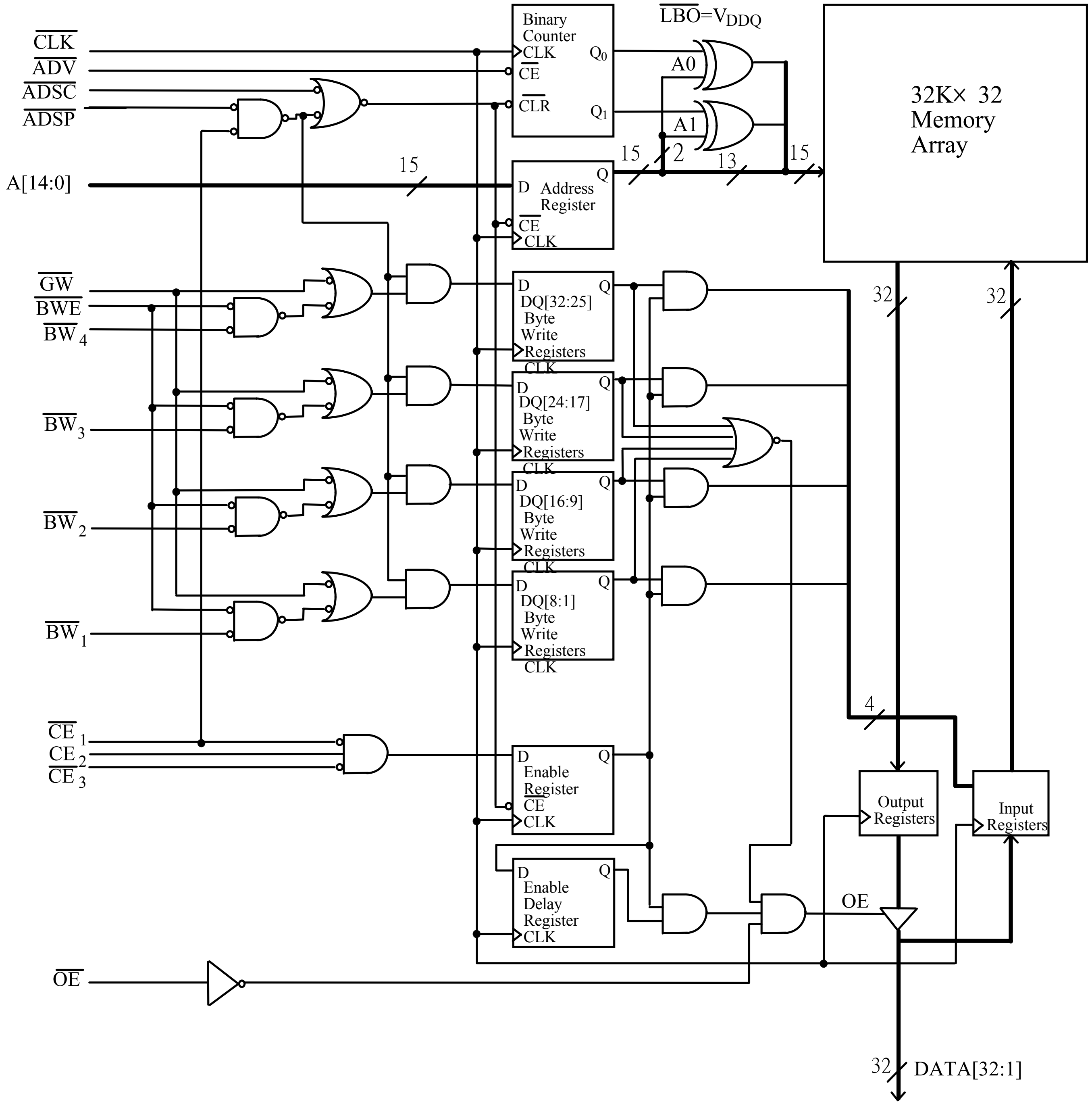
Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	SupplyVoltage (Typ.)
SB61S1024B-4	100-Pin QFP/TQFP	32,768× 32 bits	4 ns/133MHz	3.3± 0.3V
SB61S1024B-4.5			4.5 ns/117MHz	
SB61S1024B-5			5 ns/100MHz	

PIN CONNECTION (Top View) :



Functional Block Diagram :



PIN DESCRIPTION :

SYMBOL	TYPE	DESCRIPTION
A_0-A_{14}	Input, Synchronous	Host Address
I/O_1-I/O_{32}	I/O, Synchronous	Data Inputs / Outputs
CLK	Input, Clock	Processor Host Bus Clock
$\overline{CE_1}$ 、CE_2 、$\overline{CE_3}$	Input, Synchronous	Chip Enables
$\overline{GW}$	Input, Synchronous	Global Write
$\overline{BWE}$	Input, Synchronous	Byte Write Enable from Cache Controller
$\overline{BW_1}$ - $\overline{BW_4}$	Input, Synchronous	Host Bus Byte Enables Used with $\overline{BWE}$
$\overline{OE}$	Input, Asynchronous	Output Enable Input
$\overline{ADV}$	Input, Synchronous	Internal Burst Address Counter Advance
$\overline{ADSC}$	Input, Synchronous	Address Strobe from Chip Set
$\overline{ADSP}$	Input, Synchronous	Address Strobe from CPU
ZZ	Input, Asynchronous	Asynchronous Power Down (Snooze): HIGH (Sleep) LOW or NC (Wake up)
$\overline{LBO}$	Input, Static	Burst Mode: HIGH or NC (Interleaved burst) LOW (Linear burst)
V_{DDQ}		I/O Power Supply
V_{SSQ}		I/O Ground
V_{DD}		Power Supply
V_{SS}		Ground
NC		No Connection

Operating Mode:

(1) Synchronous Input Truth Table

OPERATION	CLK	$\overline{\text{CE1}}$	$\overline{\text{CE3}}$	CE2	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{WRITE}}$ [4]	ZZ [1]	ADDRESS USED	I/O [5]	CURRENT [2]
Begin Burst Read	L→H	L	L	H	L	X	X	X	L	External Address	Dout(n)	IDDO1
	L→H	L	L	H	H	L	X	H	L			
Continue Burst Read	L→H	X	X	X	H	H	L	H	L	Next Burst Address	Dout(n)	IDDO1
	L→H	H	X	X	X	H	L	H	L			
Suspend Burst Read	L→H	X	X	X	H	H	H	H	L	Current Burst Address	Dout(n)	IDDO2
	L→H	H	X	X	X	H	H	H	L			
Begin Burst Write	L→H	L	L	H	H	L	X	L	L	External Address	Din(p)	N/A
	L→H	X	X	X	H	H	H	L	L	Current Burst Address		
	L→H	H	X	X	X	H	H	L	L			
Continue Burst Write	L→H	X	X	X	H	H	L	L	L	Next Burst Address	Din(p)	N/A
	L→H	H	X	X	X	H	L	L	L			
Suspend Burst Write	L→H	X	X	X	H	H	H	L	L	Current Burst Address	Din(p)	N/A
	L→H	H	X	X	X	H	H	L	L			
Deselected	L→H	H	X	X	X	L	X	X	L	None	Hi-Z(p)	IDDS2
	L→H	L	H	X	L	X	X	X	L			
	L→H	L	X	L	L	X	X	X	L			
	L→H	L	H	X	H	L	X	X	L			
	L→H	L	X	L	H	L	X	X	L			
Snooze	L→H	X	X	X	X	X	X	X	H	None	Hi-Z(p)	IDDS3

Note: 1. ZZ input is asynchronous, but is included in this table.
2. Consumption current does not include output buffer current.
3. H is logical High and L is logical Low. X is High or Low .
4. $\overline{\text{WRITE}}$ = L means any one or more byte write enable inputs($\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$, $\overline{\text{BW4}}$) and $\overline{\text{BWE}}$ are Low or $\overline{\text{GW}}$ is Low. $\overline{\text{WRITE}}$ = H means $\overline{\text{GW}}$ and $\overline{\text{BWE}}$ are High, or $\overline{\text{GW}}$ is High and $\overline{\text{BWE}}$ is Low and all byte write enable inputs are High.
5. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.

(2) Partial Truth Table for Write Enables (Synchronous Input)

OPERATION	CLK	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	I/O1-I/O8	I/O9-I/O16	I/O17-I/O24	I/O25-I/O32
Read	L→H	H	H	X	X	X	X	DOUT(n)	DOUT(n)	DOUT(n)	DOUT(n)
	L→H	H	L	H	H	H	H	DOUT(n)	DOUT(n)	DOUT(n)	DOUT(n)
Write	L→H	L	X	X	X	X	X	Din(p)	Din(p)	Din(p)	Din(p)
		H	L	L	L	L	L	Din(p)	Din(p)	Din(p)	Din(p)
		H	L	L	H	H	H	Din(p)	Hi-Z(p)	Hi-Z(p)	Hi-Z(p)
				H	L	H	H	Hi-Z(p)	Din(p)	Hi-Z(p)	Hi-Z(p)
				H	H	L	H	Hi-Z(p)	Hi-Z(p)	Din(p)	Hi-Z(p)
				H	H	H	L	Hi-Z(p)	Hi-Z(p)	Hi-Z(p)	Din(p)
				The other 12 combinations of $\overline{BW1}$ to $\overline{BW4}$ are also effective. $\overline{BW1}$ controls I/O1-I/O8. $\overline{BW2}$ controls I/O9-I/O16. $\overline{BW3}$ controls I/O17-I/O24. $\overline{BW4}$ controls I/O25-I/O32.							

NOTE: 1. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.

(3) Asynchronous Truth Table

OPERATION	$\overline{OE}$	I/O1-I/O32
Read	L	DOUT
	H	Hi-Z
Write	X	Din, Hi-Z
Deselected	X	Hi-Z
Snooze	X	Hi-Z

(4) Write Pass-through Truth Table

Previous Cycle				Present Cycle											Next Cycle
Operation	Addr.	$\overline{\text{WRITE}}$	I/O	Operation	Addr.	$\overline{\text{WRITE}}$	$\overline{\text{CE1}}$	$\overline{\text{CE3}}$	CE2	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{\text{OE}}$	I/O	I/O
Write Cycle	Ak	L	Dn(Ak)	$\overline{\text{ADSP}}$ Initiated Read Cycle	Am	X	L	L	H	L	X	X	L	Qn(AK)	Q1(Am)
				$\overline{\text{ADSC}}$ Initiated Read Cycle	Am	H	L	L	H	H	L	X	L		
				Continue Read Cycle	X	H	X	X	X	H	H	L	L		Qn+1(Ak)
					X	H	H	X	X	X	H	L	L		

NOTE: 1. Dn(Ak) represents input data for the n-th burst address starting from address Ak.
2. Qn(Ak) represents output data from the n-th burst address starting from address Ak.
3. n=1, 2, 3, or 4
4. $\overline{\text{WRITE}}$ = L means any one or more byte write enable inputs ($\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$, $\overline{\text{BW4}}$) and $\overline{\text{BWE}}$ are Low or $\overline{\text{GW}}$ is Low. $\overline{\text{WRITE}}$ = H means $\overline{\text{GW}}$ and $\overline{\text{BWE}}$ are High, or $\overline{\text{GW}}$ is High and $\overline{\text{BWE}}$ is Low and all byte write enable inputs are High.

(5) Interleaved Burst Sequence ($\overline{\text{LBO}}$ input = NC or V_{DD})

Bit Order : A_{14} A_{13}...................... A_3 A_2 A_1 A_0

Lower 2 bits are internally generated from the external addresses , A_1 and A_0.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX.........XX00	XX.........XX01	XX.........XX10	XX.........XX11
XX.........XX01	XX.........XX00	XX.........XX11	XX.........XX10
XX.........XX10	XX.........XX11	XX.........XX00	XX.........XX01
XX.........XX11	XX.........XX10	XX.........XX01	XX.........XX00

The burst address wraps around to its initial state.

(6) Linear Burst Sequence ($\overline{\text{LBO}}$ input = V_{SS})

Bit Order : A_{14} A_{13}...................... A_3 A_2 A_1 A_0

Lower 2 bits are internally generated from the external addresses , A_1 and A_0.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX.........XX00	XX.........XX01	XX.........XX10	XX.........XX11
XX.........XX01	XX.........XX10	XX.........XX11	XX.........XX00
XX.........XX10	XX.........XX11	XX.........XX00	XX.........XX01
XX.........XX11	XX.........XX00	XX.........XX01	XX.........XX10

The burst address wraps around to its initial state.

DC Characteristics:

Absolute Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5～+4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	-0.5～V_{DD}	V
V_{IN}	Input Terminal Voltage	-0.5*～+4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	-0.5*～V_{DDQ}+0.5**	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10s)	260	℃
T_{strg}	Storage Temperature	-65～150	℃
T_{opr}	Operating Temperature	-10～85	℃

*：-1.5V with a pulse width of 0.2 t_{KC} min

**：V_{DD}+1.5V with a pulse width of 0.2 t_{KC} min

Recommended DC Operating Conditions (Ta = 0～80℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{DD}+0.3**	V
V_{IH1}	Input High Voltage for $\overline{LBO}$ pin	V_{DD} — 0.3	V_{DD}	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.8	V
V_{IL1}	Input Low Voltage for $\overline{LBO}$ pin	-0.3	0.0	0.3	V

*：-1.0V with a pulse width of 0.2 t_{KC} min

**：V_{DD}+1.0V with a pulse width of 0.2 t_{KC} min

Operating Characteristics (Ta=0～80℃, V_{DD}=3.3V± 0.3V, V_{DDQ}=3.3V± 0.3V)

SYMBOL	PARAMETERS		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current (Except $\overline{\text{LBO}}$,ZZ, pins)		V_{IN}=0～V_{DD}		-1	-	+1	μA
I_{LO}	Output Leakage Current		Device Deselected or Output Deselected, V_{OUT}=0～V_{DD}		-1	-	+1	μA
I_I	Input Current	$\overline{\text{LBO}}$ pin	V_{IN}=V_{DD}～V_{DD}-0.3V		-1	-	1	μA
			V_{IN}=0～0.3V		-100	-	1	
		ZZ pin	V_{IN}=V_{DD}～2.0V		-1	-	100	
			V_{IN}=0～0.8V		-1	-	20	
			V_{IN}=～0.3V		-1	-	1	
V_{OH}	Output High Voltage		I_{OH}= -8mA		2.4	-	-	V
			I_{OH}= -100μA		V_{DD}-0.2	-	-	
V_{OL}	Output Low Voltage		I_{OL}= 8mA		-	-	0.4	
			I_{OL}= 100μA		-	-	0.2	
I_{DDQ1}	Operating Current		Device Selected, I_{OUT}=0mA All inputs=V_{IH}/V_{IL}, CLK≧t_{kC} min .	-5	-	-	280	mA
				-4.5	-	-	300	
				-4	-	-	350	
I_{DDQ2}	Operating Current (Idle)		Device Selected, I_{OUT} = 0mA $\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$, $\overline{\text{ADV}}$ ≧ V_{IH} All inputs = V_{IH}/V_{IL}, CLK≧t_{kC} min.		-	-	60	mA
I_{DDS1}	Standby Current (CLK running)		Device Deselected, All inputs = V_{IH}/V_{IL} CLK≧t_{kC} min.		-	-	50	mA
I_{DDS2}	Standby Current		Device Deselected, All inputs = V_{DD}-0.2V or 0.2V, CLK frequency = 0 Hz		-	-	5	mA
I_{DDS3}	Standby Current		ZZ = V_{DD}-0.2V, All inputs = V_{IH}/V_{IL} CLK≧t_{kC} min.		-	-	5	mA

Capacitance (Ta = 25℃, f = 1.0MHz)

SYMBOL	PARAMETERS	TEST CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF
C_{CLK}	Clock Input Capacitance	V_{CLK} = GND	8	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

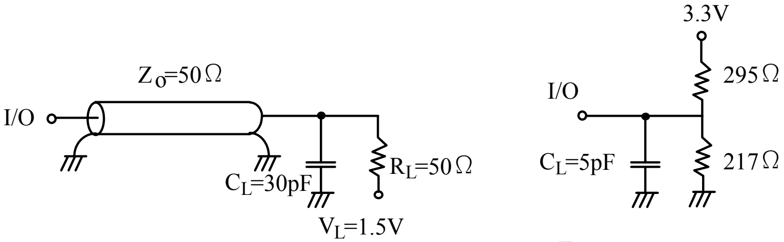
AC Timing Characteristics:

(Ta = 0～80℃, V_{DD}=3.3V± 0.3V, V_{DDQ}=3.3V± 0.3V)

SYMBOL	PARAMETERS	SB61S1024B-4 133MHz		SB61S1024B-4.5 117MHz		SB61S1024B-5 100MHz		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{KC}	CLK Cycle Time	7.5	-	8	-	10	-	ns
t_{KH}	CLK High Pulse Width	3	-	4	-	4	-	
t_{KL}	CLK Low Pulse Width	3	-	4	-	4	-	
t_{KQ}	Access Time from CLK	-	4	-	4.5	-	5	
t_{KQX}	Output Hold Time from CLK	2	-	2	-	2	-	
t_{KQLZ}	Output Enable Time from CLK	0	-	0	-	0	-	
t_{KQHZ}	Output Disable Time from CLK	2	4	2	4.5	2	5	
t_{OEQ}	Access Time from $\overline{OE}$	-	4	-	4.5	-	5	
t_{OELZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OEHZ}	Output Disable Time from $\overline{OE}$	2	4	2	4.5	2	5	
t_{AS}	Address Input Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{AH}	Address Input Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{ADSS}	$\overline{ADSP}$, $\overline{ADSC}$ Input Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Input Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{AAH}	$\overline{ADV}$ Input Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{AAS}	$\overline{ADV}$ Input Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{WS}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{WH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ Input Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{CES}	$\overline{CE1}$, CE2, $\overline{CE3}$ Input Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{CEH}	$\overline{CE1}$, CE2, $\overline{CE3}$ Input Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{DS}	Write Data Setup Time from CLK	2.5	-	2.5	-	2.5	-	
t_{DH}	Write Data Hold Time from CLK	0.5	-	0.5	-	0.5	-	
t_{ZS}	ZZ Setup Time from CLK	4	-	4	-	4	-	
t_{ZH}	ZZ Hold Time from CLK	1	-	1	-	1	-	
t_{ZR}	ZZ Recovery Time	40	-	40	-	40	-	

AC Test Conditions

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig.1

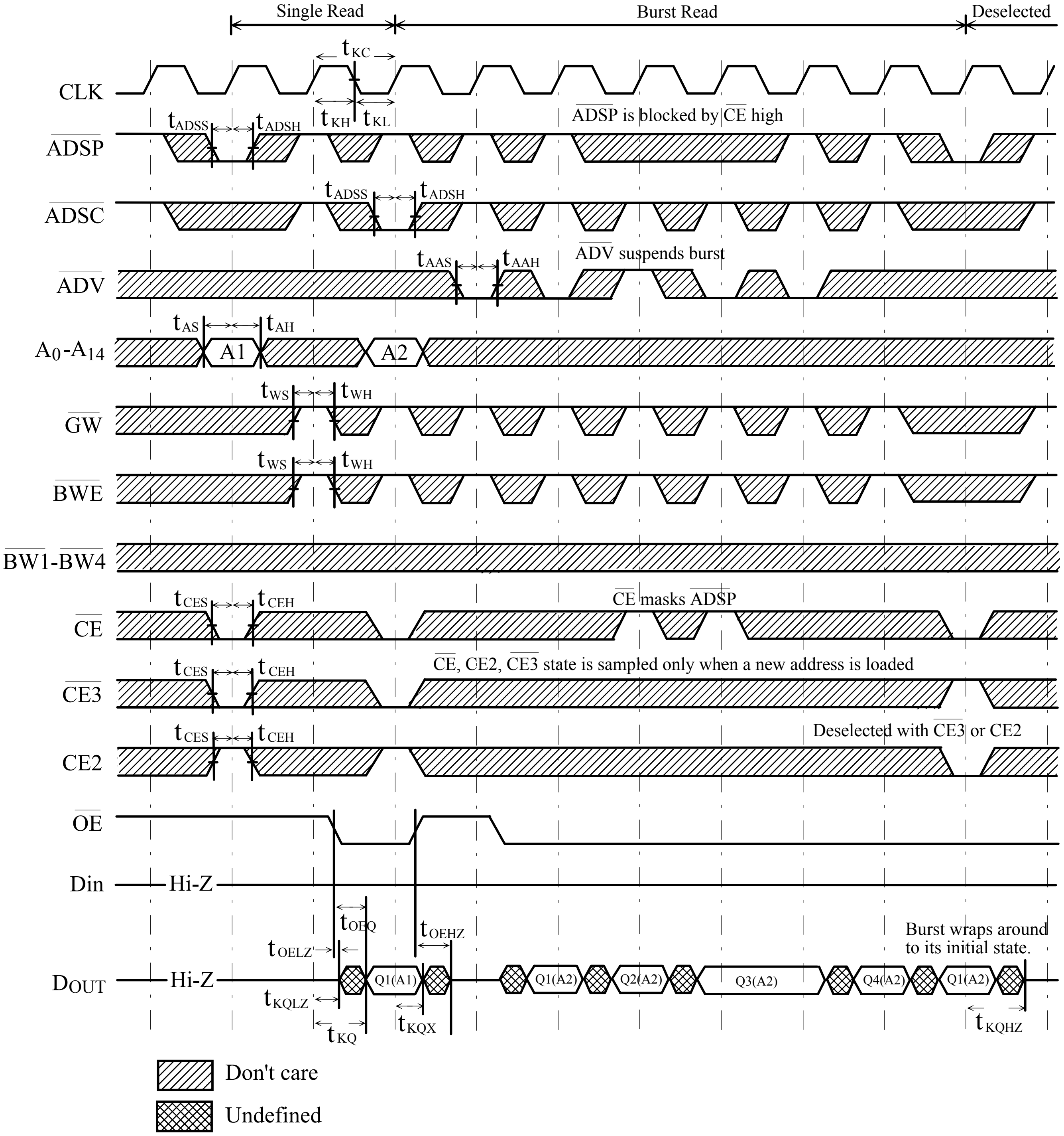


For t_{KQLZ}, t_{KQHZ}, t_{GQLZ} and t_{GQHZ}

Fig. 1

TIMING WAVEFORMS

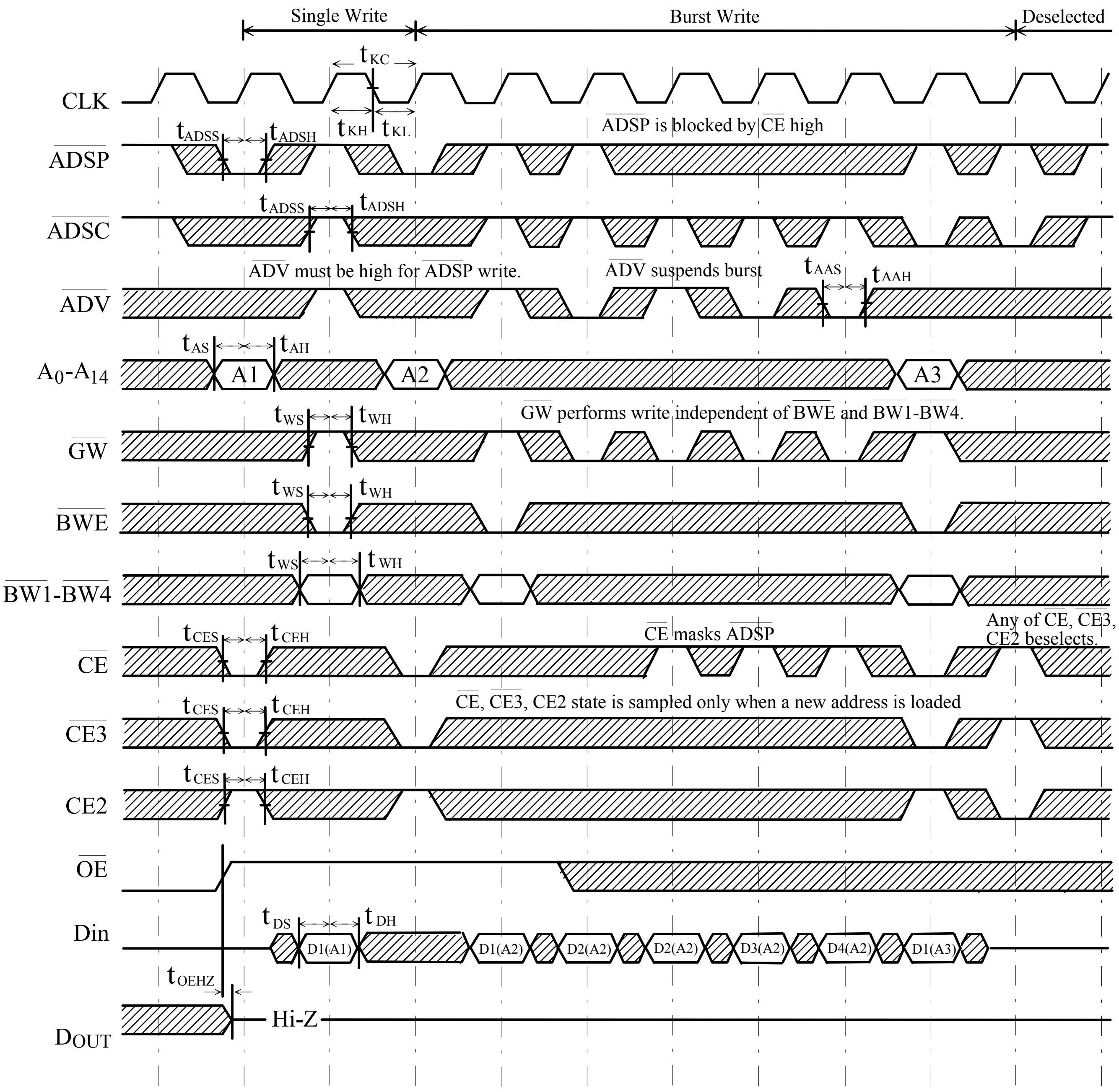
READ CYCLE



Note

1. Q1(A2) represents output data from lst burst address starting from address As. Q2(A2) represents output data from 2nd burst address starting from address A2.

WRITE CYCLE



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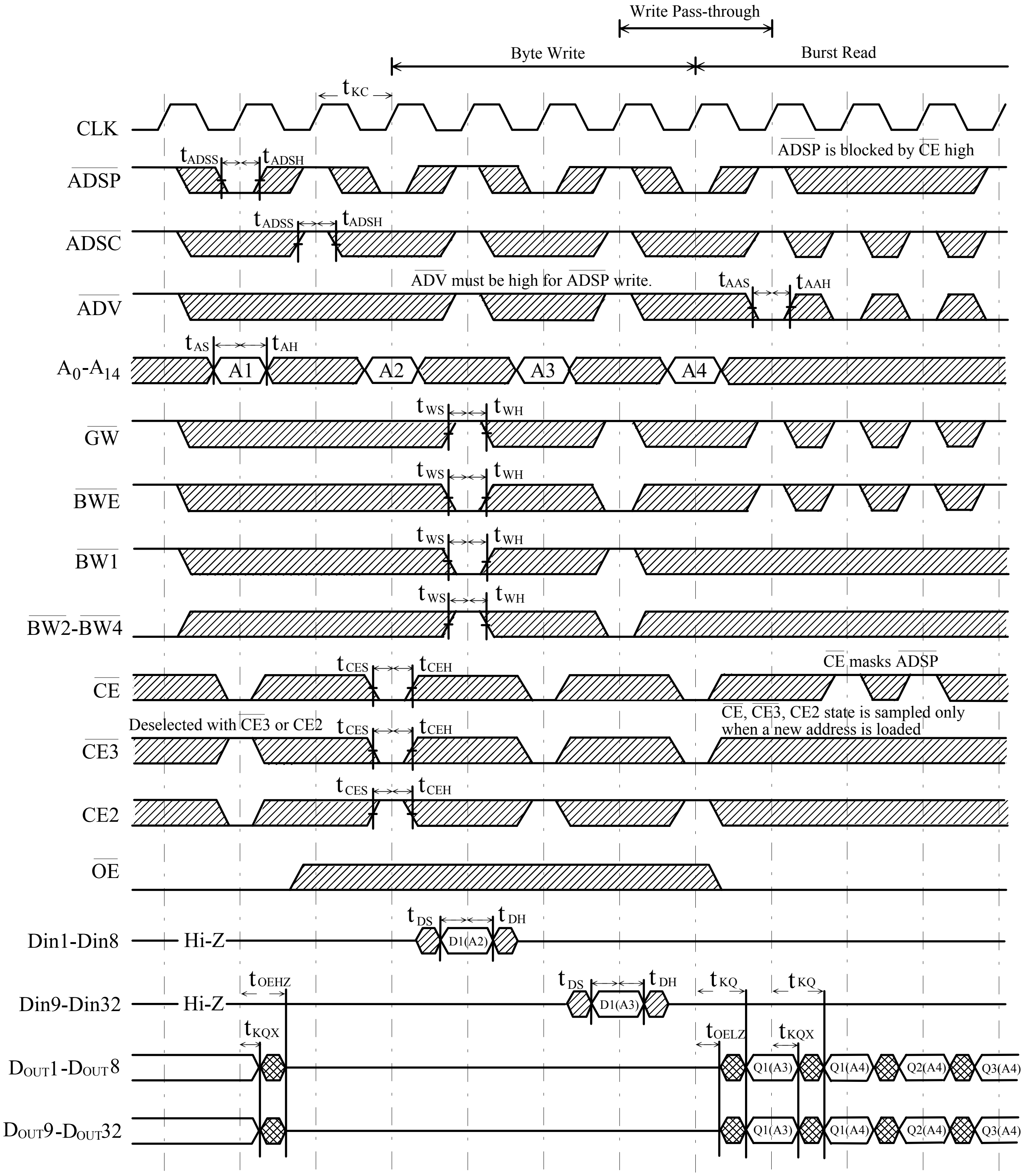
Note

1. D1(A2) represents input data for 1st burst address starting from address A2.. D2(A2) represents input data form 2nd burst address starting from address A2.

WRITE CYCLE (Byte Write Timing)



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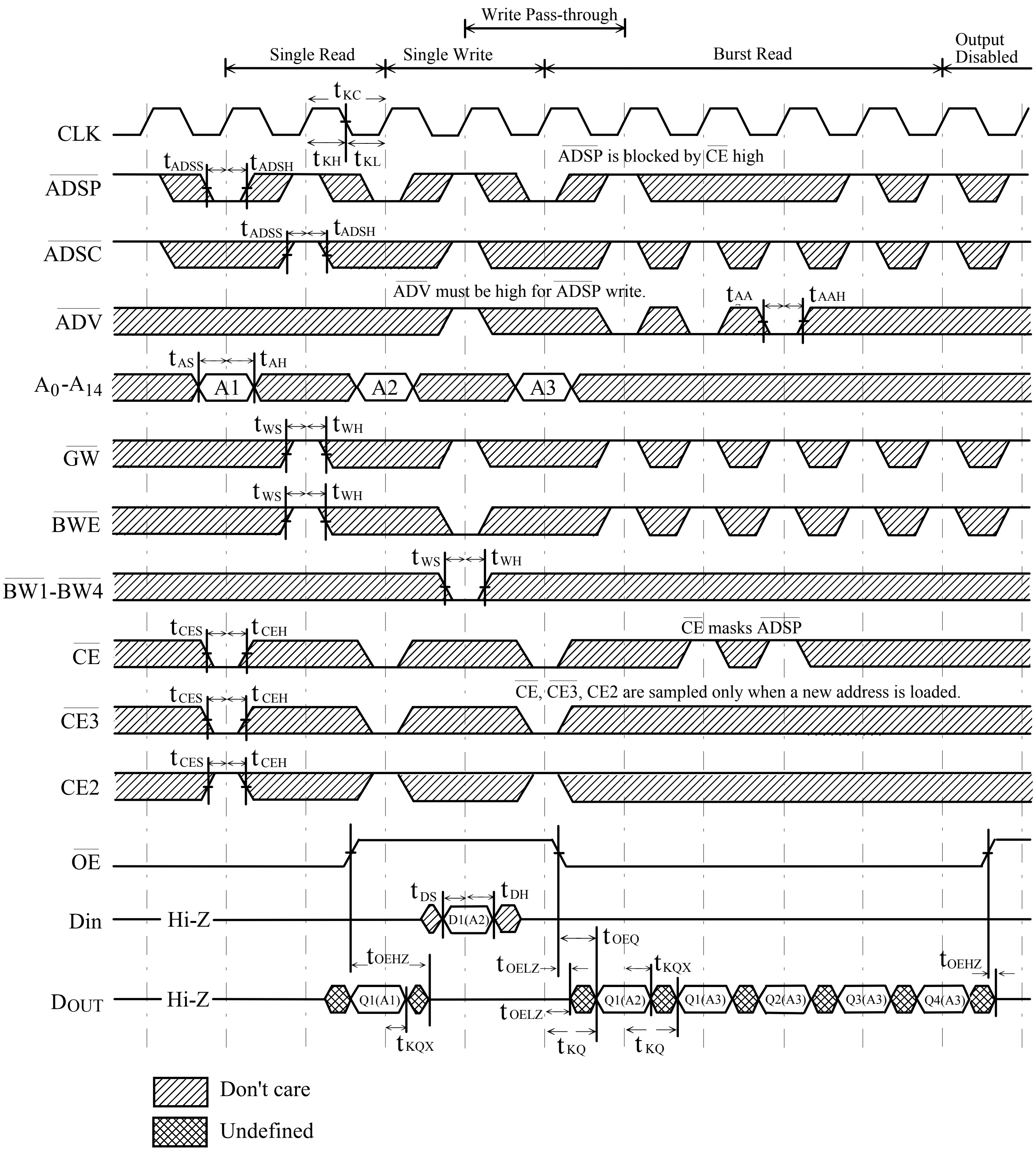
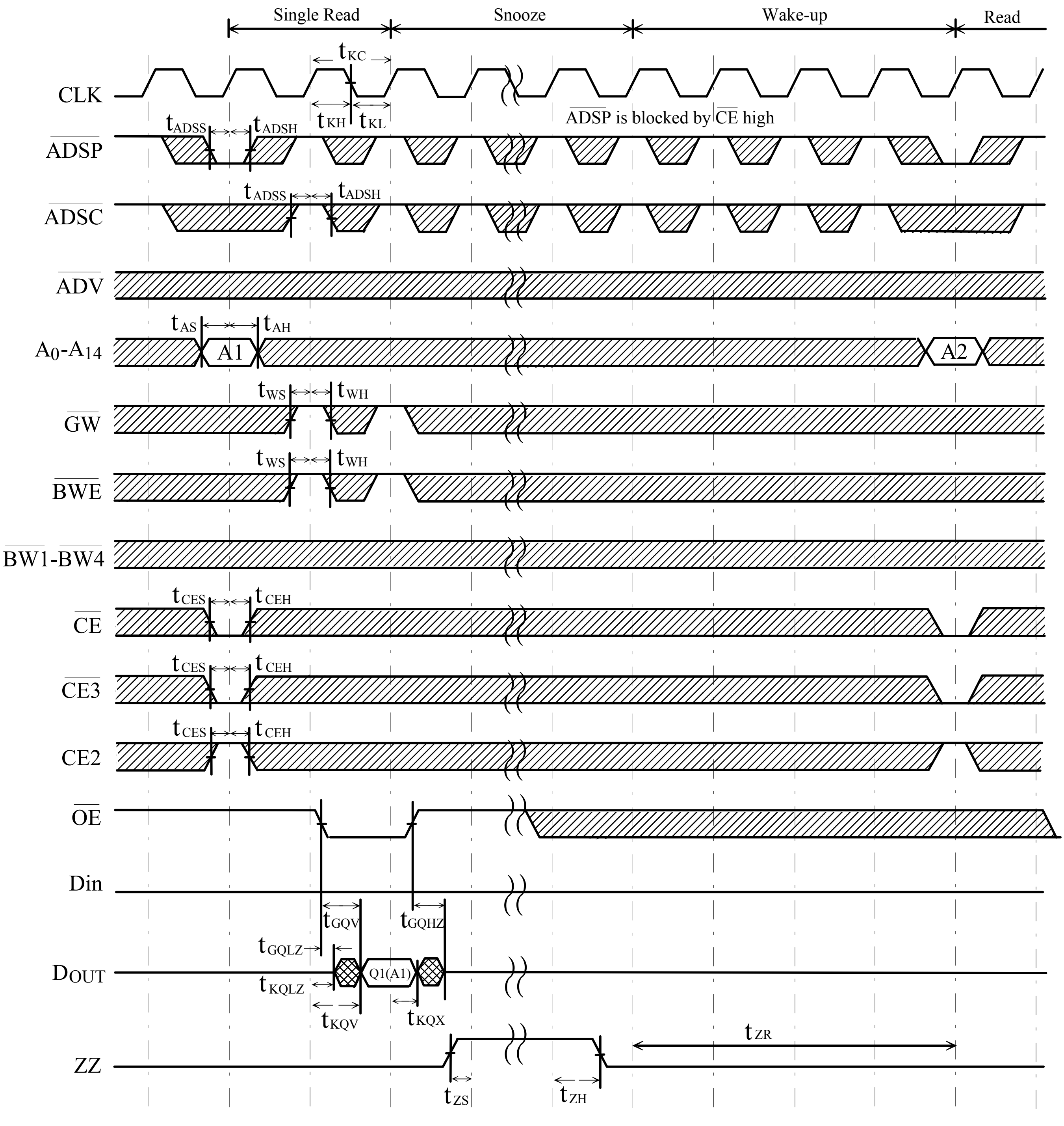
READ/WRITE CYCLE



Note

1. When a write operation follows a read operation, $\overline{OE}$ must be driven high prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$) and before input data is applied to avoid data bus contention.

SNOOZE CYCLE



▨ Don't care

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