

Silicon-Based Technology

Very High Speed and Low Power Memory

PRELIMINARY

Description:

The SB61H1024AT-XG series products are 131,072-words by 8-bits static RAM fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61H1024AT-XG series products exhibit very high-speed performance with single +5-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61H1024AT-XG is packed in a standard 32-pin 8mil*20mil TSOP-1 and other packages are available upon preorder.

Features:

- 131,072-word x 8-bit organization
- Single +5-volt power supply
- Fully static operation **■** no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
 - Active: 180/160/140 mA (Max.)
 - Standby: 5 mA
- Very high speed access: 10/12/15 ns (Max.)
- 32-pin plastic 8mil*20mil TSOP-1 green package
- Output Enable (**OE**) available for very fast access

Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61H1024AT-10G	32-Pin Plastic TSOP-1 8mil*20mil	128Kx8 bits	10	5V±10%	180	5
SB61H1024AT-12G			12		160	
SB61H1024AT-15G			15		140	

The information in this document is subject to change without notice



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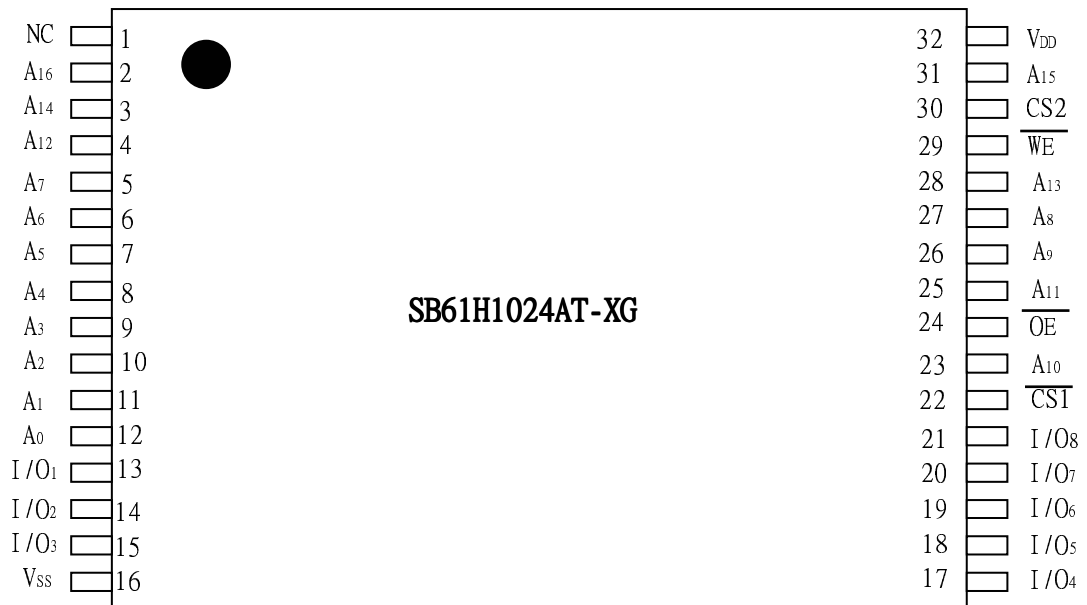
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Preliminary

Pin Configuration: 32-Pin 8mil*20mil TSOP-1

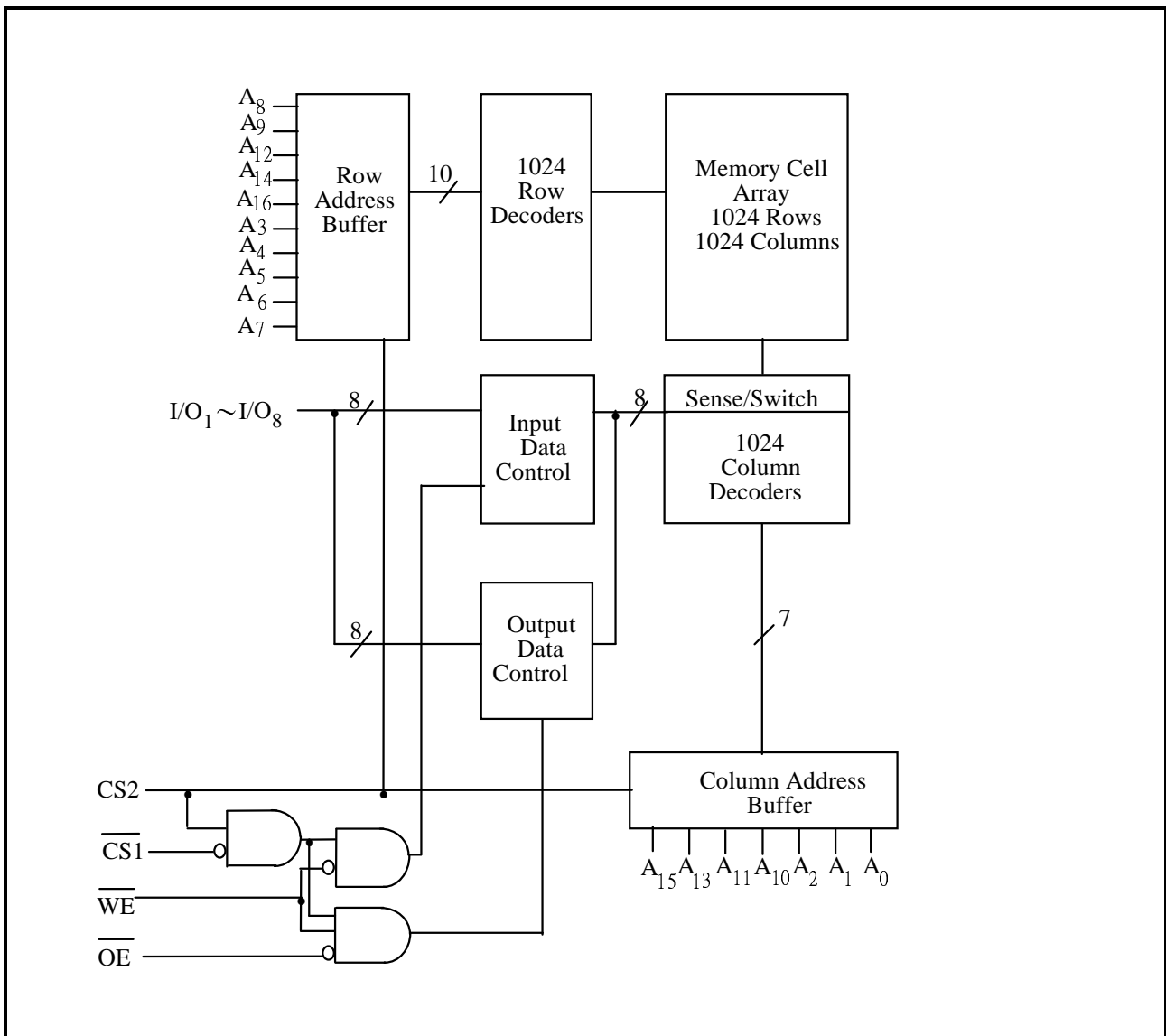


Symbols	Functions
A ₀ ~A ₁₆	Address Inputs
I/O ₁ ~I/O ₈	Data Inputs/Outputs
$\overline{CS1}$,CS2	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground



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Block Diagram:



Truth Table:

$\overline{CS1}$	$\overline{CS2}$	\overline{OE}	\overline{WE}	Mode	$I/O_1 \sim I/O_8$	V_{DD} Current
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}



Preliminary

DC Characteristics:

Absolute Maximum Ratings

Parameters	Rating	Unit
Supply Voltage to V _{SS}	-0.5 to +7.0	V
Input/Output to V _{SS}	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Operating Characteristics:

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max.	Unit	
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.7	-	V _{DD} +0.5	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-10	-	+10	μA	
Output Low Voltage	V _{OL}	I _{OL} = +8.0mA	-	-	+0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	+2.4	-	-	V	
Operating Power	I _{DD}	$\overline{CS} = V_{IL}$, I/O = 0 mA Cycle = MIN, Duty = 100%	10	-	-	180	mA
Supply Current			12	-	-	160	mA
			15	-	-	140	mA
Standby Power	I _{SB}	$\overline{CS} = V_{IH}$, Cycle = MIN Duty = 100%	-	-	10	mA	
Supply Current	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	5	mA	

Note: Typical characteristics are measured at V_{DD} = 5V, T_a = 25°C



AC Characteristics:

Capacitances

($V_{DD} = 5V$, $T_a = 25^\circ C$, $f = 1\text{ MHz}$)

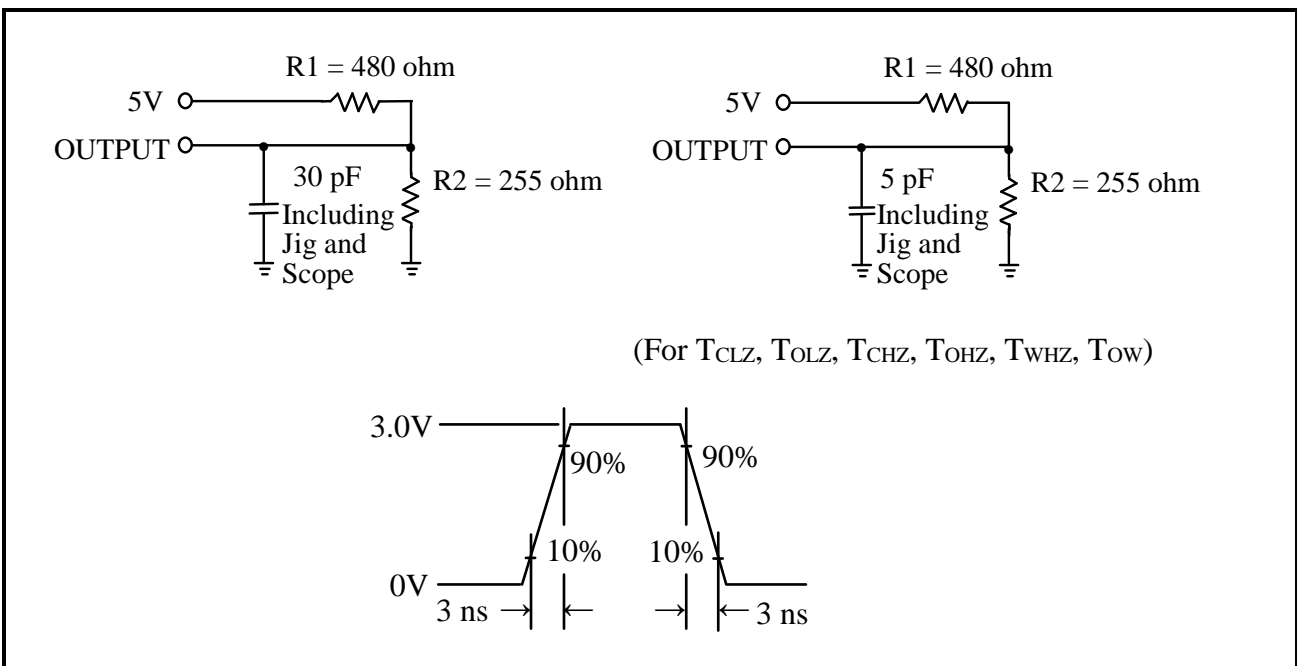
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	8	pF

Note: These parameters are sampled but not 100% tested.

AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -4\text{ mA}/8\text{ mA}$

AC Test Loads and Waveforms





AC Performances:

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C)

(1) Read Cycle

Parameters	Symbols	SB61H1024AT-10G		SB61H1024AT-12G		SB61H1024AT-15G		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T _{RC}	10	-	12	-	15	-	ns
Address Access Time	T _A A	-	10	-	12	-	15	ns
Chip Select Access Time	T _A C _S	-	10	-	12	-	15	ns
Output Enable to Output Valid	T _A O _E	-	6	-	7	-	8	ns
Chip Selection to Output in Low Z	T _C L _Z *	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T _O L _Z *	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T _C H _Z *	-	5	-	6	-	7	ns
Output Disable to Output in High Z	T _O H _Z *	-	5	-	6	-	7	ns
Output Hold from Address Change	T _O H	3	-	3	-	3	-	ns

*These parameters are sampled but not 100% tested

(2) Write Cycle

Parameters	Symbols	SB61H1024AT-10G		SB61H1024AT-12G		SB61H1024AT-15G		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T _W C	10	-	12	-	15	-	ns
Chip Selection to End of Write	T _C W	8	-	10	-	12	-	ns
Address Valid to End of Write	T _A W	8	-	10	-	12	-	ns
Address Setup Time	T _A S	0	-	0	-	0	-	ns
Write Pulse Width	T _W P	8	-	10	-	12	-	ns
Write Recovery Time	T _W R	0	-	0	-	0	-	ns
Data Valid to End of Write	T _D W	6	-	8	-	10	-	ns
Data Hold from End of Write	T _D H	0	-	0	-	0	-	ns
Write to Output in High Z	T _W H _Z *	-	5	-	6	-	7	ns
Output Disable to Output in High Z	T _O H _Z *	-	5	-	6	-	7	ns
Output Active from End of Write	T _O W	0	-	0	-	0	-	ns

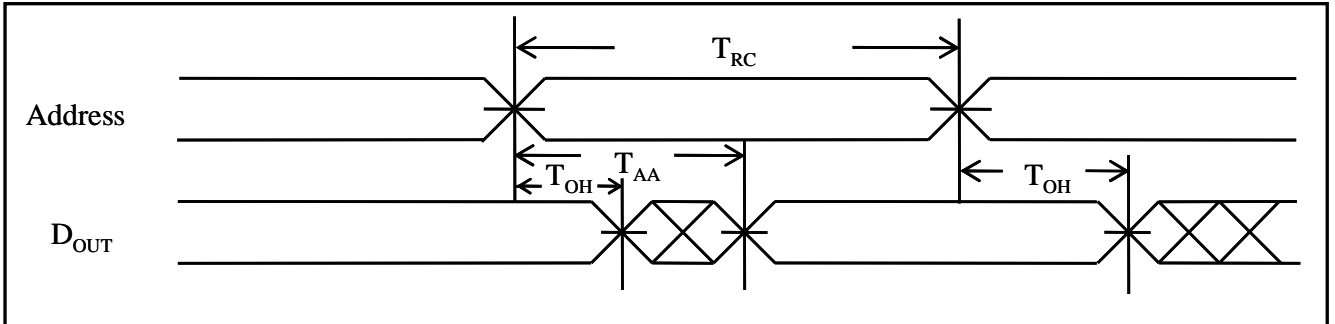
* These parameters are sampled but not 100% tested



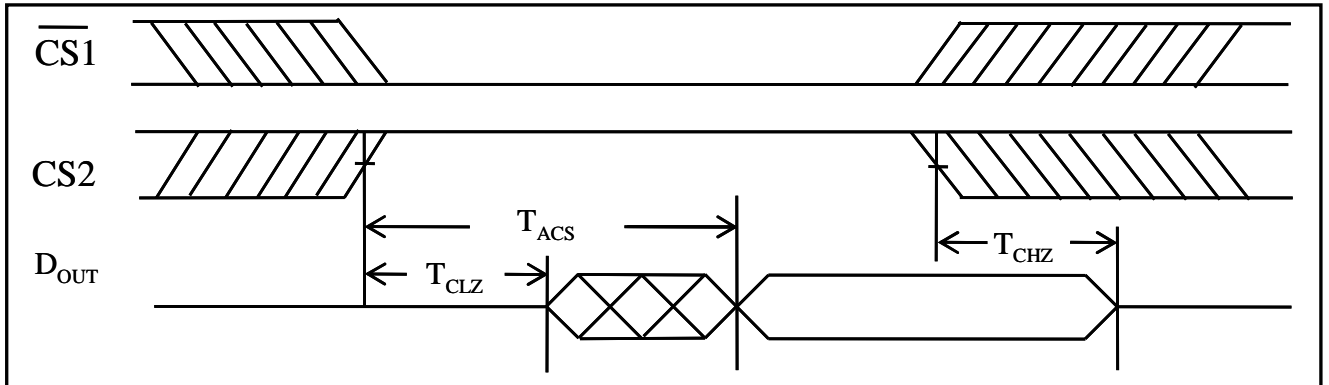
Preliminary

Timing Waveforms

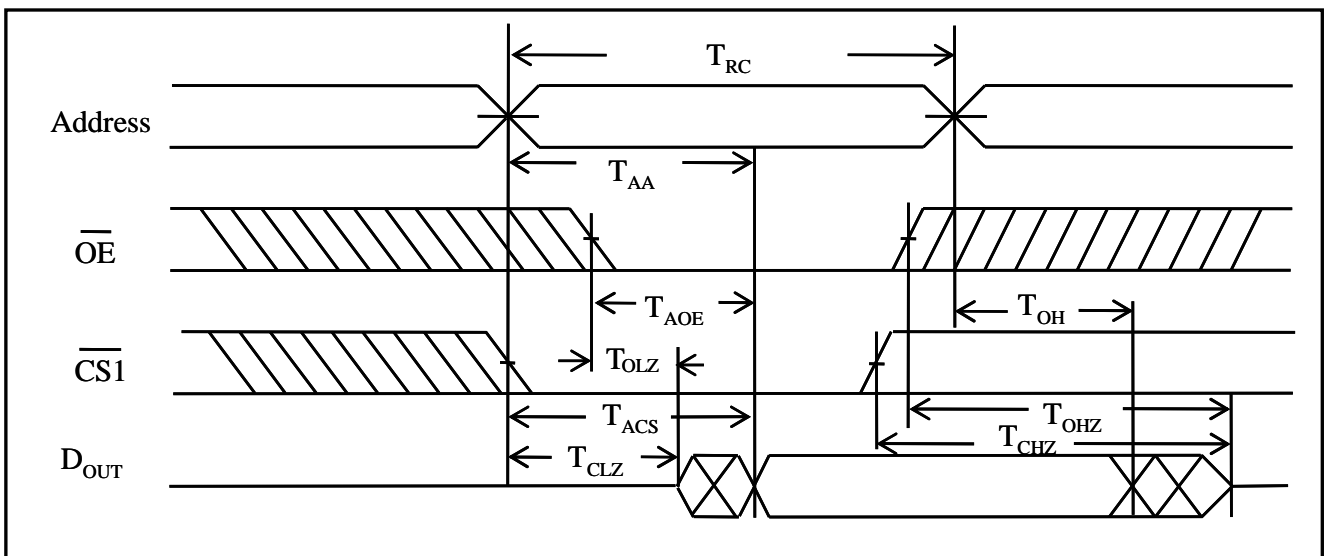
Read Cycle 1
(Address Controlled)

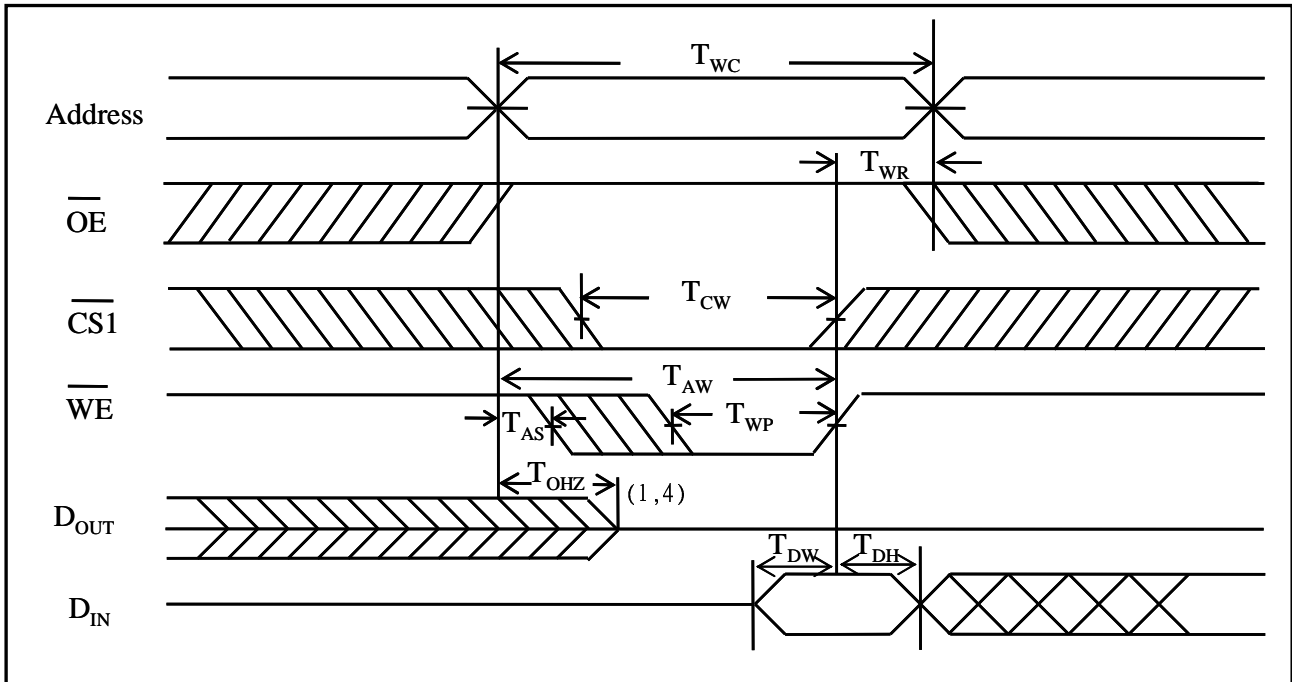
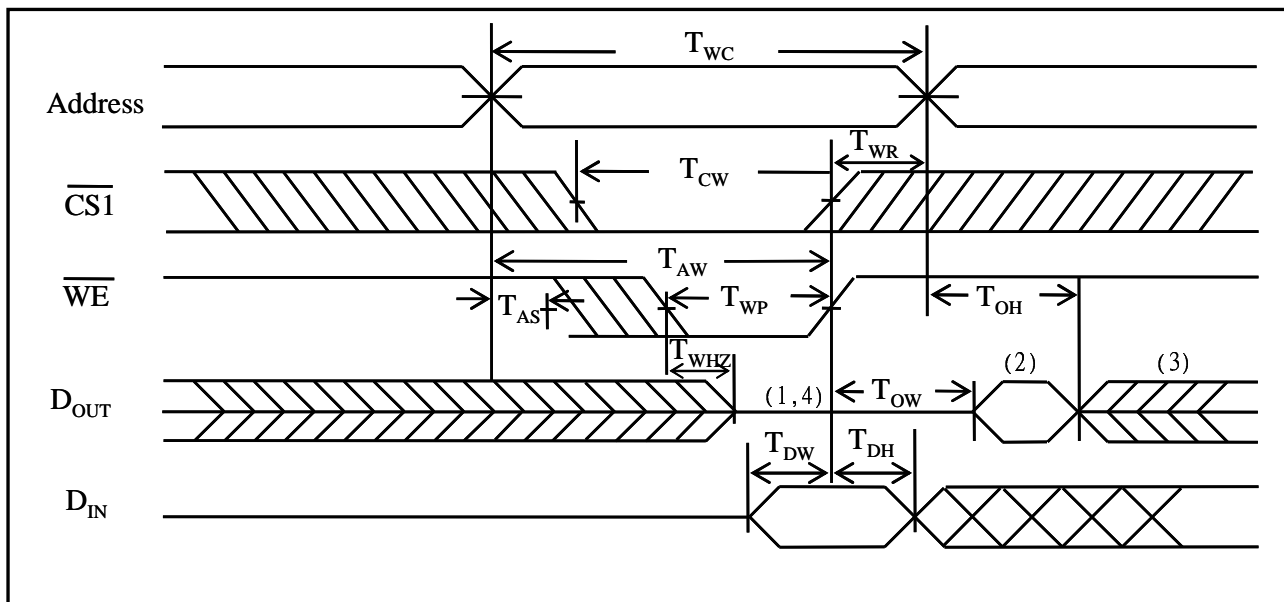


Read Cycle 2
(Chip Select Controlled)



Read Cycle 3
(Output Enable Controlled)



Write Cycle 1
 (\overline{OE} Clock)

 Write Cycle 2
 ($\overline{OE} = V_{IL}$ Fixed)


Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$. This parameter is guaranteed but not 100% tested.