SB61L256AD-XG

Silicon-Based Technology

32,768 × 8-Bits

Very High Speed and Low Power Memory

STATIC CMOS RAM

PRELIMINARY

Description:

The SB61L256AD-XG series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61L256AD-XG series products exhibit very high-speed performance with single +5-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61L256AD-XG is packed in a standard 28-pin 400mil PDIP with Pb-free and Green package materials.

Features:

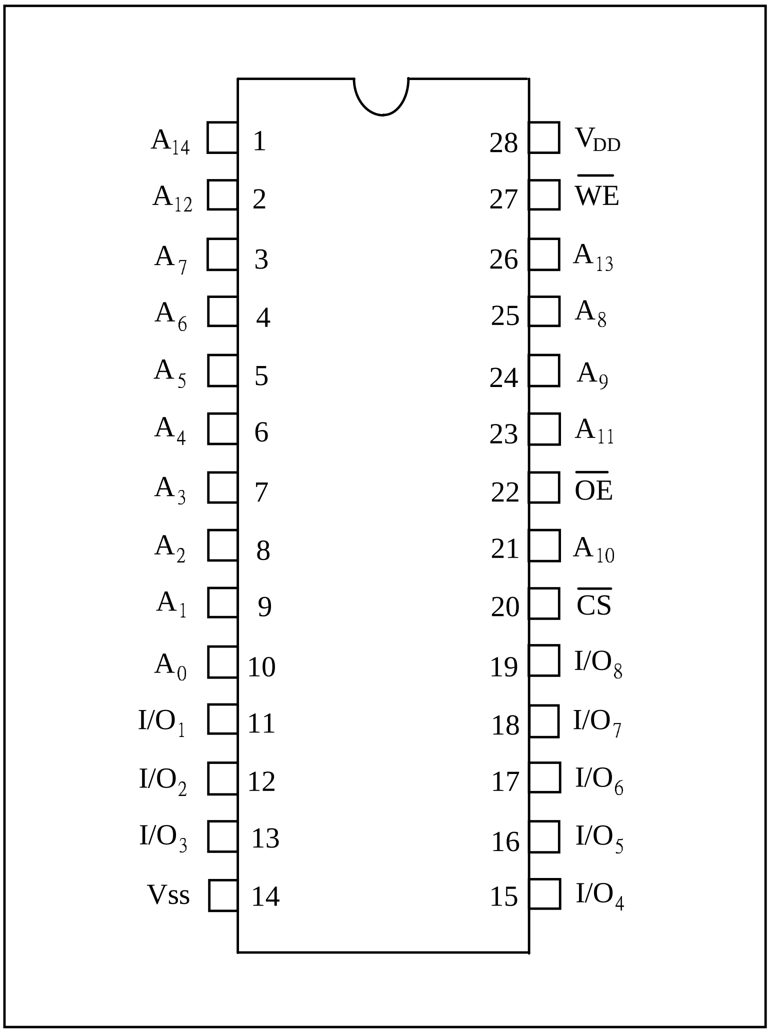
- 32,768-word x 8-bit organization
- Single +5-volt power supply
- Fully static operation — no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
  - — Active: 180/160/140 mA（Max.）
  - — Standby: 5 mA
- Pb-free and Green package materials
- Very high speed access: 8/10/12 ns（Max.）
- 28-pin plastic 400 mil PDIP green package
- Output Enable（$\overline{\text{OE}}$）available for very fast access

Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61L256AD-8G	28-Pin Plastic DIP（400 mil）	32K×8 bits	8	5V±5%	180	5
SB61L256AD-10G			10		160	
SB61L256AD-12G			12		140	

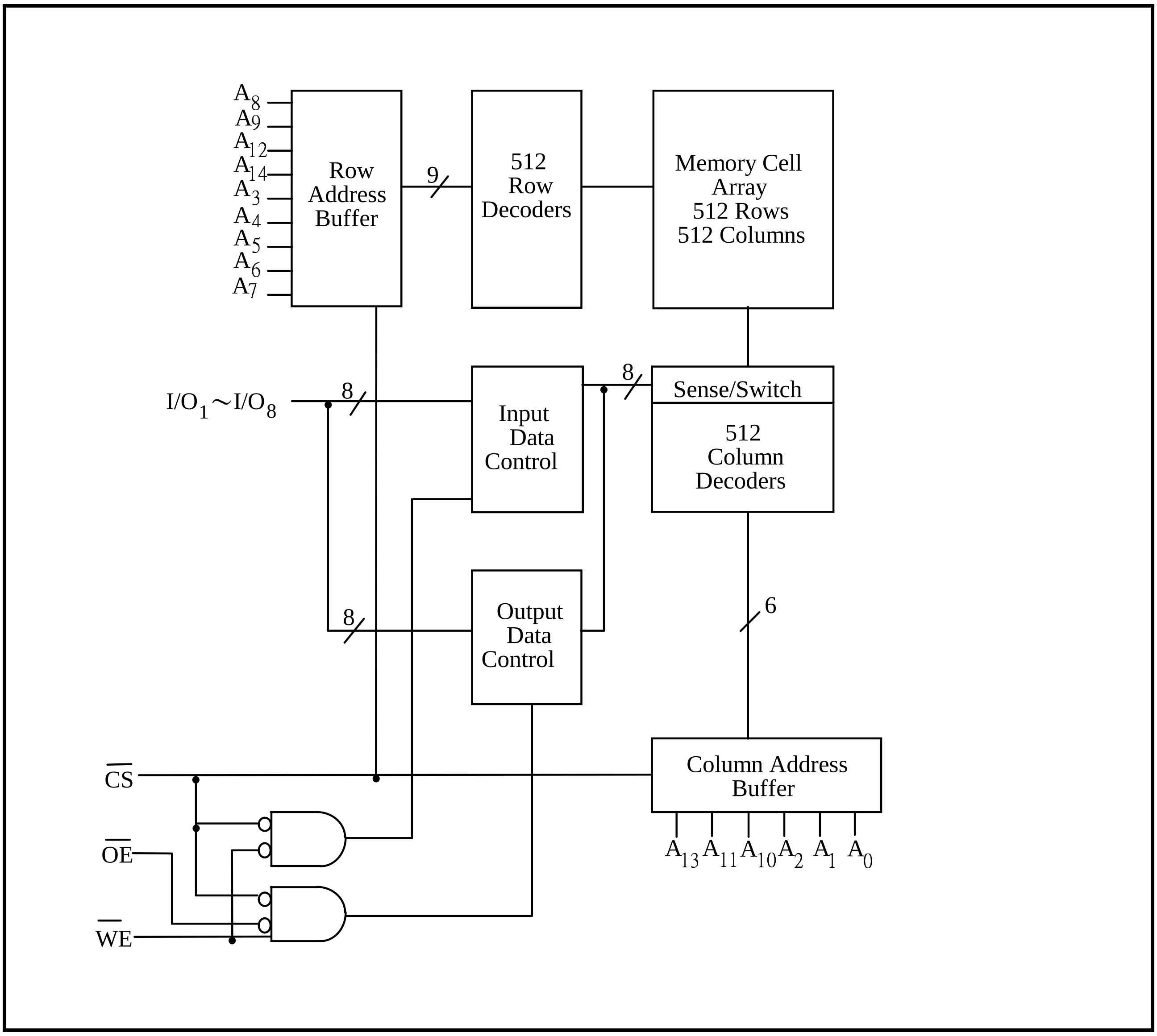
The information in this document is subject to change without notice

Pin Configuration: 28-Pin 400 mil PDIP



Symbols	**Functions**
$A_0 \sim A_{14}$	Address Inputs
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground

Block Diagram:



Truth Table:

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O$_1$～I/O$_8$	V_{DD} Current
H	X	X	Not Selected	High Z	I_{SB},I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

DC Characteristics:

Absolute Maximum Ratings

Parameters	Rating	Uuit
Supply Voltage to Vss	-0.5 to +7.0	V
Input/Output to Vss	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

Operating Characteristics:

(V_{DD} = 5V ± 5%, Vss = 0V, Ta = 0 to 70℃)

Parameters	Symbols	Test Conditions		Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}	-		-0.3	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.6	-	V_{DD}+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-10	-	+10	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	+0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		+2.8	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA Cycle = MIN , Duty = 100%	8	-	-	180	mA
			10	-	-	160	mA
			12	-	-	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle = MIN Duty = 100%		-	-	15	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{DD} -0.2V		-	-	5	mA

Note: Typical characteristics are measured at VDD = 5V, Ta = 25℃

AC Characteristics:

Capacitances

(V_{DD} = 5V, Ta = 25℃, f = 1 MHz)

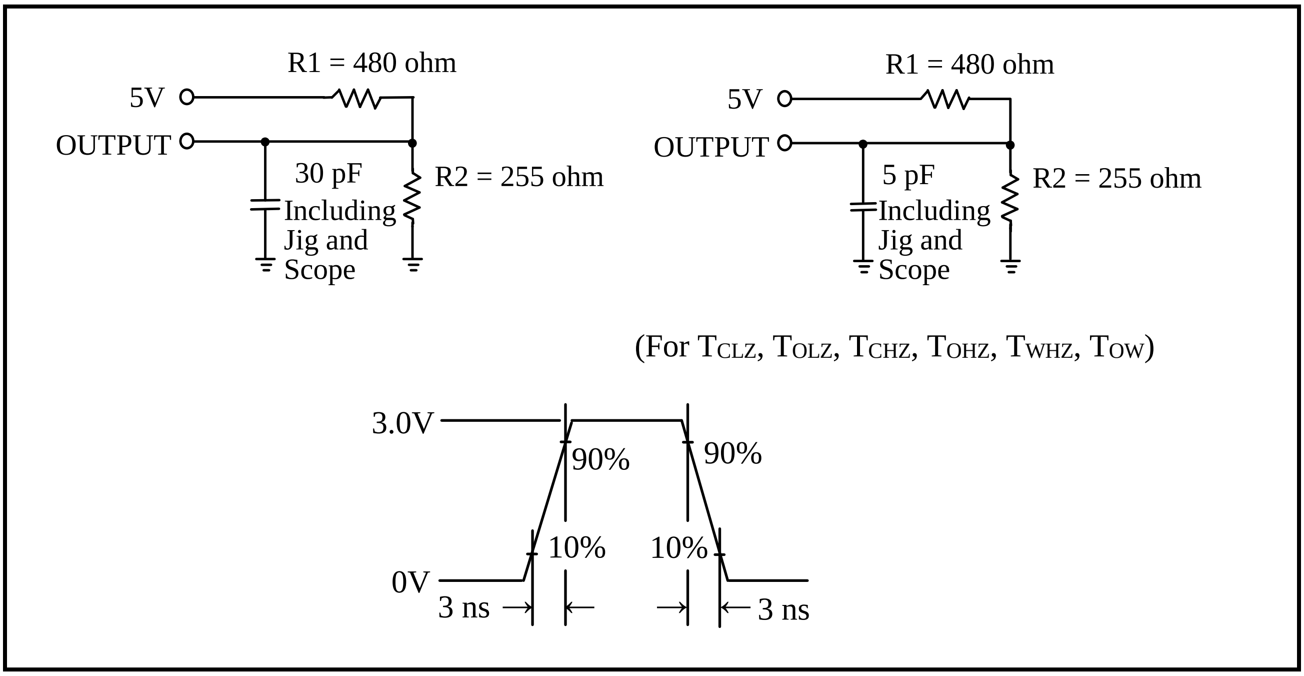
Parameters	**Symbols**	**Conditions**	**Max.**	**Unit**
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

AC Test Conditions

Parameters	**Conditions**
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveforms



AC Performances:

(V_{DD} = 5V ± 5%, V_{SS} = 0V, Ta = 0 to 70℃)

(1) Read Cycle

Parameters	**Symbols**	**SB61L256AD-8G**		**SB61L256AD-10G**		**SB61L256AD-12G**		**Unit**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
Read Cycle Time	T_{RC}	8	-	10	-	12	-	ns
Address Access Time	T_{AA}	-	8	-	10	-	12	ns
Chip Select Access Time	T_{ACS}	-	8	-	10	-	12	ns
Output Enable to Output Valid	T_{AOE}	-	5	-	6	-	7	ns
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T_{CHZ}*	-	4	-	5	-	6	ns
Output Disable to Output in High Z	T_{OHZ}*	-	4	-	5	-	6	ns
Output Hold from Address Change	T_{OH}	3	-	3	-	3	-	ns

*These parameters are sampled but not 100% tested

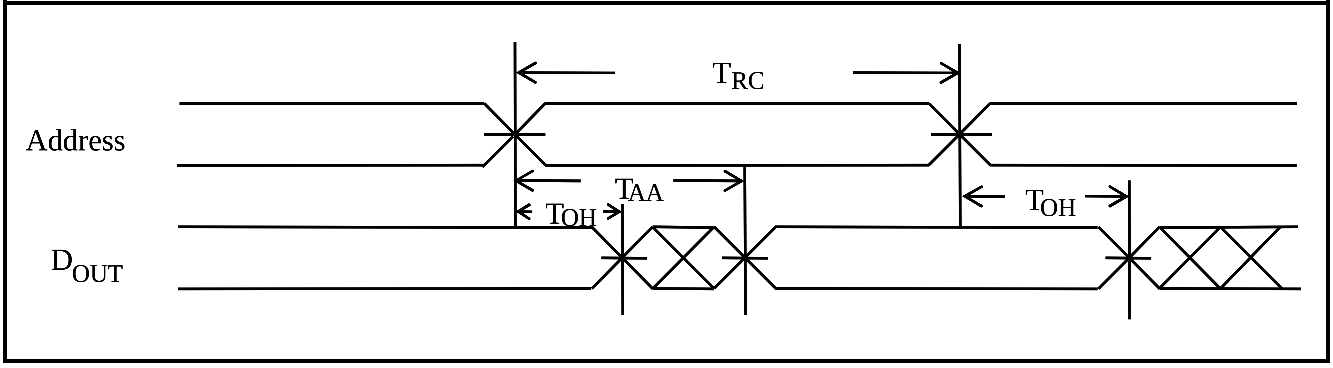
(2) Write Cycle

Parameters	**Symbols**	**SB61L256AD-8G**		**SB61L256AD-10G**		**SB61L256AD-12G**		**Unit**
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
Write Cycle Time	T_{WC}	8	-	10	-	12	-	ns
Chip Selection to End of Write	T_{CW}	6	-	8	-	10	-	ns
Address Valid to End of Write	T_{AW}	6	-	8	-	10	-	ns
Address Setup Time	T_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	T_{WP}	6	-	8	-	10	-	ns
Write Recovery Time	T_{WR}	0	-	0	-	0	-	ns
Data Valid to End of Write	T_{DW}	4	-	6	-	8	-	ns
Data Hold from End of Write	T_{DH}	0	-	0	-	0	-	ns
Write to Output in High Z	T_{WHZ}*	-	4	-	5	-	6	ns
Output Disable to Output in High Z	T_{OHZ}*	-	4	-	5	-	6	ns
Output Active from End of Write	T_{OW}	0	-	0	-	0	-	ns

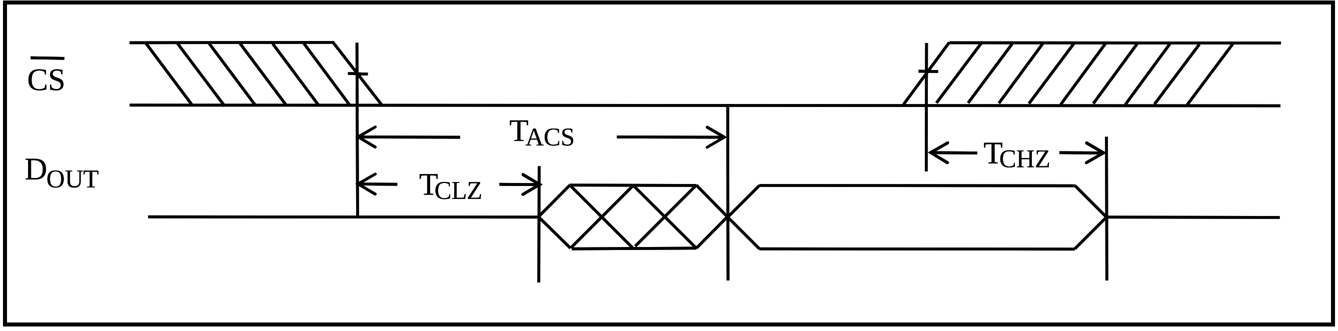
* These parameters are sampled but not 100% tested

Timing Waveforms

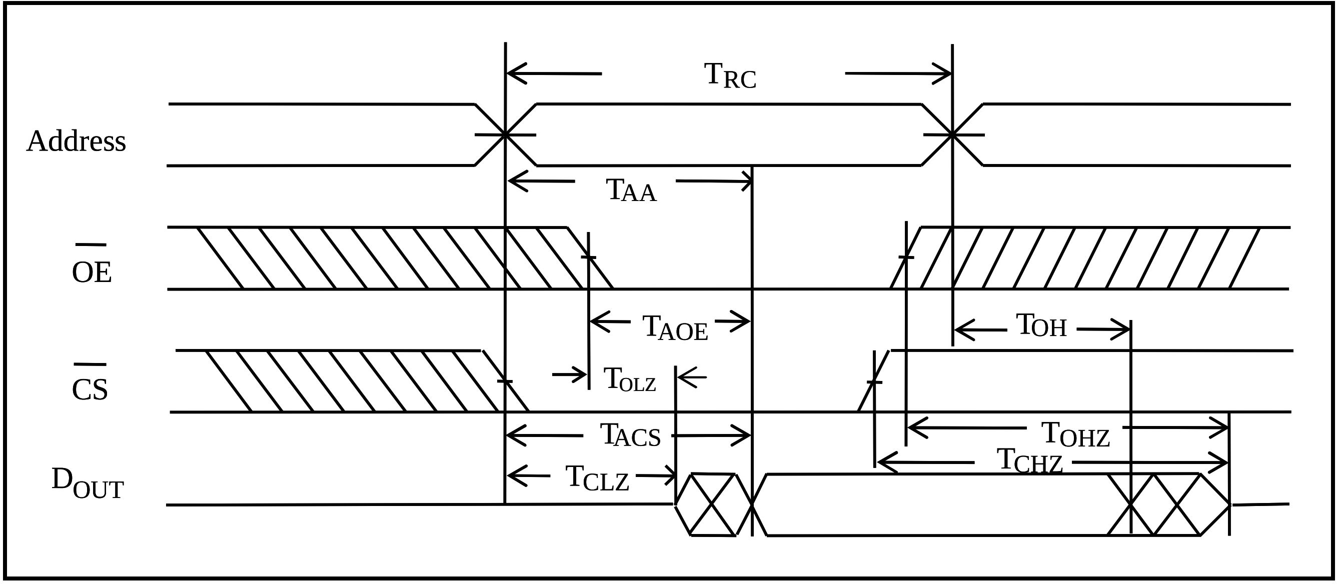
Read Cycle 1
(Address Controlled)



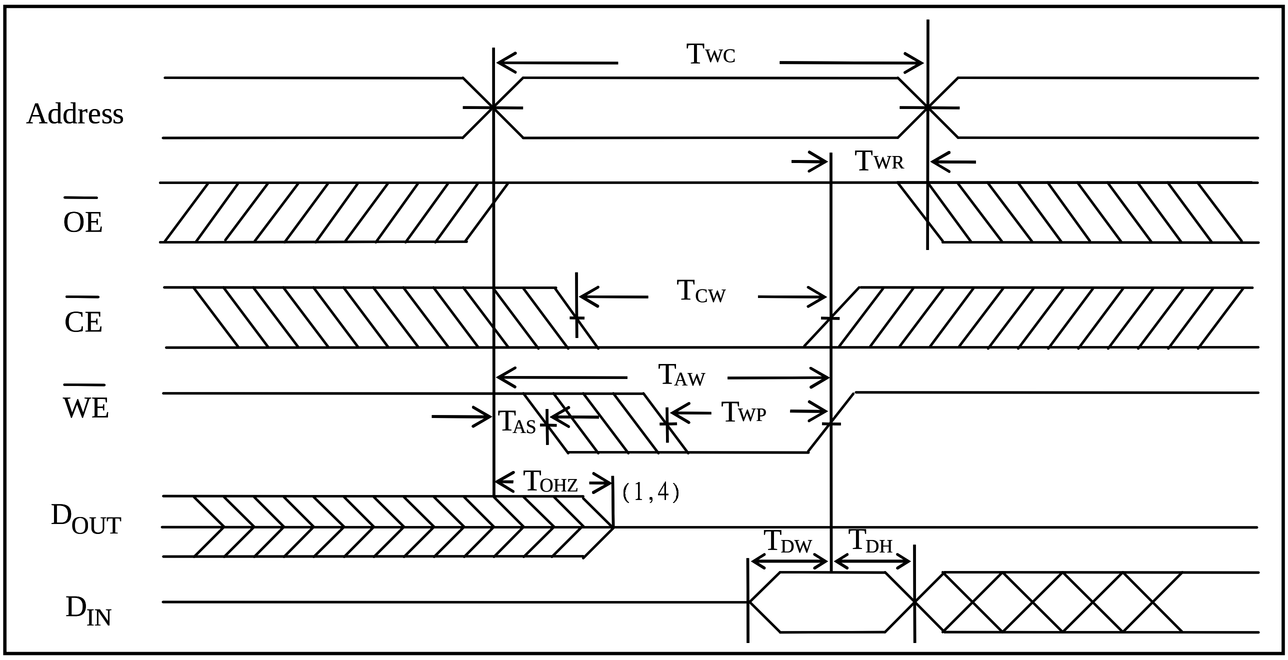
Read Cycle 2
(Chip Select Controlled)



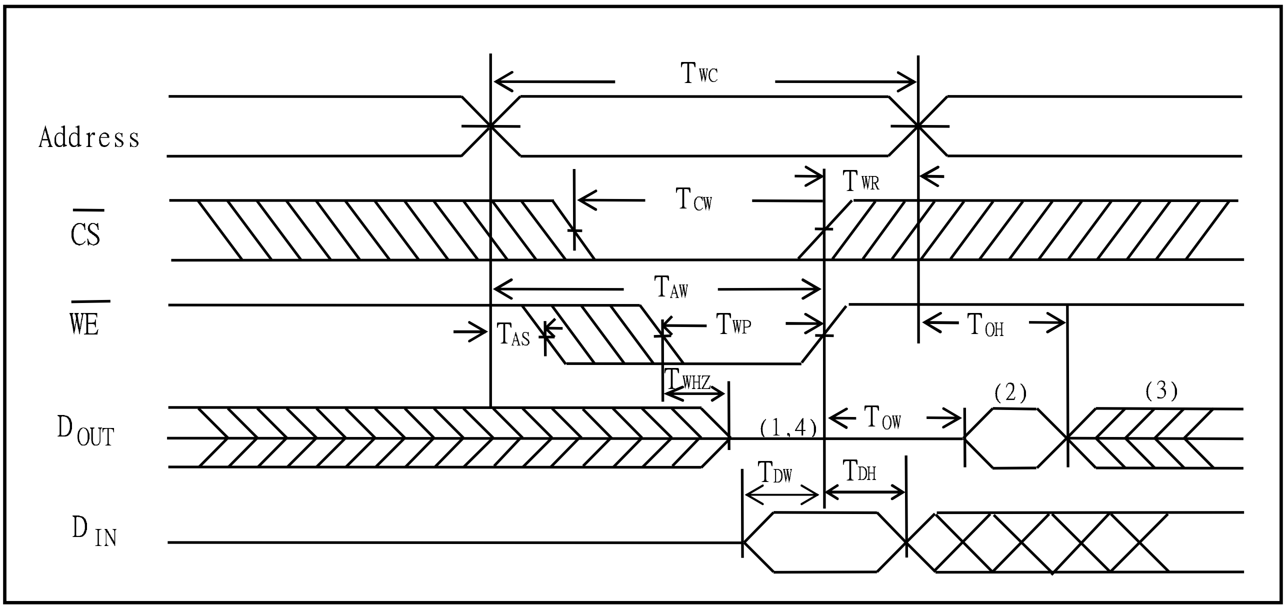
Read Cycle 3
(Output Enable Controlled)



Write Cycle 1
（$\overline{\text{OE}}$ Clock）



Write Cycle 2
($\overline{\text{OE}}$ = V_{IL} Fixed）



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.