Silicon-Based Technology

Very High Speed and Low Power Memory

PRELIMINARY

Description:

The SB61H1024BS series products are 131,072-words by 8-bits static RAM fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61H1024BS series products exhibit very high-speed performance with single +5-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61H1024BS is packed in a standard 32-pin 300mil SOJ and other packages are available upon preorder.

Features:

- 131,072-word x 8-bit organization
- Single +3.3-volt power supply
- Fully static operation ▬ no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
  - ▬Active: 120/100/80 mA（Max.）
  - ▬Standby: 3 mA

- Very high speed access: 10/12/15 ns（Max.）
- 32-pin plastic 300mil SOJ package
- Output Enable（ $\overline{\mathbf{OE}}$ ）available for very fast access

Ordering Information:

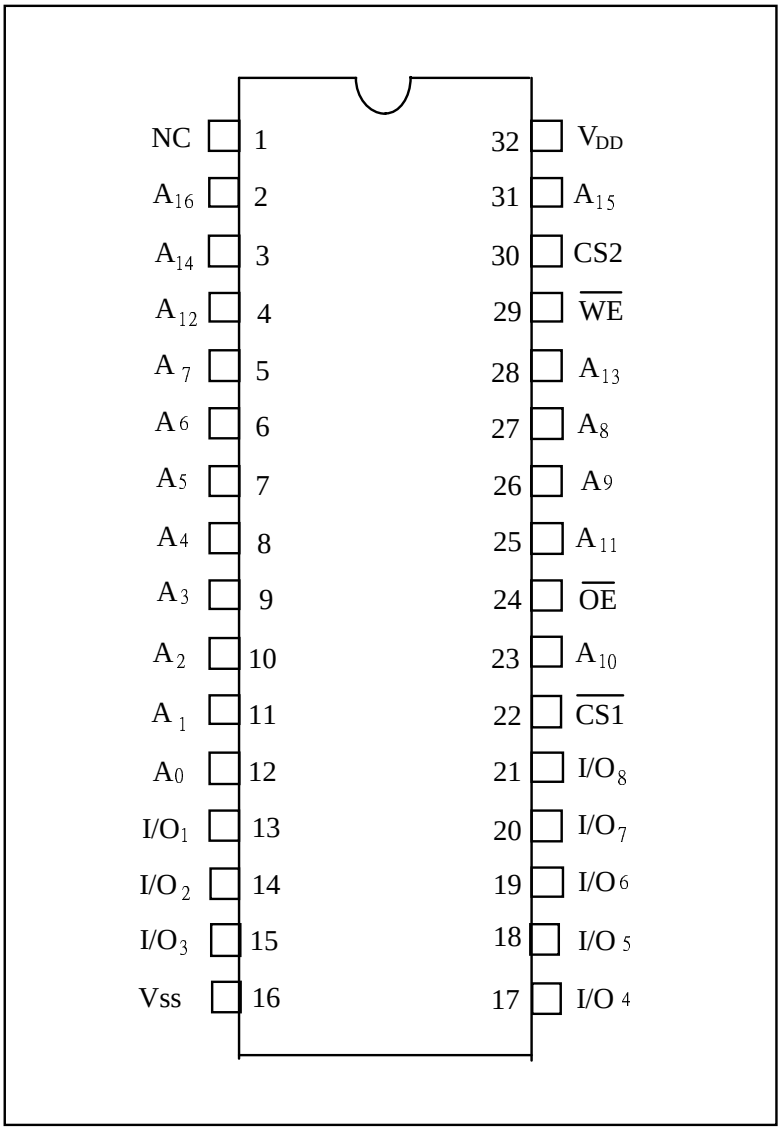
Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61H1024BS-10	32-Pin Plastic SOJ 300mil	128Kx8 bits	10	3.3V±10%	120	3
SB61H1024BS-12			12		100	
SB61H1024BS-15			15		80	

The information in this document is subject to change without notice

Silicon-Based Technology Corporation
1F,No.23, R&D Rd.I, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C. Tel：886-3-5777897
Fax：886-3-5779832

Preliminary

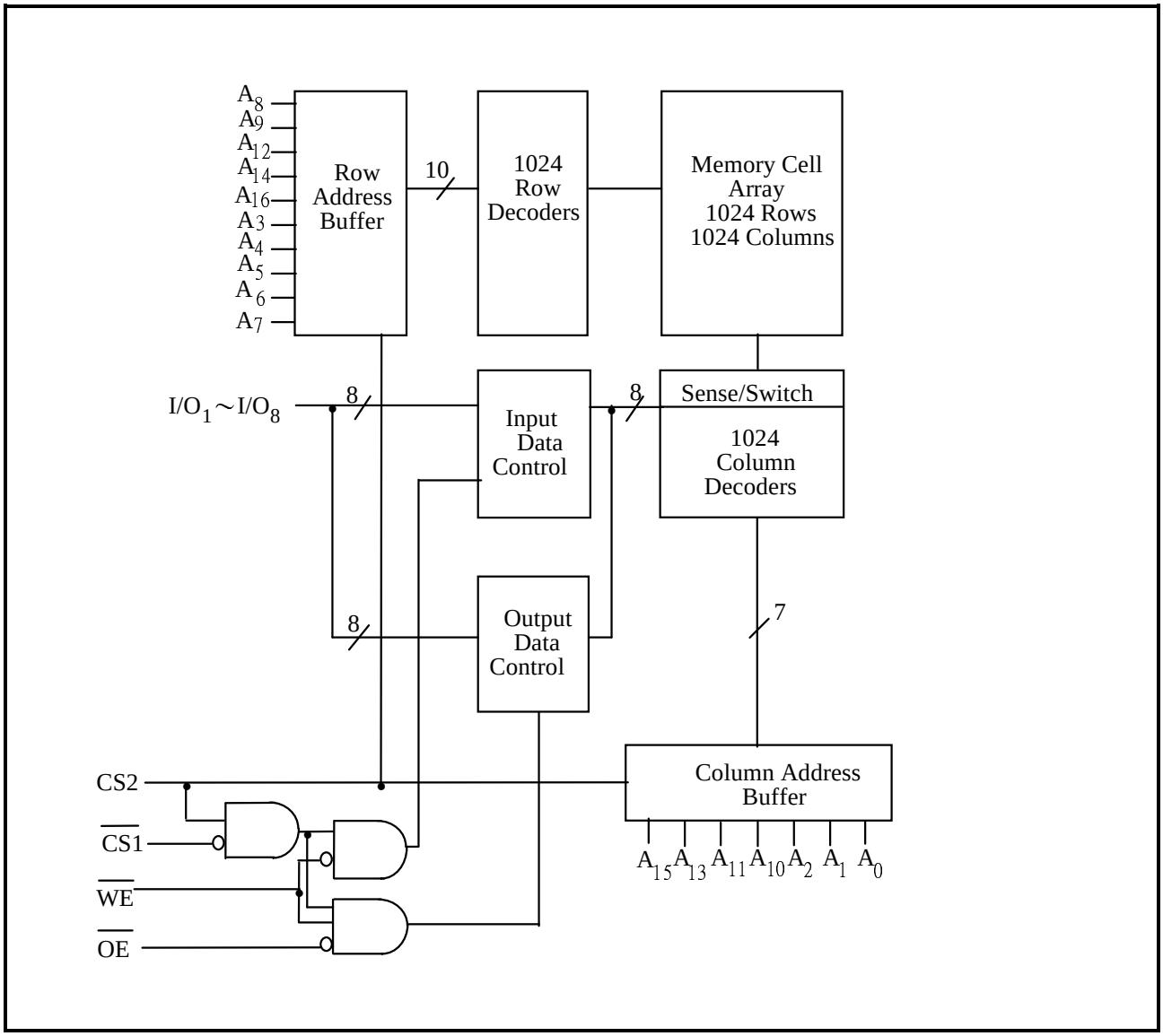
Pin Configuration: 32-Pin 300mil SOJ



Symbols	Functions
A_0～A_{16}	Address Inputs
I/O_1～I/O_8	Data Inputs/Outputs
$\overline{CS1}$,CS2	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground

Preliminary

Block Diagram:



Truth Table:

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1～I/O8	V_{DD} Current
H	X	X	X	Not Selected	High Z	I_{SB},I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB},I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

DC Characteristics:

Absolute Maximum Ratings

Parameters	Rating	Uuit
Supply Voltage to Vss	-0.5 to +7.0	V
Input/Output to Vss	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

Operating Characteristics:

(V_{DD} = 3.3V ± 10%, Vss = 0V, Ta = 0 to 70℃)

Parameters	Symbols	Test Conditions		Min.	Typ.	Max.	Unit
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.7	-	V_{DD}+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{DD}		-10	-	+10	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = Vss to V_{DD}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	+0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		+2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA Cycle = MIN , Duty = 100%	10	-	-	120	mA
			12	-	-	100	mA
			15	-	-	80	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle = MIN Duty = 100%		-	-	10	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{DD} -0.2V		-	-	3	mA

Note: Typical characteristics are measured at V_{DD} = 3.3V, Ta = 25℃

AC Characteristics:

Capacitances

(V_{DD} =3.3V, Ta = 25℃, f = 1 MHz)

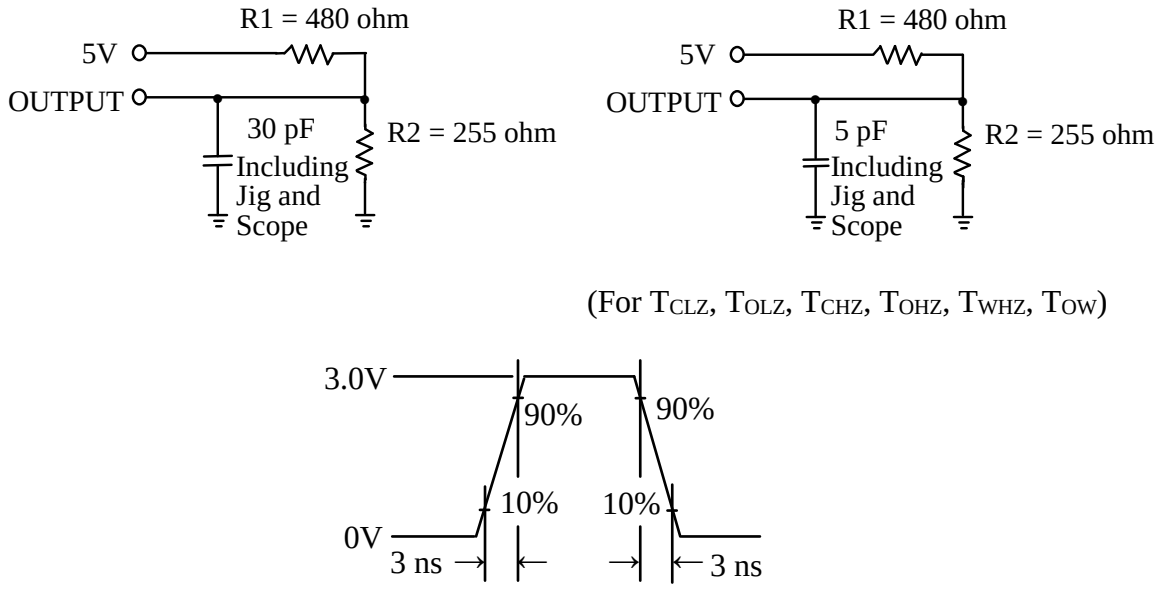
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA/8 mA

AC Test Loads and Waveforms



AC Performances:

(V_{DD} = 3.3V ± 10%, V_{SS} = 0V, Ta = 0 to 70℃)

(1) Read Cycle

Parameters	Symbols	SB61H1024BS-10		SB61H1024BS-12		SB61H1024BS-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}	10	-	12	-	15	-	ns
Address Access Time	T_{AA}	-	10	-	12	-	15	ns
Chip Select Access Time	T_{ACS}	-	10	-	12	-	15	ns
Output Enable to Output Valid	T_{AOE}	-	6	-	7	-	8	ns
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T_{CHZ}*	-	5	-	6	-	7	ns
Output Disable to Output in High Z	T_{OHZ}*	-	5	-	6	-	7	ns
Output Hold from Address Change	T_{OH}	3	-	3	-	3	-	ns

*These parameters are sampled but not 100% tested

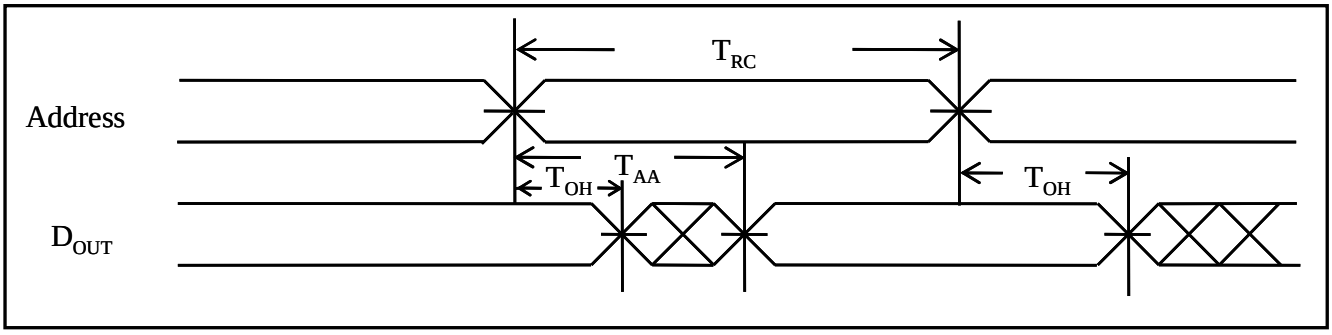
(2) Write Cycle

Parameters	Symbols	SB61H1024BS-10		SB61H1024BS-12		SB61H1024BS-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	10	-	12	-	15	-	ns
Chip Selection to End of Write	T_{CW}	8	-	10	-	12	-	ns
Address Valid to End of Write	T_{AW}	8	-	10	-	12	-	ns
Address Setup Time	T_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	T_{WP}	8	-	10	-	12	-	ns
Write Recovery Time	T_{WR}	0	-	0	-	0	-	ns
Data Valid to End of Write	T_{DW}	6	-	8	-	10	-	ns
Data Hold from End of Write	T_{DH}	0	-	0	-	0	-	ns
Write to Output in High Z	T_{WHZ}*	-	5	-	6	-	7	ns
Output Disable to Output in High Z	T_{OHZ}*	-	5	-	6	-	7	ns
Output Active from End of Write	T_{OW}	0	-	0	-	0	-	ns

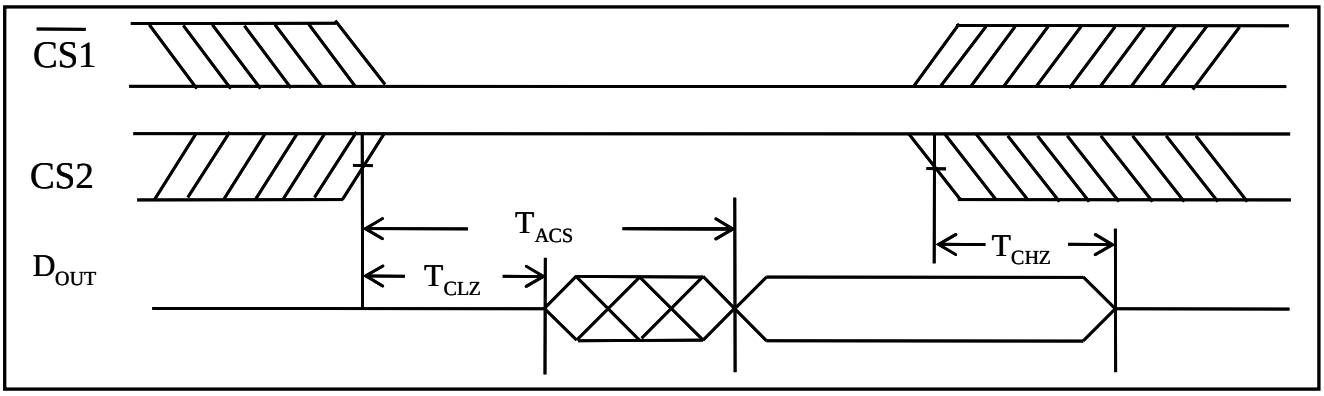
* These parameters are sampled but not 100% tested

Timing Waveforms

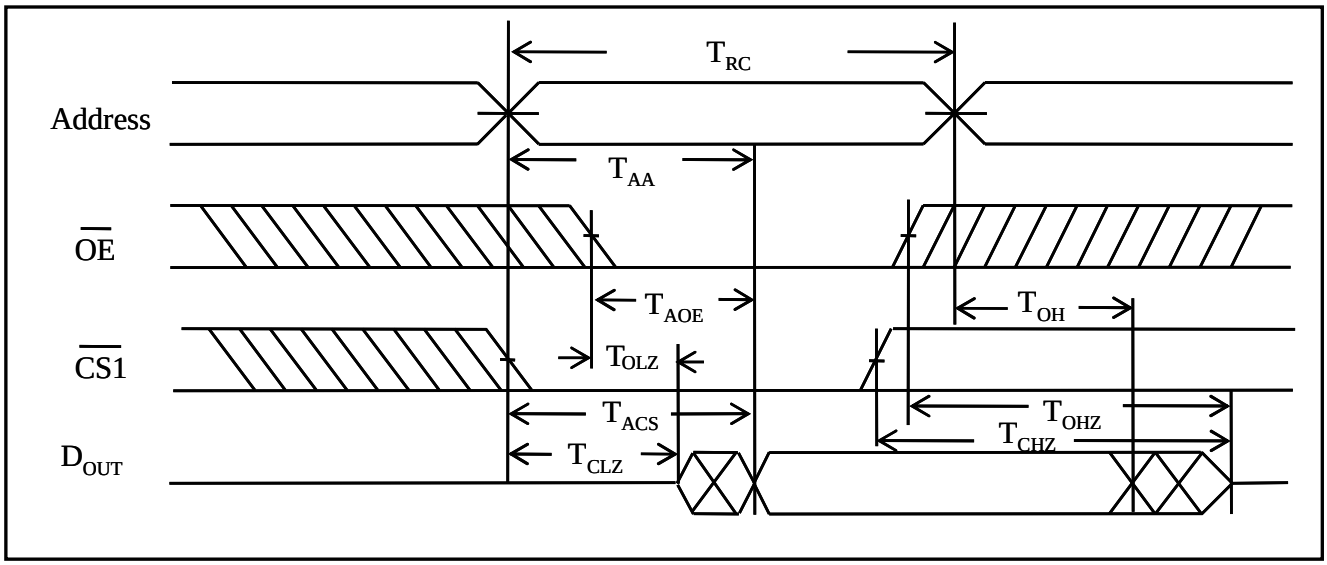
Read Cycle 1
(Address Controlled)



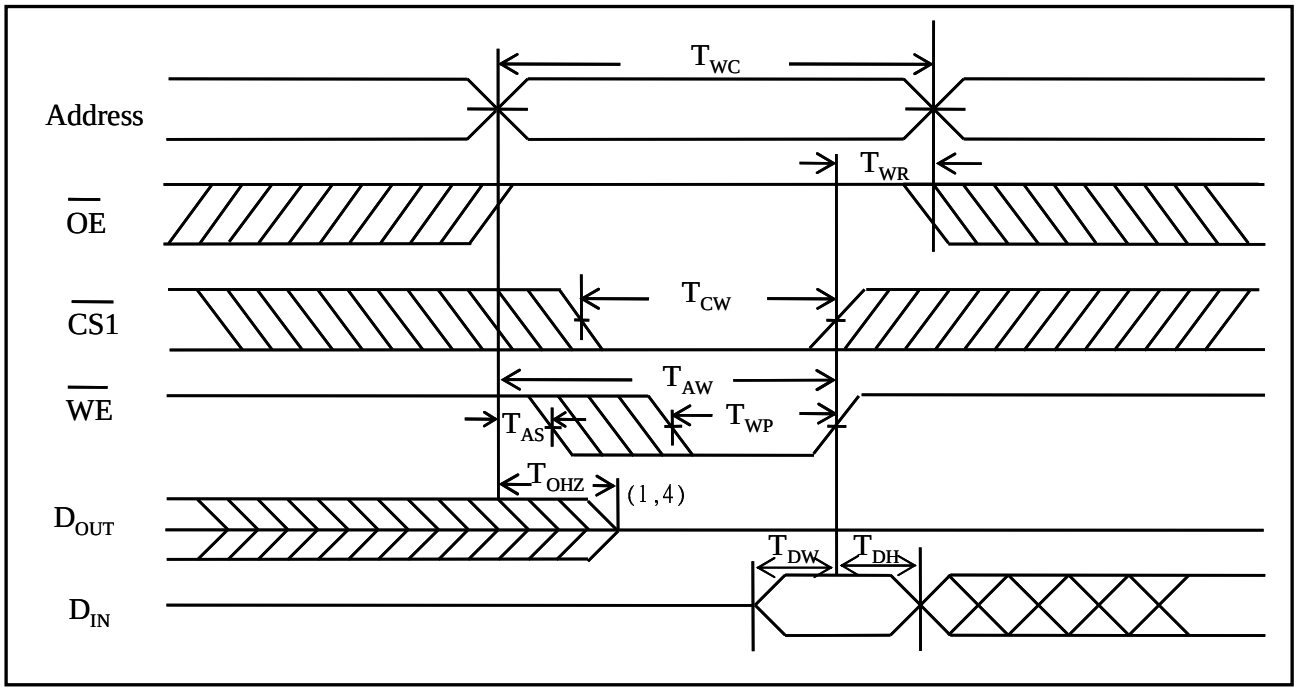
Read Cycle 2
(Chip Select Controlled)



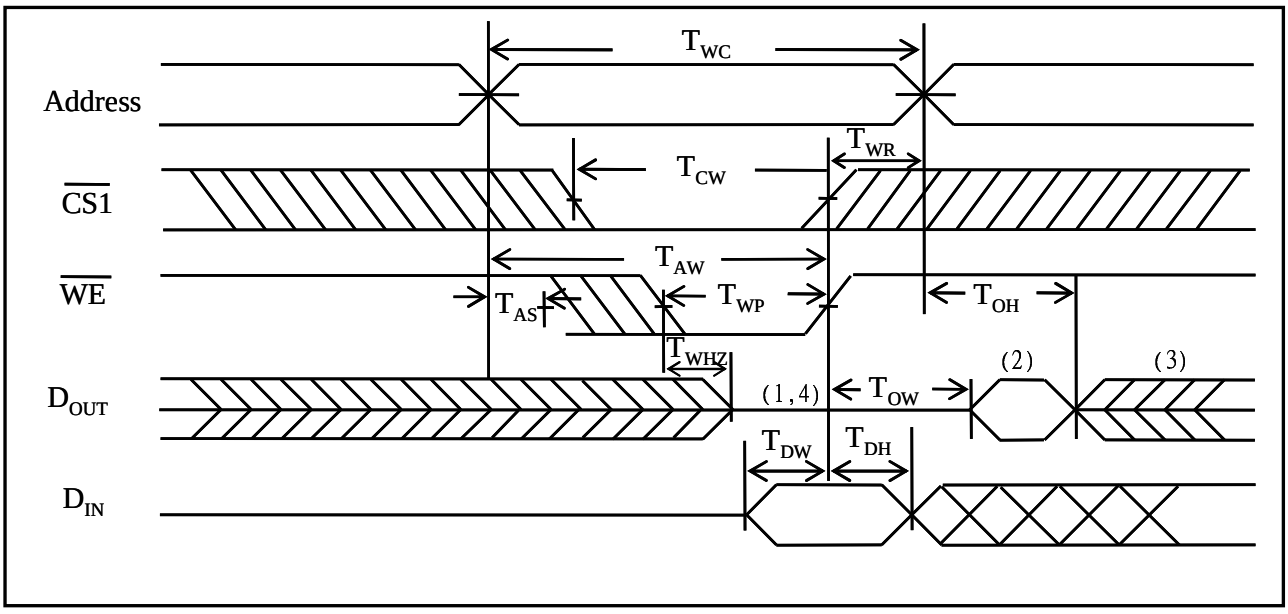
Read Cycle 3
(Output Enable Controlled)



Write Cycle 1
（$\overline{OE}$ Clock）



Write Cycle 2
（$\overline{OE}$ = V_{IL} Fixed）



Notes:
1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.