

Silicon-Based Technology

Ultra High Speed and Low Power Memory

SB61L256BD

32,768 x 8-Bits

STATIC CMOS RAM

PRELIMINARY

Description:

The SB61L256BD series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the SB61L256BD series products exhibit very high-speed performance with single +3.3-volt power supply while requiring very low power and no clock or refreshing to operate. The SB61L256BD is packed in a standard 28-pin 400mil PDIP.

Features:

- 32,768-word x 8-bit organization
- Single +3.3-volt power supply
- Fully static operation \blacksquare no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
 - \blacksquare Active: 100/80/60 mA (Max.)
 - \blacksquare Standby: 1 mA
- Very high speed access: 10/12/15 ns (Max.)
- 28-pin plastic 400 mil PDIP package
- Output Enable ($\overline{\text{OE}}$) available for very fast access

Ordering Information:

Part Number	Package	Word Organization	Access Time ns(Max.)	Supply Voltage (Typ.)	Supply Current mA (Max.)	
					Operating	Standby
SB61L256BD-10	28-Pin Plastic DIP (400 mil)	32Kx8 bits	10	3.3V \pm 5%	100	1
SB61L256BD-12			12		80	
SB61L256BD-15			15		60	

The information in this document is subject to change without notice



Silicon-Based Technology Corporation

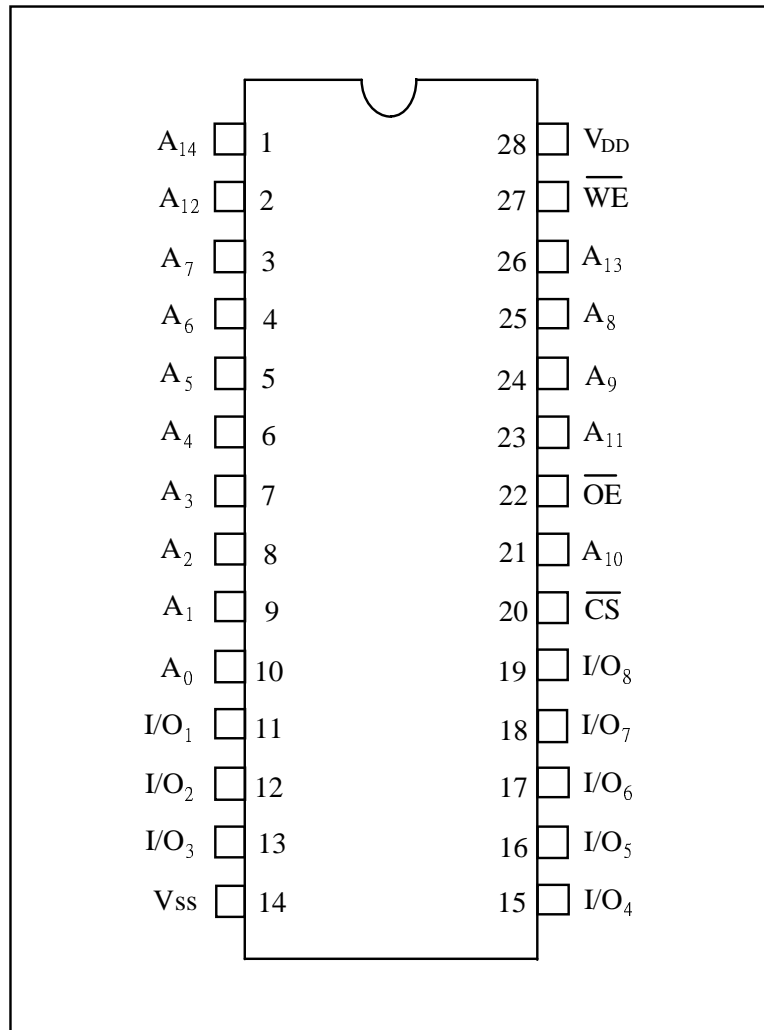
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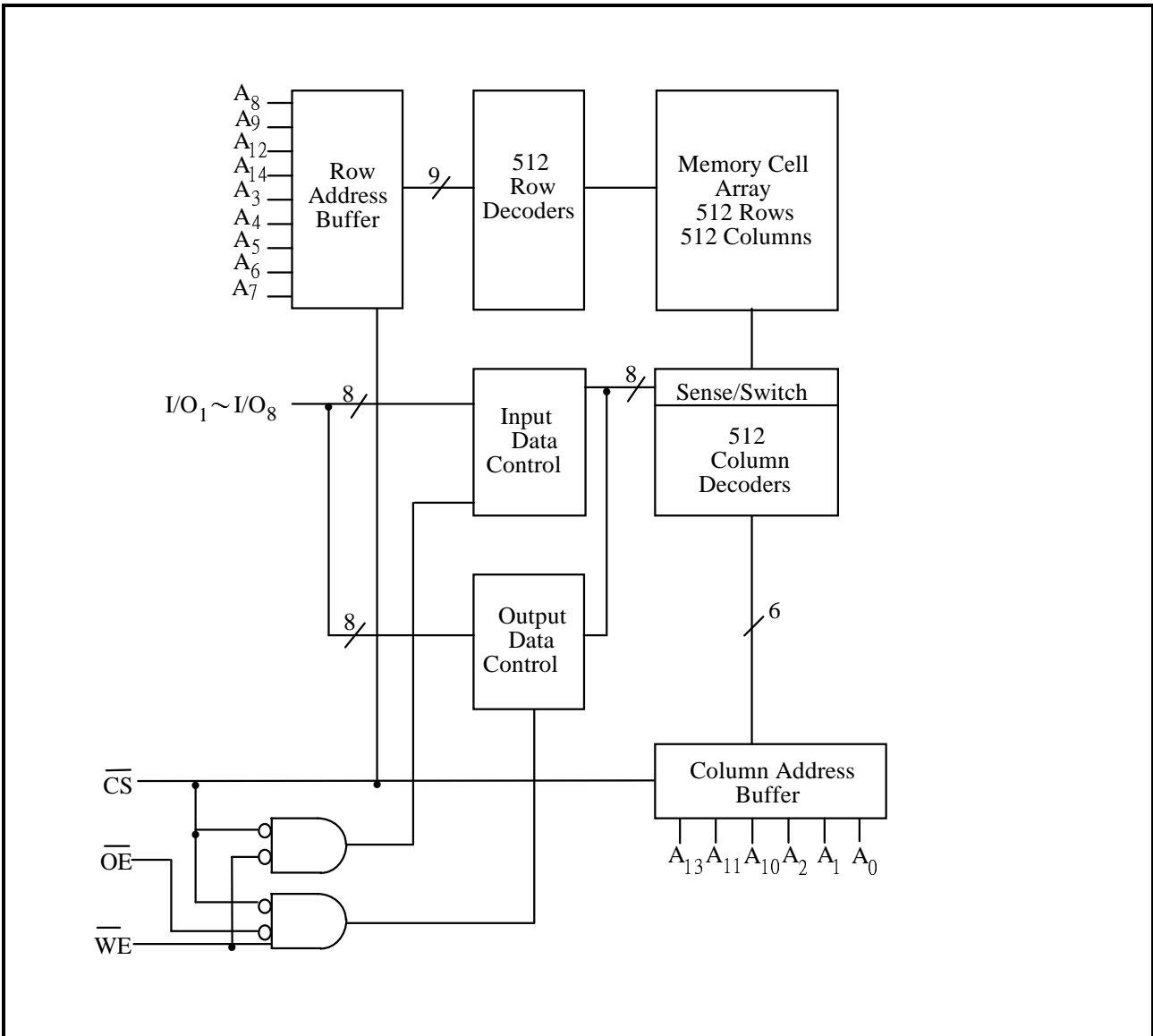
Pin Configuration: 28-Pin 400 mil PDIP



Symbols	Functions
A ₀ ~ A ₁₄	Address Inputs
I/O ₁ ~ I/O ₈	Data Inputs/Outputs
\overline{CS}	Chip Select Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground



Block Diagram:



Truth Table:

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	I/O ₁ ~I/O ₈	V _{DD} Current
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}



DC Characteristics:

Absolute Maximum Ratings

Parameters	Rating	Unit
Supply Voltage to V _{SS}	-0.5 to +4.6	V
Input/Output to V _{SS}	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Operating Characteristics:

(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Parameters	Symbols	Test Conditions	Min.	Typ.	Max.	Unit	
Input Low Voltage	V _{IL}	-	-0.3	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.1	-	V _{DD} +0.3	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-10	-	+10	μA	
Output Low Voltage	V _{OL}	I _{OL} = +8.0mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	-	-	V	
Operating Power Supply Current	I _{DD}	$\overline{CS} = V_{IL}$, I/O = 0 mA Cycle = MIN Duty = 100%	10	-	-	100	mA
			12	-	-	80	mA
			15	-	-	60	mA
Standby Power Supply Current	I _{SB}	$\overline{CS} = V_{IH}$, Cycle = MIN Duty = 100%	-	-	10	mA	
	I _{SB1}	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	1	mA	

Note: Typical characteristics are measured at V_{DD} = 3.3V, T_a = 25°C



AC Characteristics:

Capacitances

($V_{DD} = 3.3V$, $T_a = 25^\circ C$, $f = 1\text{ MHz}$)

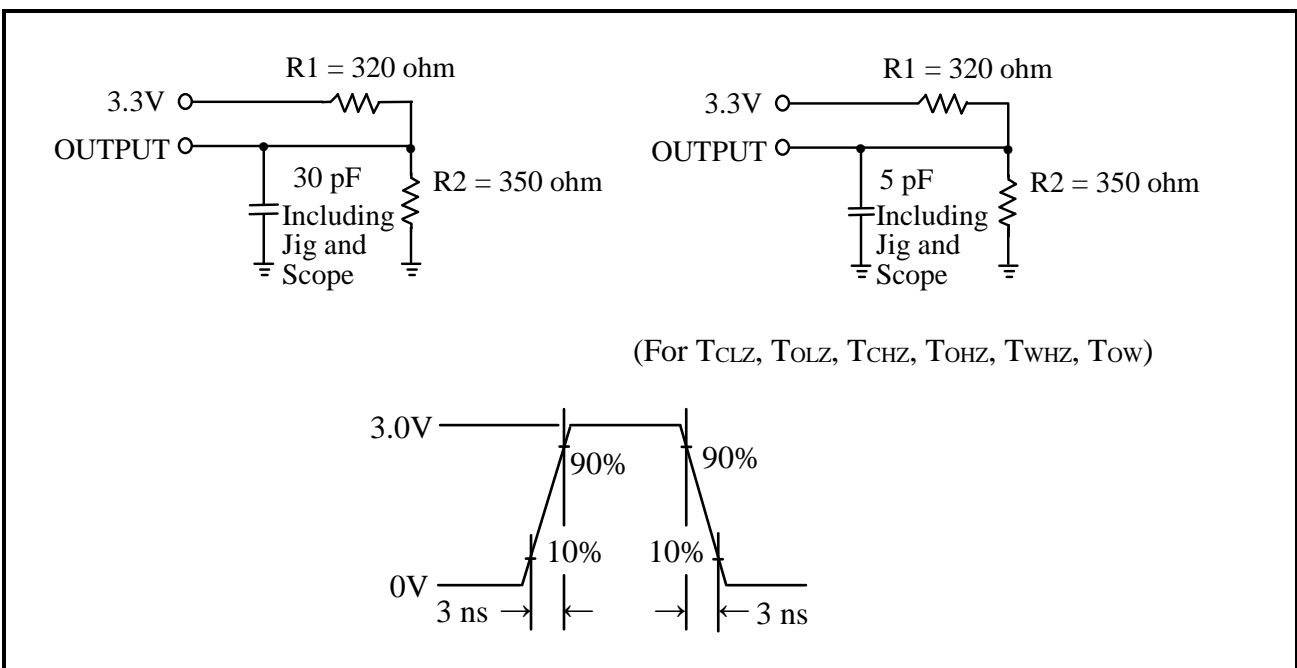
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	8	pF

Note: These parameters are sampled but not 100% tested.

AC Test Conditions

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -4\text{ mA}/8\text{ mA}$

AC Test Loads and Waveforms





AC Performances:

(V_{DD} = 3.3V ± 5%, V_{SS} = 0V, Ta = 0 to 70°C)

(1) Read Cycle

Parameters	Symbols	SB61L256BD-10		SB61L256BD-12		SB61L256BD-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T _{RC}	10	-	12	-	15	-	ns
Address Access Time	T _A A	-	8	-	10	-	12	ns
Chip Select Access Time	T _A C _S	-	8	-	10	-	12	ns
Output Enable to Output Valid	T _A O _E	-	6	-	8	-	10	ns
Chip Selection to Output in Low Z	T _C L _Z *	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	T _O L _Z *	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T _C H _Z *	-	5	-	7	-	9	ns
Output Disable to Output in High Z	T _O H _Z *	-	5	-	7	-	9	ns
Output Hold from Address Change	T _O H	5	-	5	-	5	-	ns

*These parameters are sampled but not 100% tested

(2) Write Cycle

Parameters	Symbols	SB61L256BD-10		SB61L256BD-12		SB61L256BD-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T _W C	10	-	12	-	15	-	ns
Chip Selection to End of Write	T _C W	8	-	10	-	12	-	ns
Address Valid to End of Write	T _A W	8	-	10	-	12	-	ns
Address Setup Time	T _A S	0	-	0	-	0	-	ns
Write Pulse Width	T _W P	6	-	8	-	10	-	ns
Write Recovery Time	T _W R	0	-	0	-	0	-	ns
Data Valid to End of Write	T _D W	8	-	10	-	12	-	ns
Data Hold from End of Write	T _D H	0	-	0	-	0	-	ns
Write to Output in High Z	T _W H _Z *	-	5	-	6	-	8	ns
Output Disable to Output in High Z	T _O H _Z *	-	5	-	6	-	8	ns
Output Active from End of Write	T _O W	0	-	0	-	0	-	ns

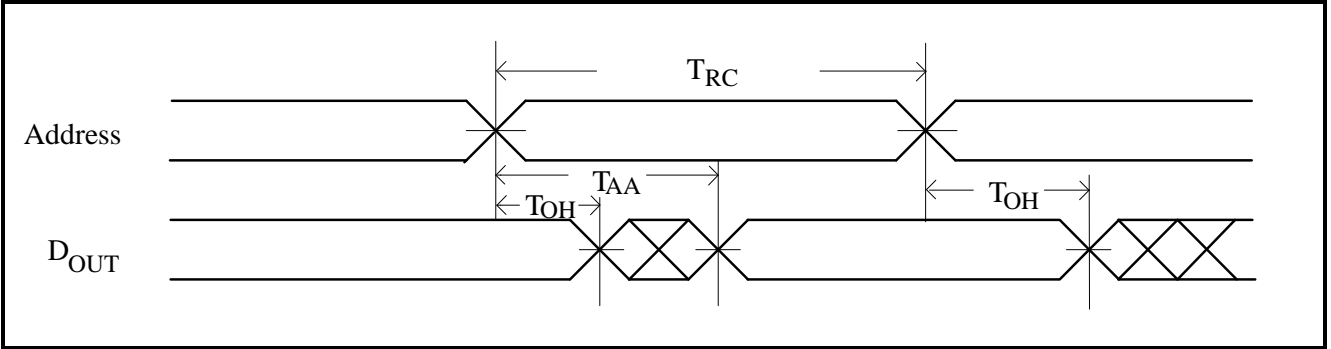
* These parameters are sampled but not 100% tested



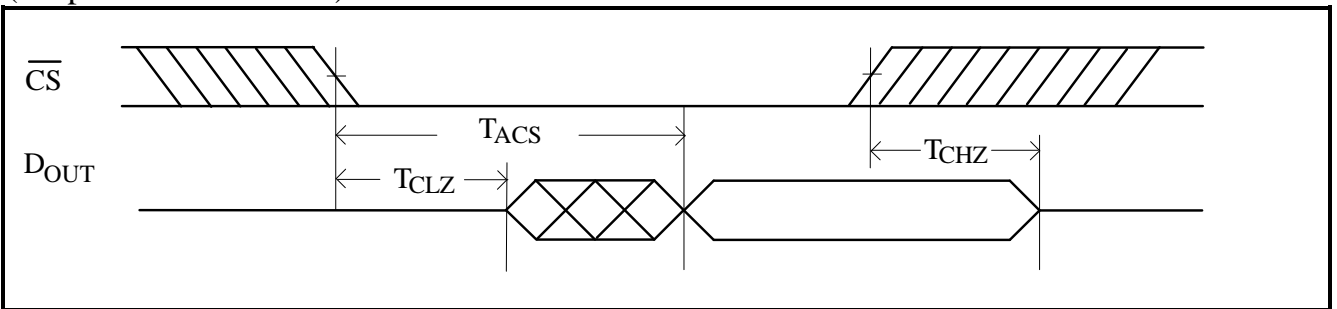
Preliminary

Timing Waveforms

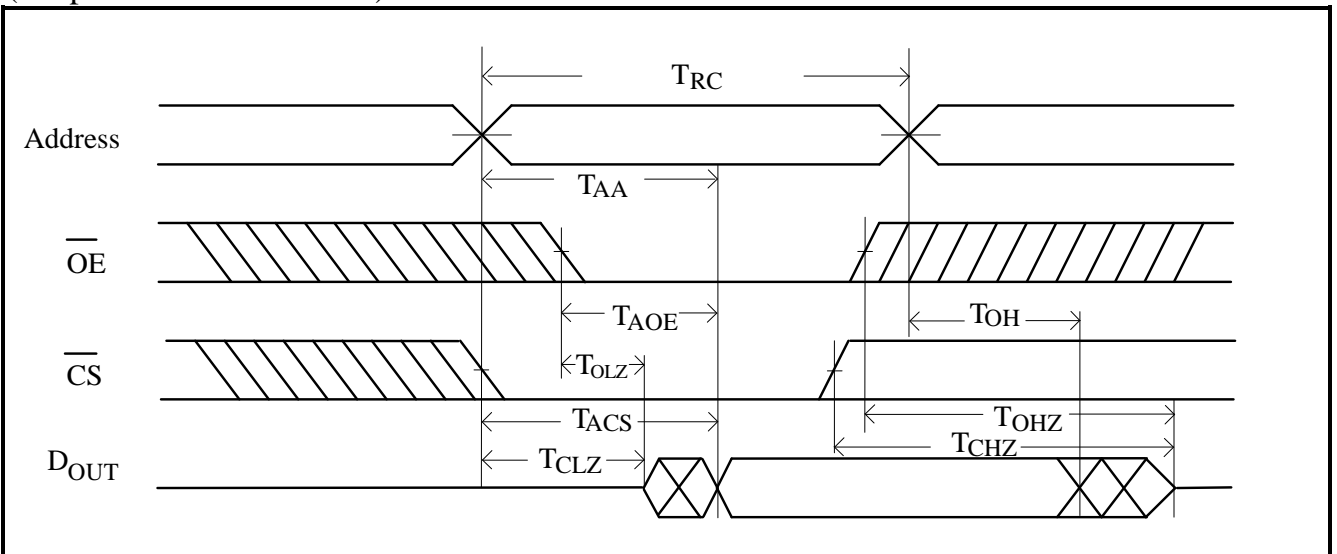
Read Cycle 1
(Address Controlled)



Read Cycle 2
(Chip Select Controlled)

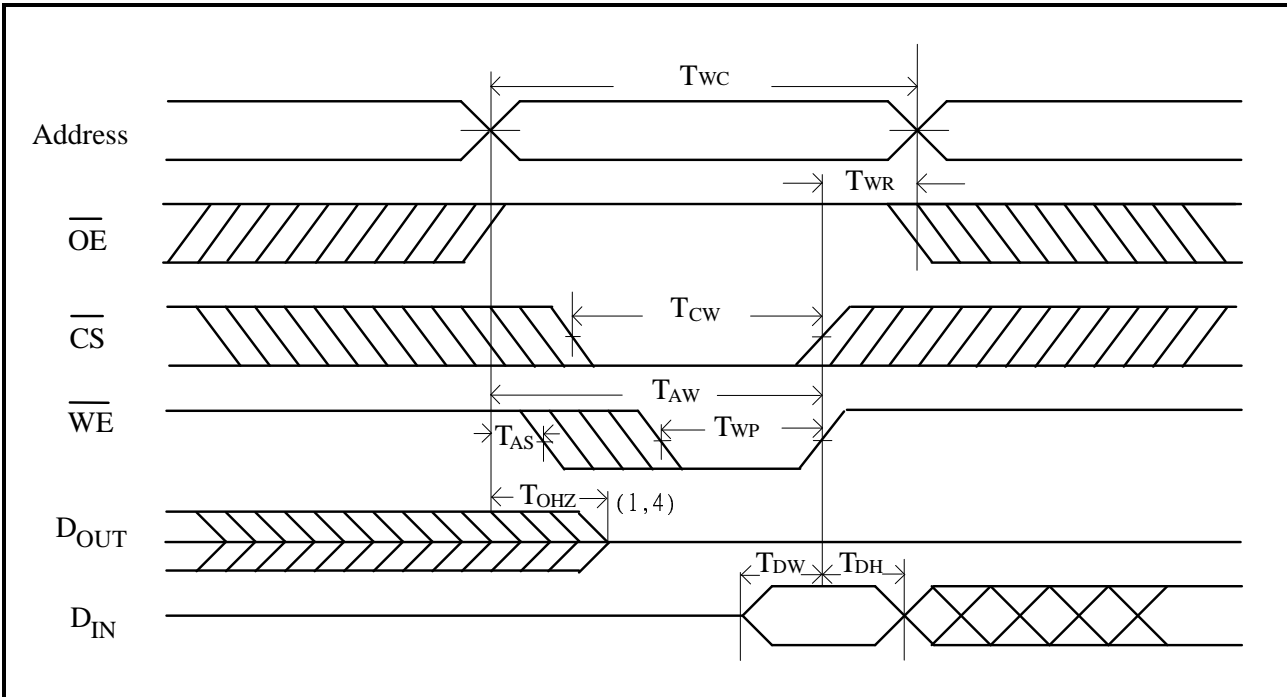


Read Cycle 3
(Output Enable Controlled)

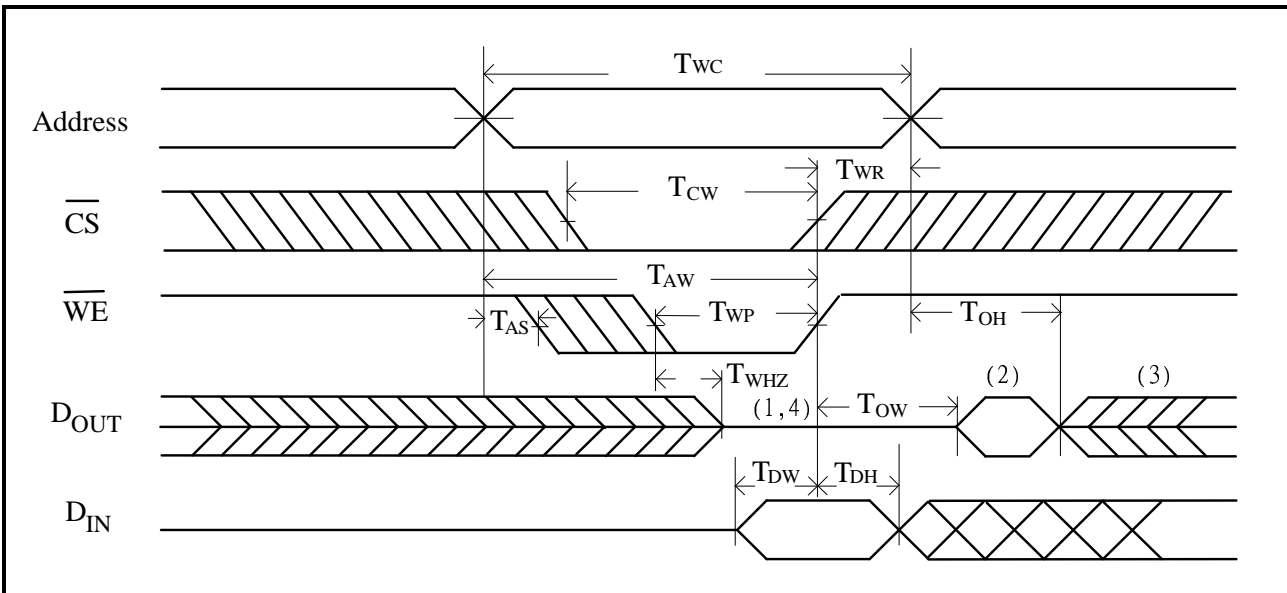




Write Cycle 1 (\overline{OE} Clock)



Write Cycle 2 ($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$. This parameter is guaranteed but not 100% tested.