RS9110-N-11-03 802.11abgn WLAN Module
Data Sheet

Version 1.3
September 2012

Redpine Signals, Inc.
2107 N. First Street, #680
San Jose, CA 95131.
Tel: (408) 748-3385
Fax: (408) 705-2019
Email: info@redpinesignals.com
Website: www.redpinesignals.com

Overview

Overview

The RS9110-N-11-03 module is a complete IEEE 802.11abgn Wi-Fi client device with an integrated MAC, Baseband processor, RF transceiver with power amplifier, and diplexer, T/R switch front-end components. Based on the Redpine Signals RS9110-LI MAC/BBP chip the module provides a complete end-to-end solution for low-power WLAN applications. It includes a multi-threaded processor and a rich set of peripheral interfaces. It can connect to a host processor through SDIO and SPI interfaces.

Applications:

- VOIP handsets
- Interactive remote control devices
- Industrial automation and telemetry
- MP3 music and MP4 video players
- Digital cameras and camcorders

Device Features:

- Conforms to IEEE 802.11a/b/g/e/i/h/j standards, single-stream 802.11 n
- 802.11n MAC features for high user throughput
- 802.11n Space Time Block Code (STBC) support for extended range and higher throughput
- Host interface through SDIO and SPI
- Bluetooth coexistence
- Integrated multi-threaded processor
- TCP checksum offloading
- Rich set of peripherals – UART, SPI, I2C, GPIO, and timers
- 2.4/5 GHz, 802.11n RF transceiver with power amplifier
- Provision for antenna diversity
- Complete WLAN software along with host driver for Windows Embedded CE, Windows XP, and Linux OS
- Single supply 3.1 to 3.6 V operation

RS9110-N-11-03 System Block Diagram

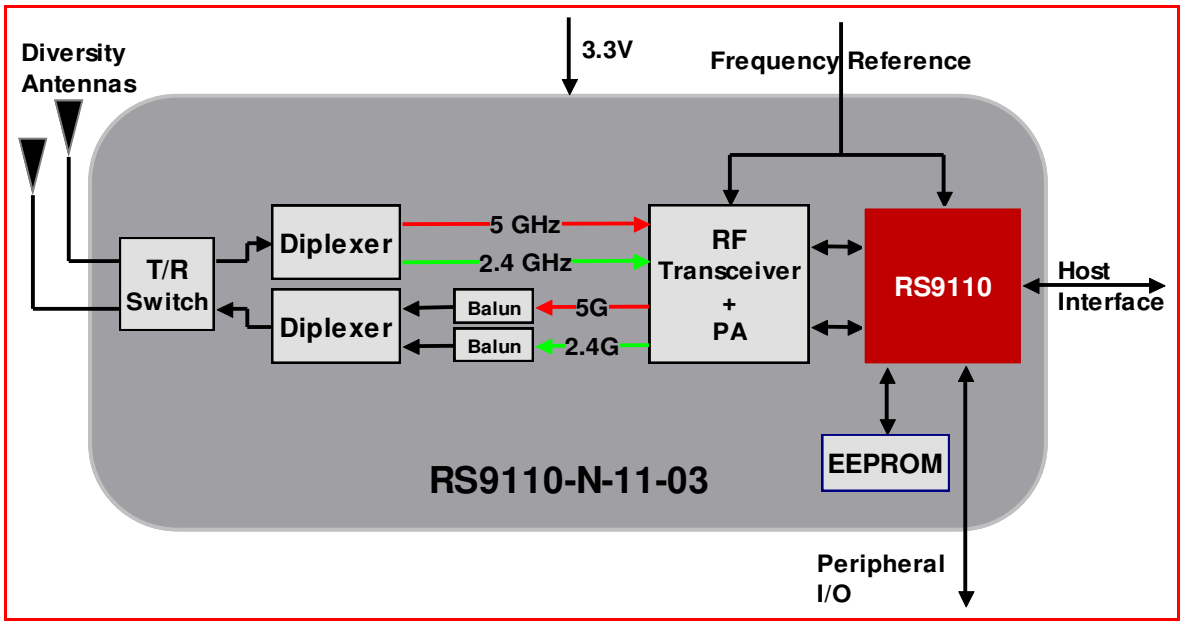


Table of Contents

1: Detailed Feature List 7
1.1: Host Interfaces 7
1.2: WLAN 7
1.2.1: MAC 7
1.2.2: Baseband Processing 7
1.2.3: RF Transceiver 7
1.3: Multi-Threaded Processor 8
1.4: Peripherals 8
1.5: Coexistence 8
1.6: Software 8
1.7: Compliance and Certification 8
2: Package Description 9
2.1: Top View 9
2.2: Bottom View 9
2.3: Package Dimensions 10
2.4: Recommended Reflow Profile 11
2.5: Baking Instructions 11
3: Pin Description 12
3.1: Module Pinout 12
3.2: Pin Description 12
4: Electrical Characteristics 19
4.1: Absolute Maximum Ratings 19
4.2: Recommended Operating Conditions 19
4.3: DC Characteristics – Digital I/O Signals 19
4.4: AC Characteristics 20
4.4.1: SDIO Interface 20
4.4.1.1: Full Speed Mode 20
4.4.1.2: High Speed Mode 20
4.4.2: SPI Interface 21
4.4.2.1: Full Speed Mode 22
4.4.2.2: High Speed Mode 22
4.4.3: JTAG Interface 23
5: Module Power Consumption 25
6: Performance Specifications 27
6.1: Wireless Specifications 27
6.2: Receive Characteristics 27
6.2.1: Sensitivity 27
6.3: Standards Compliance 28
7: Software Details 29
7.1: Architecture 29
7.2: Details 29
7.2.1: 802.1x Supplicant 30
7.2.2: Configuration Utility 30
7.2.3: WLAN Driver 30

7.2.4: HAL- Hardware Abstraction Layer 30
7.2.5: Upper MAC 30
7.2.6: Lower MAC 31
7.3: OS Support 31
8: Ordering Information 32
8.1: Contact Information 32
8.2: Device Ordering Information 32
8.2.1: Device Packaging 32
8.3: Collateral 32

Table of Figures

Figure 1: Top View of the Module 9
Figure 2: Bottom View of the Module 9
Figure 3: Reflow Profile..... 11
Figure 4: Pinout of the Module 12
Figure 5: Interface Timings – SDIO Interface Full-speed Mode 20
Figure 6: Interface Timings – SDIO Interface High-speed Mode 21
Figure 7: SPI Protocol 22
Figure 8: Interface Timings – SPI Interface Full-speed Mode..... 22
Figure 9: Interface Timings – SPI Interface High-speed Mode 23
Figure 10: Interface Timings – JTAG Interface..... 24
Figure 11: RS9110-N-11-03 Software Architecture 29

List of Tables

Table 1: Absolute Maximum Ratings 19
Table 2: Recommended Operating Conditions 19
Table 3: Input/Output DC Characteristics 20
Table 4: AC Characteristics – SDIO Interface Full-speed Mode..... 20
Table 5: AC Characteristics – SDIO Interface High-speed Mode 21
Table 6: AC Characteristics – SPI Interface Full-speed Mode 22
Table 7: AC Characteristics – SPI Interface High-speed Mode..... 23
Table 8: AC Characteristics – JTAG Interface 23
Table 9: Wireless Specification..... 27
Table 10: Receive Sensitivity..... 28

1: Detailed Feature List

1.1: Host Interfaces

- SDIO
  - Version 2.0-compatible
  - Supports SD-SPI, 1-bit, and 4-bit SDIO modes
  - Operation up to a maximum clock speed of 50 MHz
- SPI Interface
  - Operation up to a maximum clock speed of 75 MHz

1.2: WLAN

1.2.1: MAC

- Conforms to IEEE 802.11a/b/g/n/e/i/h/j standards for MAC[1]
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, WPA2-Enterprise, Voice Personal, WPS (PIN/PBC),
- WMM and WMM-PS support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application

1.2.2: Baseband Processing

- Supports DSSS (1, 2 Mbps) and CCK (5.5, 11 Mbps) modes
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, and 54 Mbps)
- Supports IEEE 802.11n single-stream modes with data rates up to 65 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes
- Antenna selection diversity – choice of antenna for transmission and reception; or possibility of providing for separate antennas for 2.4 GHz and 5 GHz bands

1.2.3: RF Transceiver

- Highly integrated 2.4 GHz/5 GHz transceiver with direct conversion architecture
- Receiver with 34 dB RF selectable gain range and 60 dB baseband variable gain range
- Power amplifier with 19 dBm maximum output power.

[1] Compliance to Inter-operatability specifications based on the standard

- Integrated LNA, BPF, and T/R switch

1.3: Multi-Threaded Processor

- RISC-based pipelined architecture
- Non-blocking thread operation
- Processing capability of up to 118 million instructions per second (MIPS) at 118 MHz

1.4: Peripherals

- I2C interface with support for multiple masters and high-speed mode
- SPI peripheral interface
- UART interface with programmable baud-rate generator
- GPIO interface

1.5: Coexistence

- Flexible BT coexistence mechanism with 3-wire hardware interface

1.6: Software

- Drivers for Windows Embedded CE, Windows XP ,Windows 7 ,Android and Linux
- Control and management GUI
- Embedded software for complete WLAN functionality including 802.11n aggregation and Block-ACK, auto rate adaptation, security, and QoS modes

1.7: Compliance and Certification

- Reference design certified for Wi-Fi 802.11n, WPA, WPA2, WPA2-Enterprise, WMM, WMM-PS, WPS, Voice-Personal
- RoHS (Restriction of Hazardous Substances) compliant

2: Package Description

2.1: Top View

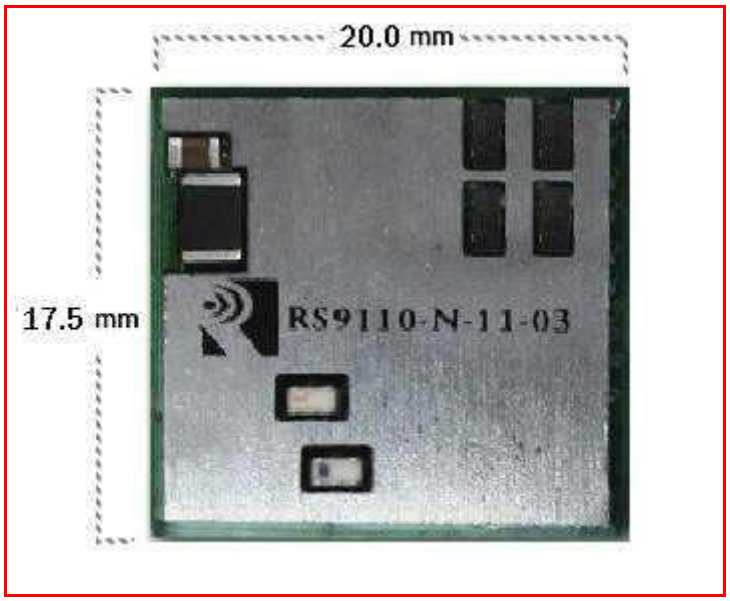


Figure 1: Top View of the Module

2.2: Bottom View

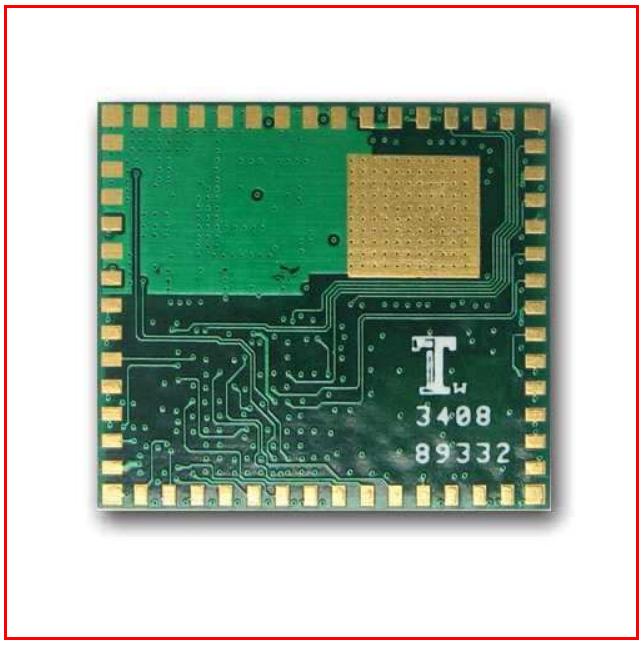
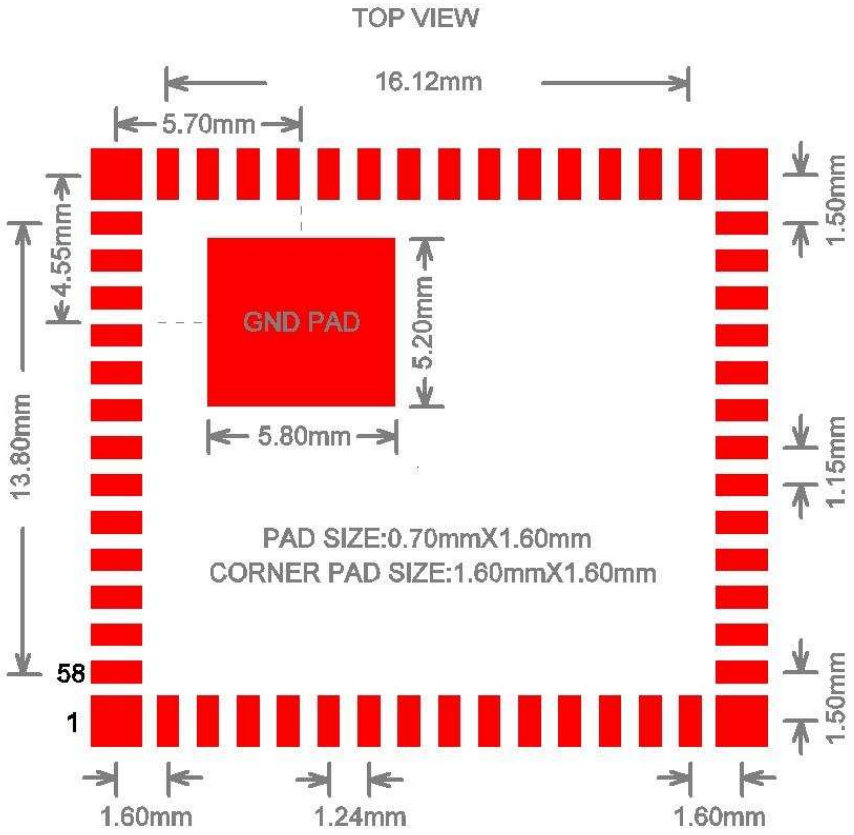


Figure 2: Bottom View of the Module

2.3: Package Dimensions

Note: Module height is 3.45 mm with ± 5% tolerance.



2.4: Recommended Reflow Profile

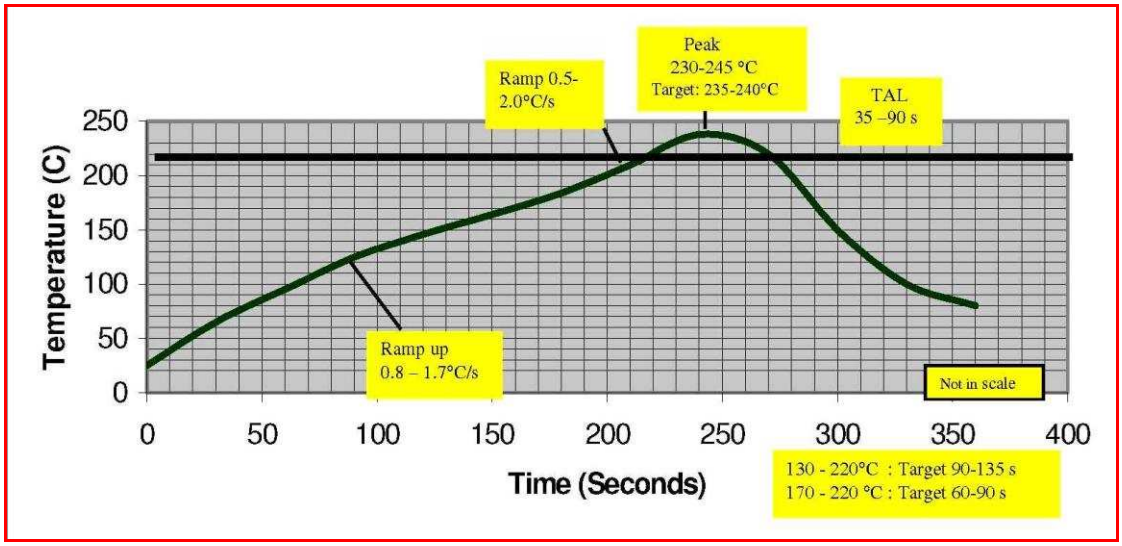


Figure 3: Reflow Profile

Note: The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it.

2.5: Baking Instructions

The RS9110-N-11-03 package is moisture sensitive and devices must be handled appropriately. After the devices are removed from their vacuum sealed packs, they should be taken through reflow for board assembly within 168 hours at room conditions, or stored at under 10% relative humidity. If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125° C.

3: Pin Description

3.1: Module Pinout

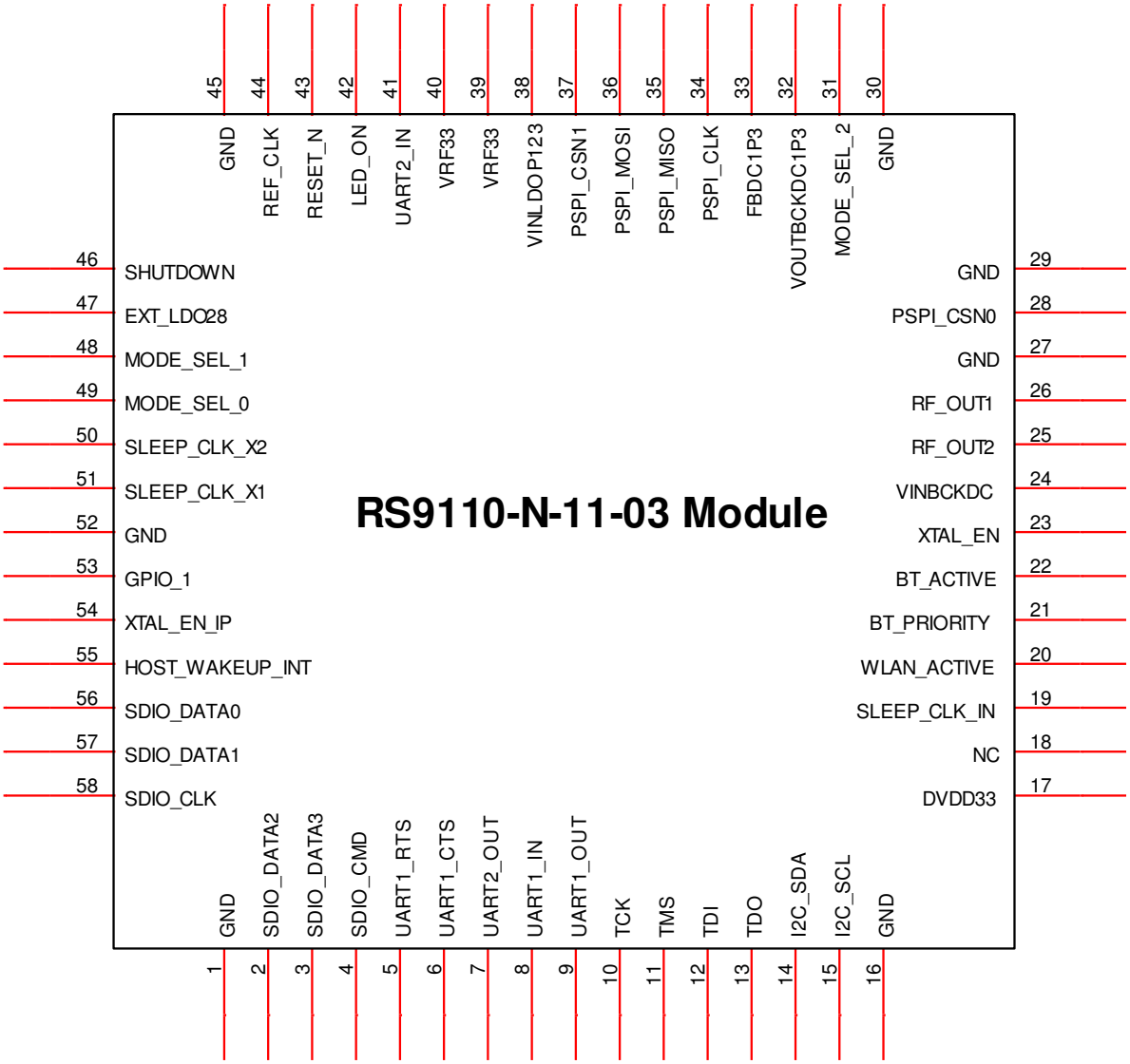


Figure 4: Pinout of the Module

3.2: Pin Description

Pin No.	Pin Name	Pin Type	Description
1)	GND	Ground	Ground

2)	SDIO_DATA2/SPI_INTR	Inout	SDIO 4-bit: Data [2]/Read wait SDIO 1-bit: Read wait SDIO-SPI: SPI_DOUT SPI: SPI_INT[2]
3)	SDIO_DATA3	Inout	SDIO 4-bit: Data [3] SDIO 1-bit: Reserved SDIO-SPI: SPI_INT SPI: Reserved
4)	SDIO_CMD/SPI_CS	Input	SDIO 4-bit: Command/Response SDIO 1-bit: Command SDIO-SPI: SPI_CS SPI: SPI_CS
5)	UART1_RTS	Inout	UART Port1 RTS. This is a firmware configured GPIO pin. Where not used, it should be left open. The default firmware does not use this pin.
6)	UART1_CTS	Inout	UART Port1 CTS. This is a firmware configured GPIO pin. Where not used, it should be left open. The default firmware does not use this pin.
7)	UART2_OUT	Inout	UART Port2 output. This is a firmware configured GPIO pin. Where not used, it should be left open. The default firmware does not use this pin.
8)	UART1_IN	Inout	UART Port1 input. This is a firmware configured GPIO pin. Where not used, it should be left open. The default firmware does not use this pin.
9)	UART1_OUT	Inout	UART Port1 output. This is a firmware configured GPIO pin. Where not used, it should be left open. The default firmware does not use this pin.
10)	TCK	Input	This is a JTAG input pin, and recommended to be connected to ground.
11)	TMS	Input	This is a JTAG input pin, and recommended to be connected to

[2] SPI_INT is used to raise an interrupt, level triggered active_high, upon events in the chip pertaining to SPI host interface.

			ground.
12)	TDI	Input	This is a JTAG input pin, and recommended to be connected to ground.
13)	TDO	Output	This is a JTAG output pin, and recommended to be left open.
14)	I2C_SDA	Inout	I2C Bus Data. By default, and unless firmware is modified, this line is programmed as an output and should be left open.
15)	I2C_SCL	Inout	I2C Bus Clock. By default, and unless firmware is modified, this line is programmed as an output and should be left open.
16)	GND	Ground	Ground
17)	DVDD33	Power	3.3 Volts Input to the I/O Rail
18)	NC	Not Connected	Should be left open
19)	SLEEP_CLK_IN	Inout	Sleep clock input is NC for default firmware. An external 32KHz signal is fed to this pin if the external 32KHz input mode is selected. Please refer to notes on Sleep Clock Input for more details.
20)	WLAN_ACTIVE	Inout	When configured for BT coexistence, this is an output and indicates with logic high that WLAN activity is in progress. When low, BT device has the opportunity to transmit. This is a firmware configured GPIO pin. Where not used, it should be left open.
21)	BT_PRIORITY	Inout	Indicates through 'logic high' that BT is transmitting high priority traffic. This is a firmware configured GPIO pin. Where not used, it should be left open.
22)	BT_ACTIVE	Inout	This signal may be used by an external Bluetooth device to indicate its activity or impending activity. This signal is not used in the default BT coexistence firmware. . This is a firmware

			configured GPIO pin. Where not used, it should be left open.
23)	XTAL_EN	Output	This signal controls an external reference clock oscillator for power-save purposes. 1 – Enable 0 – Disable
24)	VINBCKDC	Power	3.3 Volts input to the Lite-Fi's PMU
25)	RF_OUT2	RFIn/RFOut	Antenna-2 port. 50 ohms impedance.
26)	RF_OUT1	Rfin/Rfout	Antenna-1 Port. 50 ohms impedance
27)	GND	Ground	Ground
28)	NC	No-connect	This pin is to be left unconnected.
29)	GND	Ground	Ground
30)	GND	Ground	Ground
31)	NC	No-connect	This pin is to be left unconnected.
32)	VOUTBCKDC1P3	Power	Internal DC-DC convertor output. A Schottky diode is to be placed on this line for protection.
33)	FBDC1P3	Power	Feedback for the DC-DC Converter
34)	PSPI_CLK	Inout	When enabled as a SPI interface pin, this is the SPI Master clock output. This is a firmware configured GPIO pin. Where not used, it should be left open. Default firmware does not use this pin.
35)	PSPI_MISO	Inout	When enabled as a SPI interface pin, this is the SPI Master data input. This is a firmware configured GPIO pin . Where not used, it should be left open. Default firmware does not use this pin.
36)	PSPI_MOSI	Inout	When enabled as a SPI interface pin, this is the SPI Master data output. This is a firmware configured GPIO pin. Where not used, it should be left open. Default firmware does not use this pin
37)	PSPI_CSN1	Output	When enabled as a SPI interface

			pin, this is the chip-select output from SPI Master. This is a firmware configured GPIO pin. Where not used, it should be left open. Default firmware does not use this pin
38)	VINLDOP123	Power	Input to the LDO's. This has to be connected to FBDC1P3.
39)	VRF33	Power	3.3 Volts input to the RF transceiver
40)	VRF33	Power	3.3 Volts input to the RF transceiver
41)	UART2_IN	Inout	UART-2 Input. This is a firmware configured GPIO pin. Where not used, it should be left open.
42)	LED_ON	Inout	LED Control signal. Indicates activity on WLAN – the device pulls this line low when the module is activated. To be connected to the Cathode of an LED with a recommended series resistor of 820 ohms to VDD. This pin may also be used as a GPIO.
43)	RESET_n	Input	Power on reset. Active low, and required to be active for at least 10 ms.
44)	REF_CLK	Input	Reference Clock source: 40MHz.
45)	GND	Ground	Ground
46)	GND	Ground	Ground
47)	EXT_LDO28	Power	2.8 Volts LDO O/P
48)	MODE_SEL_1	Input	SDIO MODE: No connect. SPI Mode: Connect pull down of 4.7Kohms.
49)	MODE_SEL_0	Input	BOOT MODE: On no-connect, boot parameters will be loaded from internal flash. Should be left unconnected so as to enable bootloading.
50)	SLEEP_CLK_X2	Input	32KHz crystal connection The pin should be left open except as describe in mode (iii) as described in note below for Sleep Clock Input.
51)	SLEEP_CLK_X1	Input	32KHz crystal connection The pin should be left grounded

			except as describe in mode (iii) as described in note below for Sleep Clock Input.
52)	GND	Ground	Ground
53)	GPIO_1	Inout	General purpose input/output. In the default configuration this is programmed as an output and should be left unconnected.
54)	XTAL_EN_IP	Inout	This is a GPIO signal by default and it should be left open. If used, it can be configured through firmware to be combined, through a logical OR operation, with the internal oscillator enable and the output given on XTAL_EN pin. This can be used when a crystal oscillator is shared between the WLAN module and other functional blocks in the system.
55)	HOST_WAKEUP_INT	Inout	This pin is a GPIO. If this is not used, it should be left open. This pin is to be used by those hosts which enter into power save mode and which are not able to detect the regular interrupt pin in that power save mode. If used as HOST_WAKEUP_INT, a pull-up or pull-down of 100K has to be connected on this pin based on the polarity indicated to the firmware. Active low requires a pull-up. Active high requires a pull-down.
56)	SDIO_DATA0/MOSI	Inout	SDIO 4-bit: Data [0] SDIO 1-bit: Data line SDIO-SPI: SPI_DIN (MOSI) SPI: SPI_DIN
57)	SDIO_DATA1/MISO	Inout	SDIO 4-bit: Data [1]/Interrupt SDIO 1-bit: Interrupt SDIO-SPI: Reserved SPI: SPI_DOUT
58)	SDIO_CLK/SPI_CLK	Input	SDIO/SPI interface clock input

Notes:

- Some interfaces are not used in the default configuration or mode of operation. These include the I2C, GPIO, and UART interfaces. These may be used in custom applications with appropriate firmware. These are all fundamentally Inout signals and may be configured either as input or output.
- JTAG functionality is not included in default firmware.
- The Bluetooth coexistence interface (BT_PRIORITY, WLAN_ACTIVE, BT_ACTIVE) are also general purpose I/O signals and may be reprogrammed to be inputs or outputs as needed. Please refer to BT coexistence application note for more details.
- Sleep Clock Input:

  By default, an internal 32KHz oscillator is used, so this pin can be open.

  This should be a 32 kHz clock and is used in power-save modes, if chosen.

  During the low power sleep state, the module's wake-up timer uses the sleep clock – which can have one of three sources

  i) an internal 32 kHz oscillator- Default option, leave open

  ii) a 32 kHz clock fed into this pin,

  iii) a 32 kHz crystal connected to pins SLEEP_CLK_X2 and SLEEP_CLK_X1. In this case the pin should be left open.

  This is a firmware configured GPIO pin and where not used, should be left open.

  NOTE: The recommended mode of operation is i).

- Please refer to the Module Integration Guide document for reference schematics and the list of recommended part numbers.
- Please contact Redpine for application notes or for customization of a solution.

4: Electrical Characteristics

4.1: Absolute Maximum Ratings

Absolute maximum ratings in the table given below are the values beyond which the device could be damaged. Functional operation at these conditions or beyond these conditions is not guaranteed.

Parameter	Symbol	Value	Units
Input Supply voltage	Vin	3.6	V
Supply voltage for I/O Rail	DVDD33	3.6	V
Supply Voltage for the RF	VRF33	3.6	V
RF Input Level	RFIN	10	dBm
Storage temperature	T_{store}	-65 to 150	°C
PA Output Load Mismatch		10:1	
Electrostatic discharge tolerance (MM)	ESD_{MM}	200	V
Electrostatic discharge tolerance (CDM)	ESD_{CDM}	500	V
Electrostatic discharge tolerance (HBM)	ESD_{HBM}	2000	V

Table 1: Absolute Maximum Ratings

4.2: Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Input supply voltage	V_{IN}	3.1	3.3	3.6	V
Supply voltage for I/O Rail	DVDD33	3.1	3.3	3.6	V
Supply voltage for the RF	VRF33	3.1	3.3	3.6	V
Ambient temperature	T_a	-40	25	85	°C

Table 2: Recommended Operating Conditions

4.3: DC Characteristics – Digital I/O Signals

Parameter	Min.	Typ.	Max.	Units
Input high voltage	2	-	5.5	V
Input low voltage	-0.3	-	0.8	V

Parameter	Min.	Typ.	Max.	Units
Output low voltage	-	-	0.4	V
Output high voltage	2.4	-	-	V
Input leakage current (at 3.3V or 0V)	-	-	±10	µA
Tristate output leakage current (at 3.3V or 0V)	-	-	±10	µA

Table 3: Input/Output DC Characteristics

4.4: AC Characteristics

4.4.1: SDIO Interface

4.4.1.1: Full Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK	Tsdio	0		25	MHz
SDIO_DATA, input setup time	Ts	5	-	-	ns
SDIO_DATA, input hold time	Th	2	-	-	ns
SDIO_DATA, clock to output delay	Tod	5	-	11	ns

Table 4: AC Characteristics – SDIO Interface Full-speed Mode

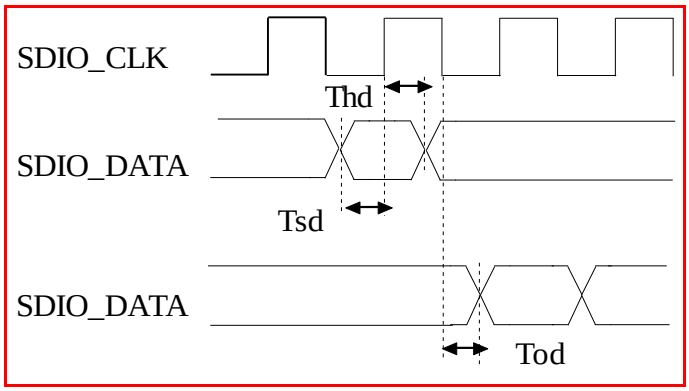


Figure 5: Interface Timings – SDIO Interface Full-speed Mode

4.4.1.2: High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SDIO_CLK	Tsdio	25	-	50	MHz
SDIO_DATA, input setup time	Tsd	5	-	-	ns

SDIO_DATA, input hold time	Thd	2	-	-	ns
SDIO_DATA, clock to output delay	Tod	5.5	-	12.5	ns

Table 5: AC Characteristics – SDIO Interface High-speed Mode

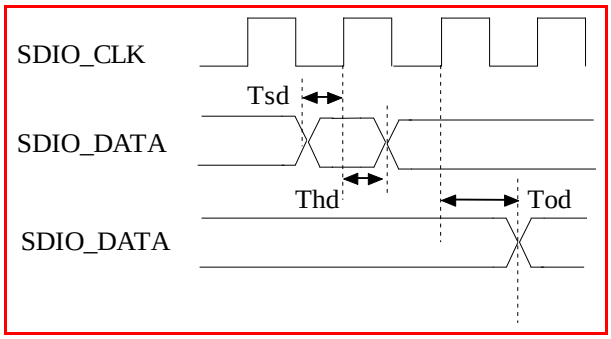


Figure 6: Interface Timings – SDIO Interface High-speed Mode

4.4.2: SPI Interface

The SPI Interface is a full duplex serial host interface, which supports 8-bit and 32-bit data granularity. It also supports gated mode of SPI clock and both the low and the high frequency modes. Incase of low frequency host, the data is driven on the falling edge and sampled on the rising edge and hence, it should be ensured that a valid data is present on the bus at the immediate rising edge after the SPI chip select is driven low. For high frequency transmission the data is driven as well as sampled on rising edge.

This interface has the interrupt pin along with the regular signals clock, chip select, data in and data out. Device interrupts the host processor regarding the packet pending event through this interrupt pin. This is an active high signal, and this will get cleared only after clearing the source of the interrupt, i.e. reading the pending packet from device. This will be generally connected to a GPIO pin of host platform and GPIO has to be configured for detecting interrupt on level high, and interrupt from this GPIO has to be mapped to driver ISR.

The SPI Slave supports mode 0 (SPI_POL=0, SPI_PHA=0) and mode 3 (SPI_POL=1, SPI_PHA=1).

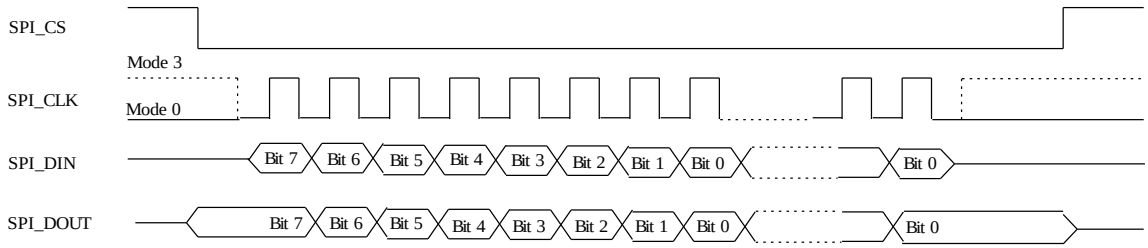


Figure 7: SPI Protocol

4.4.2.1: Full Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI_CLK	Tspi	0		25	MHz
SPI_CS to output delay	Tcs	3.5	-	7.5	ns
SPI CS to input setup time	Tcst	5.5	-	-	
SPI_DIN (MOSI), input setup time	Ts	1	-	-	ns
SPI_DIN (MOSI), input hold time	Th	1.5	-		ns
SPI_DOUT (MISO), clock to output delay	Tod	4	-	9	ns

Table 6: AC Characteristics – SPI Interface Full-speed Mode

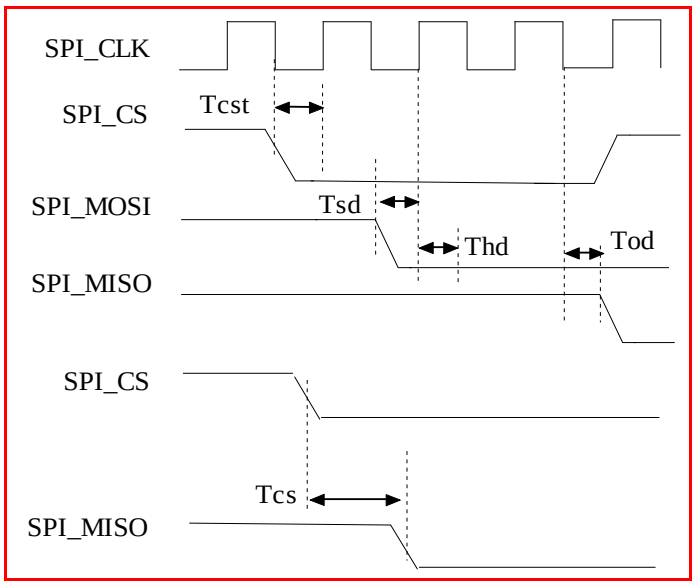


Figure 8: Interface Timings – SPI Interface Full-speed Mode

4.4.2.2: High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI_CLK	Tspi	25	-	75	MHz
SPI_CS to output delay	Tcs	3.5	-	7.5	ns
SPI CS to input setup time	Tcst	5.5	-	-	

Parameter	Symbol	Min.	Typ.	Max.	Units
SPI_MOSI, input setup time	Ts	1	-		ns
SPI_MOSI, input hold time	Th	1.5	-		ns
SPI_MISO, clock to output delay	Tod	4	-	9.5	ns

Table 7: AC Characteristics – SPI Interface High-speed Mode

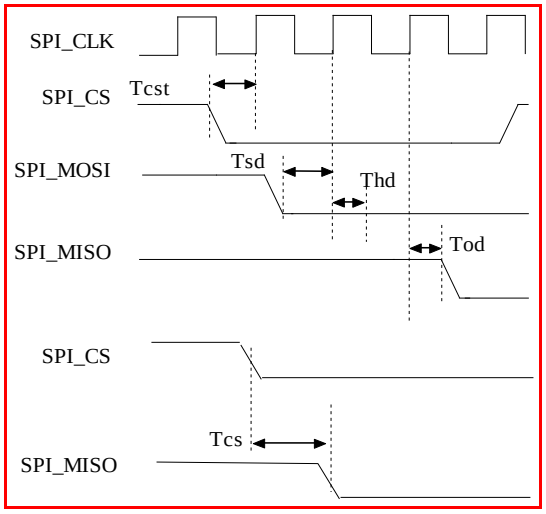


Figure 9: Interface Timings – SPI Interface High-speed Mode

4.4.3: JTAG Interface

Parameter	Symbol	Min.	Typ.	Max.	Units
TCK	Tjtag	0		5	MHz
TDI, setup time	Tstdi	5	-	-	Ns
TDI, hold time	Thtdi	5	-	-	Ns
TMS, setup time	Tstms	5	-	-	Ns
TMS, hold time	Thtms	5	-	-	Ns
TDO, clock to output valid	Totdo	0	-	14	Ns

Table 8: AC Characteristics – JTAG Interface

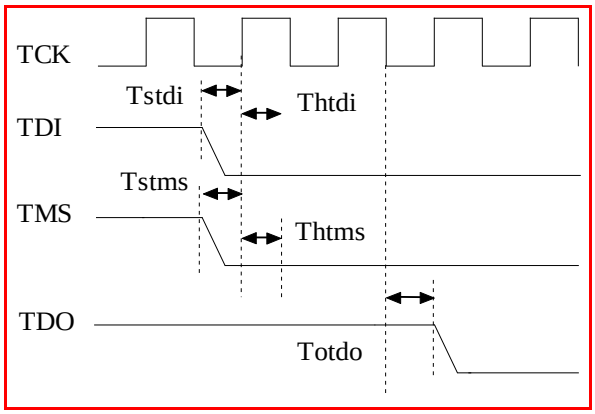


Figure 10: Interface Timings – JTAG Interface

5: Module Power Consumption

The following is the typical power consumption data for the RS9110-N-11-03 802.11a/b/g/n module. A single point 3.3V supply is used. Transmit power at antenna is 15dBm.

Mode	Conditions	Module Current
Standard Operational Modes – 2.4 GHz		
Data Transfer – Transmit TCP	1Mbps throughput	23 mA
Data Transfer – Transmit TCP	2Mbps throughput	41 mA
Data Transfer – Transmit TCP	22 Mbps throughput	226 mA
Data Transfer – Receive TCP	1Mbps throughput	26 mA
Data Transfer – Receive TCP	2Mbps throughput	57 mA
Data Transfer – Receive TCP	22 Mbps throughput	174 mA
Listen	Receive mode, with no active packet reception in progress	143 mA
Standby	Remaining connected to the Access Point, in Power-Save mode, with DTIM=3, beacon interval of 200 ms	1.5 mA
Sleep	Not connected to an AP; ready to connect upon driver command. The module can transition to any active mode in less than 2.5 ms.	0.8 mA
Standard Operational Modes – 5 GHz		
Data Transfer – Transmit TCP	1Mbps throughput	31 mA
Data Transfer – Transmit TCP	2Mbps throughput	51 mA
Data Transfer – Receive TCP	1Mbps throughput	23 mA
Data Transfer – Receive TCP	2Mbps throughput	41 mA
Data Transfer – Receive TCP	22 Mbps throughput	225 mA
Listen	Receive mode, with no active packet reception in progress	191 mA
Standby	Remaining connected to the Access Point, in Power-Save mode, with DTIM=3, beacon	1.2 mA

	interval of 200 ms	
Sleep	Not connected to an AP; ready to connect upon driver command. The module can transition to any active mode in less than 2.5 ms.	0.5 mA

Note:
1. The current numbers mentioned include the current drawn by the crystal oscillator.
2. Applications where wireless LAN module is inactive for extended periods of time an external power switch can be integrated. This may be used to obtain idle current of less than 5 uAmp which would be the leakage current of the power switch

6: Performance Specifications

6.1: Wireless Specifications

Note that the transmit power mentioned in the following table varies with data rate and also with the channel of operation for regulatory reasons.

Feature	Description
Frequency Band	2.400 – 2.500 GHz (Low band) 4.900 – 5.850 GHz (High Band)
Frequency Reference	40 MHz
Modulation	OFDM with BPSK, QPSK, 16-QAM, and 64-QAM 802.11b with CCK and DSSS
Supported Data Rates	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps 802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11b: 1, 2, 5.5, 11 Mbps
802.11n Features	MCS 0-7, STBC, RIFS, Greenfield Protection A-MPDU, A-MSDU Aggregation with Block-ack, PSMP, and MTBA
Typical Transmit Power (+/- 2 dBm) 'bg' Mode	17 dBm for 802.11b DSSS 17 dBm for 802.11b CCK 15 dBm for 802.11g/n OFDM
Typical Transmit Power (+/- 2 dBm) 'a' Mode	12 dBm

Table 9: Wireless Specification

6.2: Receive Characteristics

6.2.1: Sensitivity

Data Rate (bg Mode)	Typical Sensitivity (+/- 1.5 dBm)
1 Mbps	-94.0 dBm (< 8% PER)
2 Mbps	-89.0 dBm (< 8% PER)
11 Mbps	-86.0 dBm (< 8% PER)
6 Mbps	-89.0 dBm (<10% PER)
54 Mbps	-74.0 dBm (< 10% PER)
65 Mbps	-71.0 dBm (< 10% PER)
Data Rate (a Mode)	**Typical Sensitivity (+/- 1.5 dBm)**
6 Mbps	-88.0 dBm (<10% PER)
54 Mbps	-72.0 dBm (< 10% PER)

Data Rate (bg Mode)	Typical Sensitivity (+/- 1.5 dBm)
65 Mbps	-69.0 dBm (< 10% PER)

Table 10: Receive Sensitivity

6.3: Standards Compliance

RS9110-N-11-03 is compliant with the requirements of IEEE 802.11b, 802.11g, 802.11a, 802.11j, and 802.11n that include the following:

- Transmit Spectral Mask
- Transmit Center Frequency Leakage
- Transmit Center Frequency Tolerance
- Symbol Clock Frequency Tolerance
- Transmit Constellation error
- Receiver Adjacent Channel Interference Rejection
- Receiver Non-adjacent Channel Rejection
- Receiver Minimum Input Level
- Receiver Maximum Input Level

7: Software Details

The RS9110-N-11-03 provides a zero-host-load system architecture by implementing most of the 802.11 MAC functions in its internal multi-threaded ThreadArch™ processor. The driver consumes less than 5 MIPS from the host processor, thereby giving the freedom to the host processor to run its own applications.

7.1: Architecture

The following diagram depicts the software architecture of the solution.

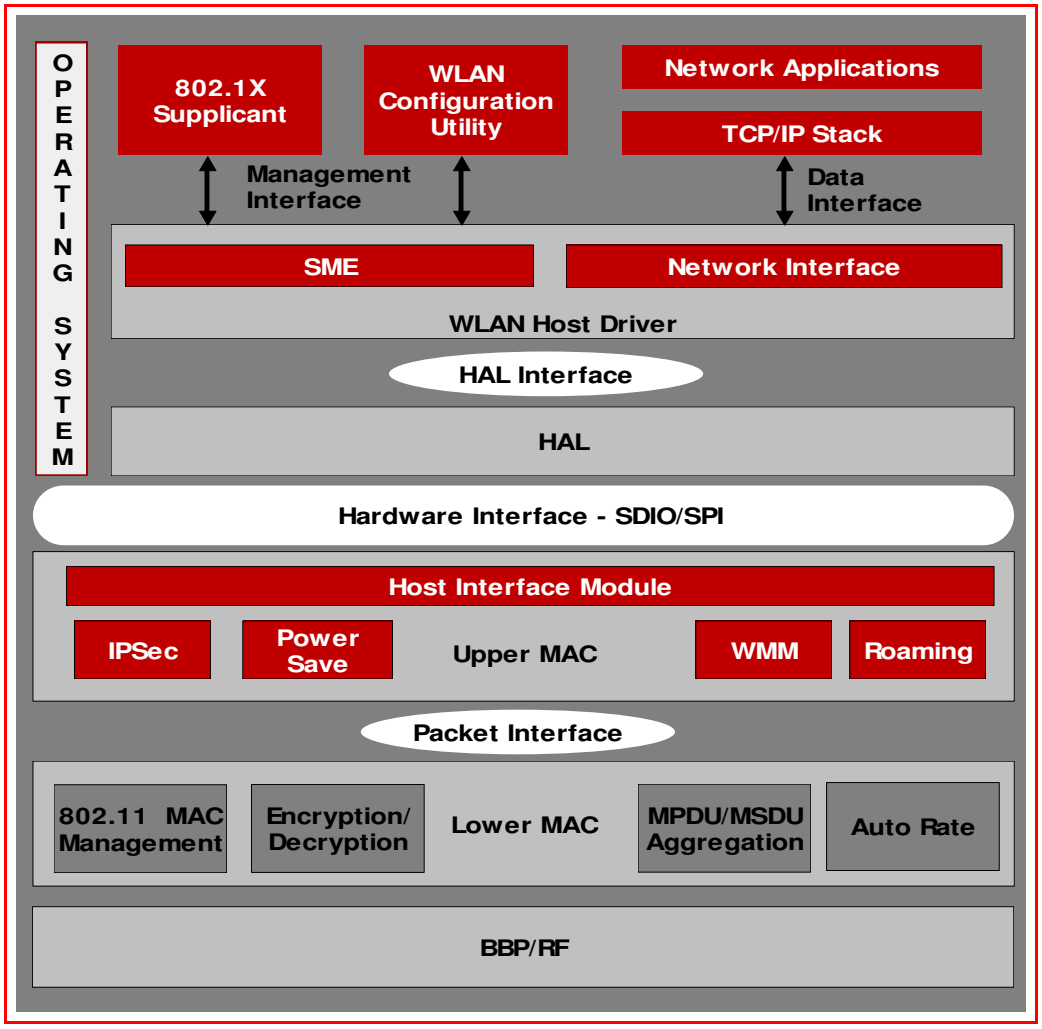


Figure 11: RS9110-N-11-03 Software Architecture

7.2: Details

This section provides an overview of the functionality of each of the key modules in the WLAN system.

7.2.1: 802.1x Supplicant

- WPA/WPA2-Personal mode functionality
- WPA/WPA2-EAP exchanges for entreprise mode
- Key negotiation and management – WEP, TKIP, and CCMP
- Pre-authentication and PMKSA caching for roaming

7.2.2: Configuration Utility

- It is a user-mode application to manage wireless network
- SSID selection
- Channel and rate selection
- Key management
- Configuration of 802.11 parameters

7.2.3: WLAN Driver

- Consumes < 5 MIPS from host processor
- Initialization module
- Baseband and RF programming
- Firmware downloading
- TCP/IP Network Interface Layer
- Transmission of TCP/IP packets
- Indicating received TCP/IP packets
- 802.11 Station Management Module
- Interaction with HAL layer – SDIO and SPI
- Power-save modes
  - Sleep
  - Standby

7.2.4: HAL- Hardware Abstraction Layer

- HAL layer changes depending on the host interface used
- SPI Interface – SPI host controller driver
- SDIO Interface – SDIO host controller and bus drivers

7.2.5: Upper MAC

- Non-time critical 802.11 MAC functions
- Classification of the packets
- Block-Acknowledgement negotiation
- Power save features
- Transfer of packets from host to LMAC and vice versa

- IPSec off-loading
- RNG – Random Number Generation

7.2.6: Lower MAC

- Time-critical 802.11 MAC functionality
- 802.11 frame formatting
- 802.3 frame to 802.11 conversion and vice-versa
- Beacon processing
- Backoff algorithm
- WEP 64 and 128 bit, WPA/WPA2 encryption and decryption
- Auto rate algorithm
- A-MPDU and A-MSDU aggregation
- Re-transmission
- Fragmentation and reassembly

7.3: OS Support

The Lite-Fi™ family devices including RS9110-N-11-03 support the device drivers and wireless configuration utilities for the following operating systems:

- Windows CE® 5.0 and 6.0
- Linux – 2.6.xx kernel
- Windows XP®
- Android 2.2

8: Ordering Information

8.1: Contact Information

For additional information, please contact Sales at Redpine Signals, Inc.

Redpine Signals, Inc.

2107 North First Street, Suite 680,

San Jose, CA 95131 USA

Phone: +1 408 748 3385

E-mail: sales@redpinesignals.com

Website: http://www.redpinesignals.com/

8.2: Device Ordering Information

The following table lists the part numbers to be used for ordering modules or evaluation boards (EVB). The 'xx' in the part numbers indicate a version number – 01, 02, etc., - identifying the version of the custom firmware that is included with the module or EVB. Redpine can create and provide customized firmware based on user requirements.

Device Number	Description	Packaging	Qualification
RS9110-N-11-03	Standard Part	Tray	Industrial
RS9110-N-11-03-EVB	Evaluation board for standard part	Board	

8.2.1: Device Packaging

- 60 RS9110-N-11-03 modules per tray
- Each tray has 12 rows and 5 columns
- Tray dimensions 14cm x 32.5cm x 0.8cm (L X W X H)
- The device packaging is MSL-3 compliant

8.3: Collateral

The following documentation and software are available along with the RS9110-N-11-03 module.

- Module Evaluation Board (EVB) with SDIO host interface
- Device driver and configuration software for Windows XP, Windows CE, or Linux[3]
- Test mode software

[3] Please contact Redpine for details of operating systems and processor platforms supported, and for software porting and customization services

- EVB User Guide
- Software Installation Guide
- Wi-Fi Evaluation Procedure Manual
- Module Integration Guide

Document History:

Rev.	Ver. No.	Date	Changes
1.	1.0	November 2008	Adapted from -02 module datasheet
2.	1.1	January 2009	Updated with new pinout, reflow profile, etc.
3.	1.11	January 2009	Removed power numbers section as a temporary release
4.	1.12	February 2009	Added module height. Note: power numbers are not added in yet
5.	1.13	February 2009	Modified module height. Modified operating temperature range.
6.	1.14	February 2009	Added missing table headings
7.	1.15	March 2009	Added new logo
8.	1.16	June 2009	Modified the supported Reference frequencies.
9.	1.17	Aug 2009	Modified descriptions of SLEEP_CLK_IN, and XTAL_IP_EN
10.	1.18	Sep 2009	Minimum voltage changed to 3.1V. Allusion to Vout corrected. *Pending: Frequency reference list*
11.	1.19	Sep 2009	Changed XTAL_IP_EN to XTAL_EN_IP
12.	1.2	Oct 2009	Added RoHS
13.	1.21	November 2009	Removed "draft 2.0" from 11n
14.	1.22	Jan 2010	Removed DRM and Module Test Reports from 'Collateral' section
15.	1.23	Feb 2010	Changed PIN out for SHUTDOWN pin. Modified HOST_WAKEUP_INT, SLEEP_CLK_IN description.
16.	1.24	March 2010	Module height is changed and a note regarding Tx power is added
17.	1.25	July 2010	Added module power consumption section Remove reference clock frequencies Added SPI mode description
18.	1.26	November 2010	Updated with comments from Venkatesh, Subba, Suresh. The comments are same as from RS9110-N-11-02 datasheet.

19.	1.27	December 2010	Updated with comments carried over from RS9110-N-11-02 datasheet.
20.	1.28	January 2011	Updated with the PCB layout diagram.
21.	1.28.1	February 2011	Modified date and sleep_clk_xxx pin description
22.	1.29	July 2011	Added humidity information and OS support for Android
23.	1.31	Sep, 2012	Removed reel from packaging

*****