



Product List

SM8954AL25, 25MHz 16KB internal flash MCU
SM8954AC25, 25MHz 16KB internal flash MCU
SM8954AC40, 40MHz 16KB internal flash MCU

Description

The SM8954A series product is an 8 - bit single chip micro controller with 16KB on-chip flash and 1K byte RAM embedded. It is a derivative of the 8052 micro controller family. It has 5-channel SPWM build-in. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 16 I/O pins for PDIP package or up to 36 I/O pins for PLCC/PQFP/LQFP package, or applications which need up to 16K byte flash memory for program data. To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method.

Ordering Information

yymm
SM8954AihhKL

yy: year, mm: month
v: version identifier{ , A, B,...}
i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
L:PB Free identifier
{No text is Non-PB Free , "P" is PB Free}

Features

- Working Voltage: 3.0V ~ 3.6V For L Version.
4.5V ~ 5.5V For C Version.
- General 8052 family compatible
- 12 clocks per machine cycle
- 16K byte on chip program flash
- 1024 byte on-chip data RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- 5 channel SPWM function with P1.3 ~ P1.7

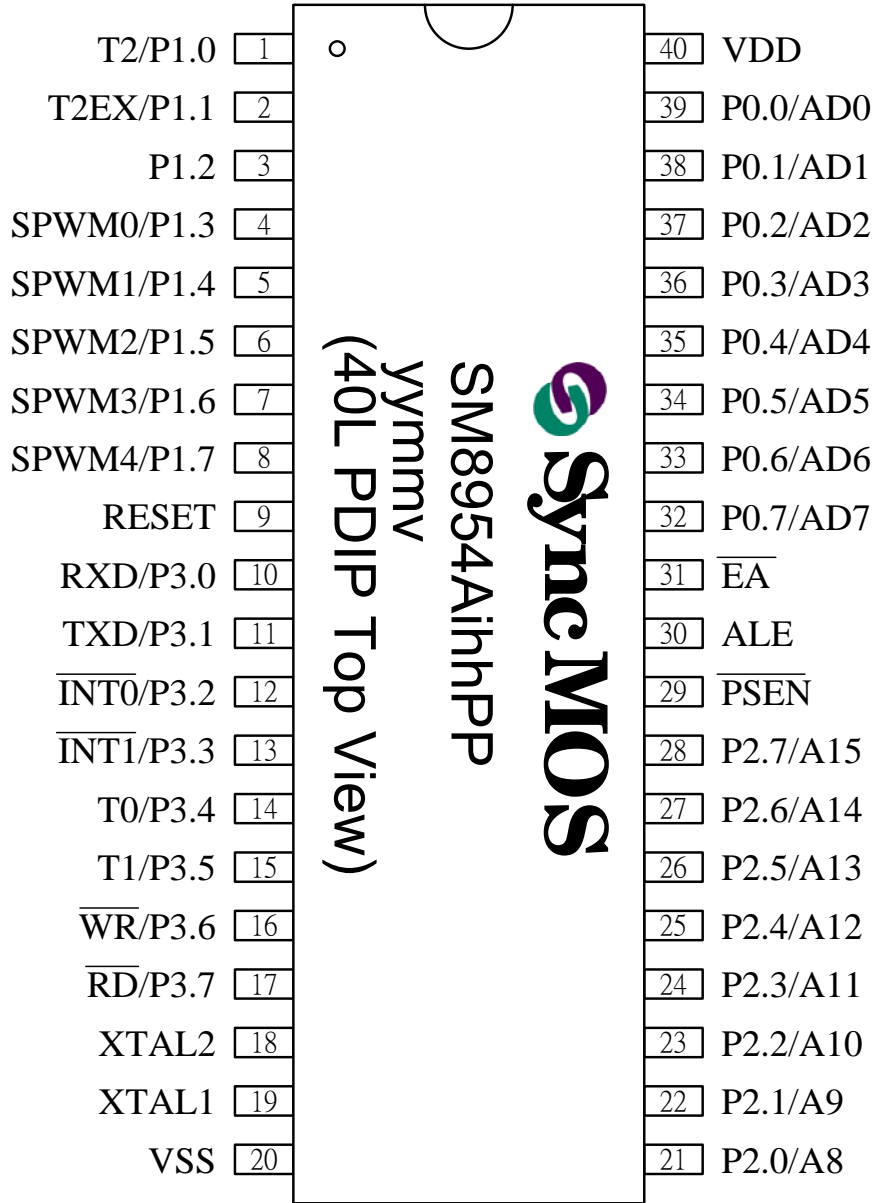
Taiwan
6F, No.10-2 Li- Hsin 1st Road ,
Science-based Industrial Park,
Hsinchu, Taiwan 30078

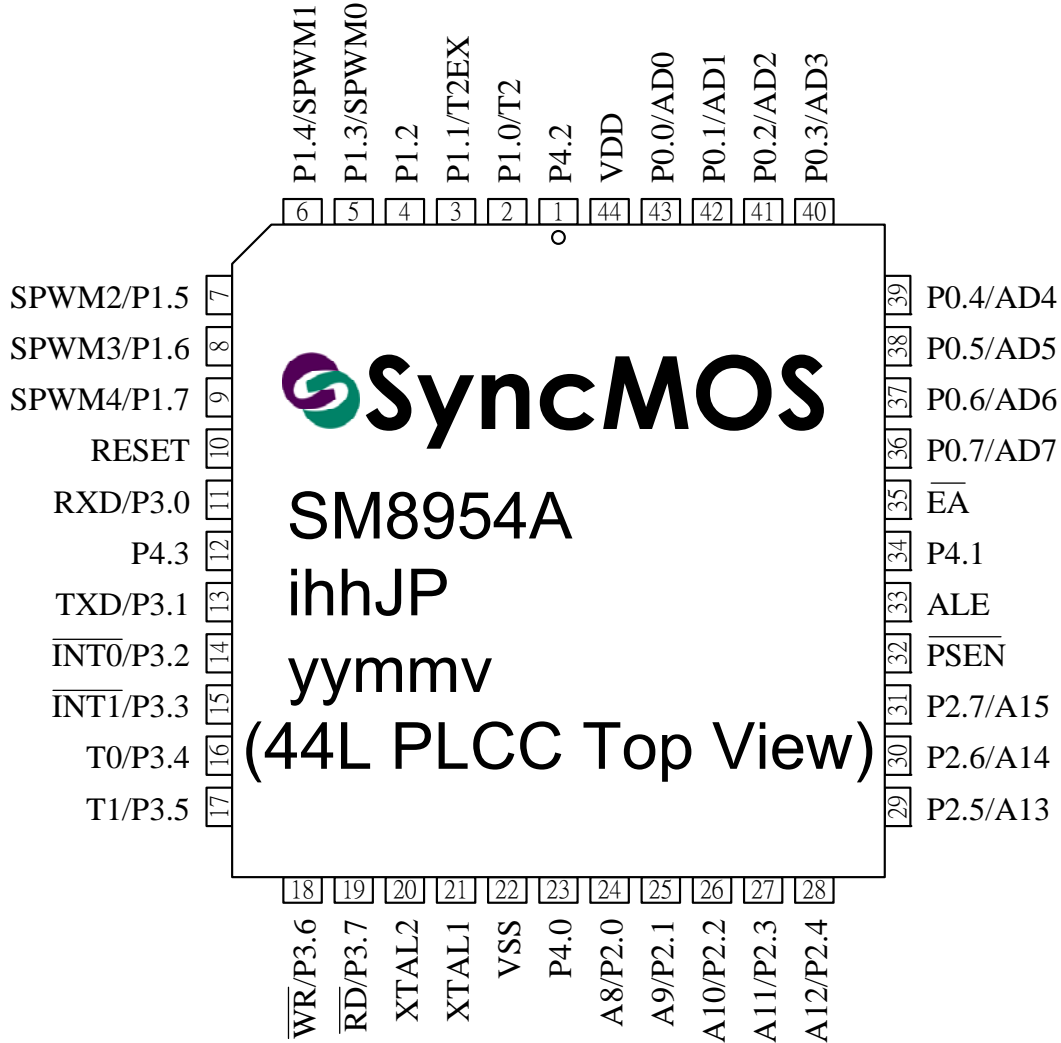
TEL: 886-3-567-1820
886-3-567-1880
FAX: 886-3-567-1891
886-3-567-1894

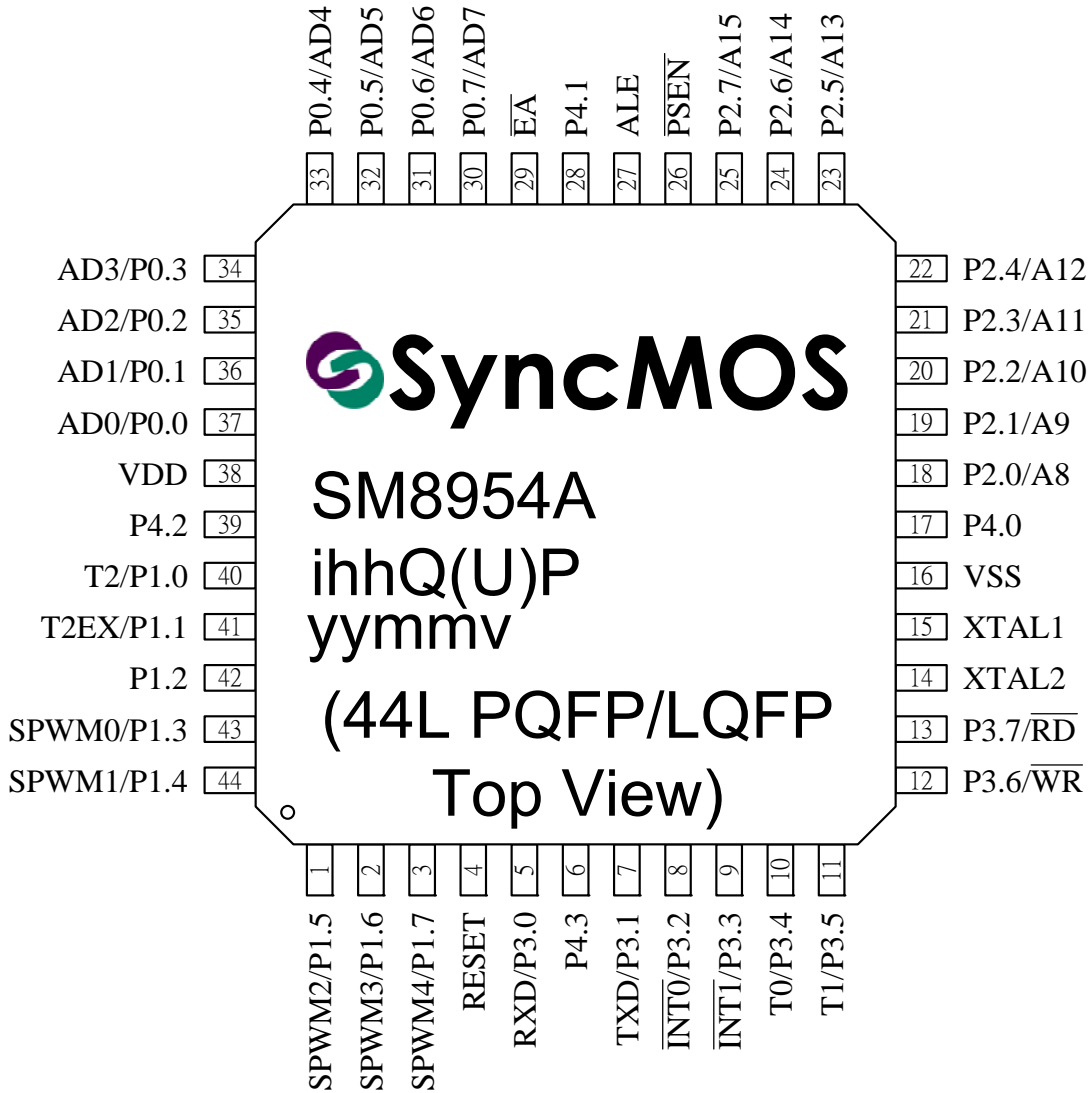
| Postfix | Package | Pin / Pad Configuration |
|---------|----------|-------------------------|
| P | 40L PDIP | Page 2 |
| J | 44L PLCC | Page 3 |
| Q | 44L PQFP | Page 4 |
| U | 44L LQFP | Page 4 |



Pin Configuration

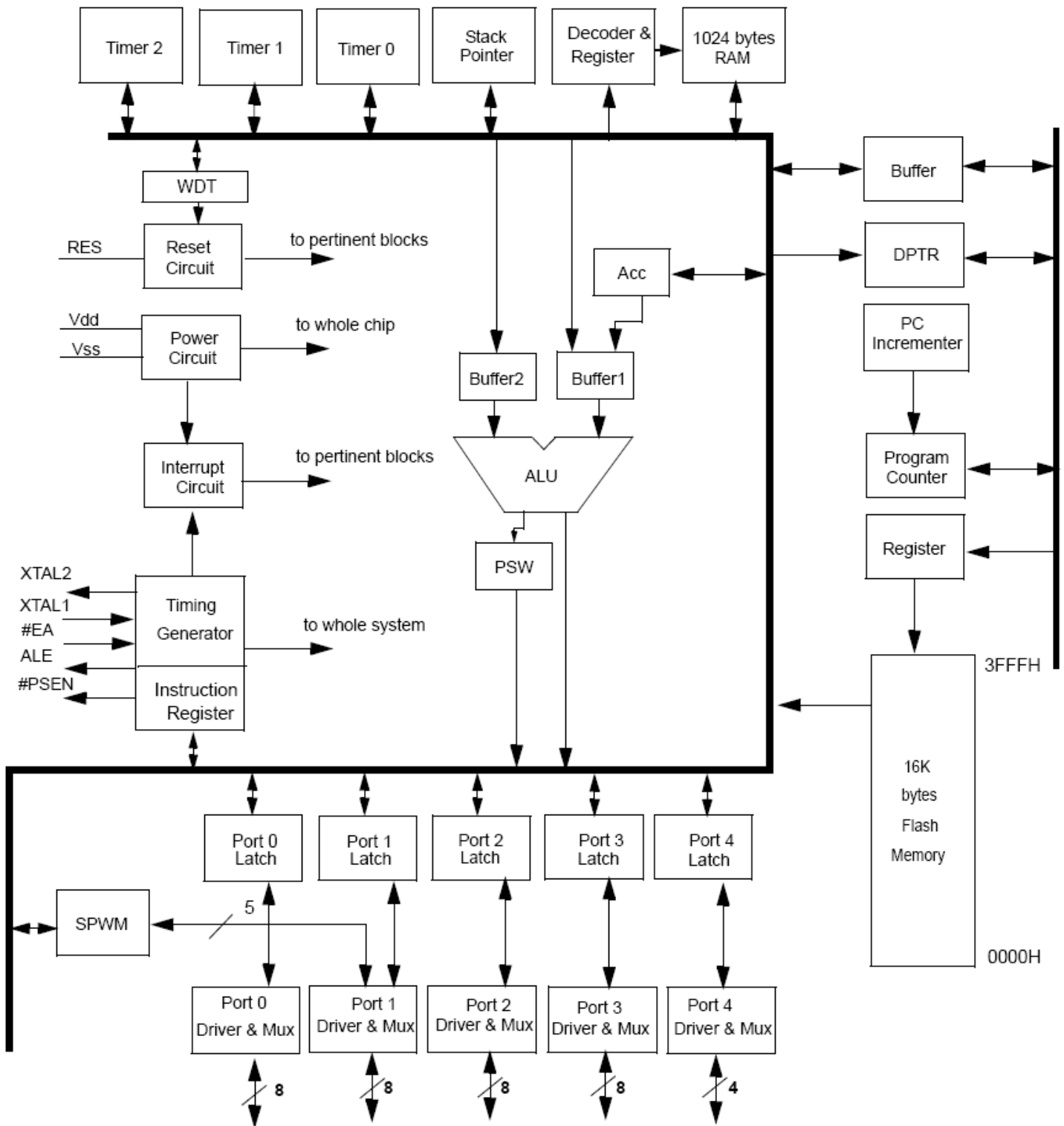








Block Diagram



Specifications subject to change without notice contact your sales representatives for the most recent information.



Pin Description

| 40L PDIP Pin# | 44L PQFP/LQFP Pin# | 44L PLCC Pin# | Symbol | Active | I/O | Names |
|---------------|--------------------|---------------|------------|--------|-----|---|
| 1 | 40 | 2 | P1.0/T2 | | i/o | bit 0 of port 1 & timer 2 clock out |
| 2 | 41 | 3 | P1.1/T2EX | | i/o | bit 1 of port 1 & timer 2 control |
| 3 | 42 | 4 | P1.2 | | i/o | bit 2 of port 1 |
| 4 | 43 | 5 | P1.3/SPWM0 | | i/o | bit 3 of port 1 & SPWM channel 0 |
| 5 | 44 | 6 | P1.4/SPWM1 | | i/o | bit 4 of port 1 & SPWM channel 1 |
| 6 | 1 | 7 | P1.5/SPWM2 | | i/o | bit 5 of port 1 & SPWM channel 2 |
| 7 | 2 | 8 | P1.6/SPWM3 | | i/o | bit 6 of port 1 & SPWM channel 3 |
| 8 | 3 | 9 | P1.7/SPWM4 | | i/o | bit 7 of port 1 & SPWM channel 4 |
| 9 | 4 | 10 | RES | H | i | Reset |
| 10 | 5 | 11 | P3.0/RXD | | i/o | bit 0 of port 3 & Receiver data |
| 11 | 7 | 13 | P3.1/TXD | | i/o | bit 1 of port 3 & Transmit data |
| 12 | 8 | 14 | P3.2/#INT0 | L/- | i/o | bit 2 of port 3 & low true interrupt 0 |
| 13 | 9 | 15 | P3.3/#INT1 | L/- | i/o | bit 3 of port 3 & low true interrupt 1 |
| 14 | 10 | 16 | P3.4/T0 | | i/o | bit 4 of port 3 & Timer 0 |
| 15 | 11 | 17 | P3.5/T1 | | i/o | bit 5 of port 3 & Timer 1 |
| 16 | 12 | 18 | P3.6/#WR | | i/o | bit 6 of port 3 & ext. memory write |
| 17 | 13 | 19 | P3.7/#RD | | i/o | bit 7 of port 3 & ext. memory Read |
| 18 | 14 | 20 | XTAL2 | | o | Crystal out |
| 19 | 15 | 21 | XTAL1 | | i | Crystal in |
| 20 | 16 | 22 | VSS | | | Sink Voltage, Ground |
| 21 | 18 | 24 | P2.0/A8 | | i/o | bit 0 of port 2 & bit 8 of ext. memory address |
| 22 | 19 | 25 | P2.1/A9 | | i/o | bit 1 of port 2 & bit 9 of ext. memory address |
| 23 | 20 | 26 | P2.2/A10 | | i/o | bit 2 of port 2 & bit 10 of ext. memory address |
| 24 | 21 | 27 | P2.3/A11 | | i/o | bit 3 of port 2 & bit 11 of ext. memory address |
| 25 | 22 | 28 | P2.4/A12 | | i/o | bit 4 of port 2 & bit 12 of ext. memory address |
| 26 | 23 | 29 | P2.5/A13 | | i/o | bit 5 of port 2 & bit 13 of ext. memory address |
| 27 | 24 | 30 | P2.6/A14 | | i/o | bit 6 of port 2 & bit 14 of ext. memory address |
| 28 | 25 | 31 | P2.7/A15 | | i/o | bit 7 of port 2 & bit 15 of ext. memory address |
| 29 | 26 | 32 | #PSEN | | o | program storage enable |
| 30 | 27 | 33 | ALE | | o | address latch enable |
| 31 | 29 | 35 | #EA | L | I | External access |
| 32 | 30 | 36 | P0.7/AD7 | | i/o | bit 7 of port 0 & data/address bit 7 of ext. memory |
| 33 | 31 | 37 | P0.6/AD6 | | i/o | bit 6 of port 0 & data/address bit 6 of ext. memory |
| 34 | 32 | 38 | P0.5/AD5 | | i/o | bit 5 of port 0 & data/address bit 5 of ext. memory |
| 35 | 33 | 39 | P0.4/AD4 | | i/o | bit 4 of port 0 & data/address bit 4 of ext. memory |
| 36 | 34 | 40 | P0.3/AD3 | | i/o | bit 3 of port 0 & data/address bit 3 of ext. memory |
| 37 | 35 | 41 | P0.2/AD2 | | i/o | bit 2 of port 0 & data/address bit 2 of ext. memory |
| 38 | 36 | 42 | P0.1/AD1 | | i/o | bit 1 of port 0 & data/address bit 1 of ext. memory |
| 39 | 37 | 43 | P0.0/AD0 | | i/o | bit 0 of port 0 & data/address bit 0 of ext. memory |
| 40 | 38 | 44 | VDD | | | Drive Voltage, +5 Vcc |
| | 17 | 23 | P4.0 | | i/o | bit 0 of Port 4 |
| | 28 | 34 | P4.1 | | i/o | bit 1 of Port 4 |
| | 39 | 1 | P4.2 | | i/o | bit 2 of Port 4 |
| | 6 | 12 | P4.3 | | i/o | bit 3 of port 4 |

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Special Function Register (SFR)

The address \$80 to \$FF can be accessed by direct addressing mode only.

Address \$80 to \$FF is SFR area.

The following table lists the SFRs which are identical to general 8052, as well as SM8954A Extension SFRs.

Special Function Register (SFR) Memory Map

| | | | | | | | | | | |
|------|-----------|-------|--------|--------------|---------------|---------------|---------------|---------------|---------------|------|
| \$F8 | | | | | | | | | | \$FF |
| \$F0 | B | | | | | | | | | \$F7 |
| \$E8 | | | | | | | | | | \$EF |
| \$E0 | ACC | | | | | | | | | \$E7 |
| \$D8 | P4 | | | | | | | | | \$DF |
| \$D0 | PSW | | | | | | | | | \$D7 |
| \$C8 | T2CON | T2MOD | RCAP2L | RCAP2H | TL2 | TH2 | | | | \$CF |
| \$C0 | | | | | | | | | | \$C7 |
| \$B8 | IP | | | | | | | | SCONF | \$BF |
| \$B0 | P3 | | | | | | | | | \$B7 |
| \$A8 | IE | | | | SPWMD4 | | | | | \$AF |
| \$A0 | P2 | | | SPWMC | SPWMD0 | SPWMD1 | SPWMD2 | SPWMD3 | | \$A7 |
| \$98 | SCON | SBUF | | P1CON | | | | | WDTC | \$9F |
| \$90 | P1 | | | | | | | | WDTKEY | \$97 |
| \$88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | | | | \$8F |
| \$80 | P0 | SP | DPL | DPH | | RCON | | | PCON | \$87 |

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM8954A

| Addr | SFR | Reset | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------------|-----------|---------|---------|---------|---------|---------|---------|---------|---------|
| 85H | RCON | 00H | | | | | | | RAMS1 | RAMS0 |
| 97H | WDTKEY | 00H | WDTKEY7 | WDTKEY6 | WDTKEY5 | WDTKEY4 | WDTKEY3 | WDTKEY2 | WDTKEY1 | WDTKEY0 |
| 9BH | P1CON | 00000*** | SPWME4 | SPWME3 | SPWME2 | SPWME1 | SPWME0 | | | |
| 9FH | WDTC | 0*0***000 | WDTE | | CLEAR | | | PS2 | PS1 | PS0 |
| A3H | SPWMC | *****00 | | | | | | | SPFS1 | SPFS0 |
| A4H | SPWMD0 | 00H | SPWMD04 | SPWMD03 | SPWMD02 | SPWMD01 | SPWMD00 | BRM02 | BRM01 | BRM00 |
| A5H | SPWMD1 | 00H | SPWMD14 | SPWMD13 | SPWMD12 | SPWMD11 | SPWMD10 | BRM12 | BRM11 | BRM10 |
| A6H | SPWMD2 | 00H | SPWMD24 | SPWMD23 | SPWMD22 | SPWMD21 | SPWMD20 | BRM22 | BRM21 | BRM20 |
| A7H | SPWMD3 | 00H | SPWMD34 | SPWMD33 | SPWMD32 | SPWMD31 | SPWMD30 | BRM32 | BRM31 | BRM30 |
| ACH | SPWMD4 | 00H | SPWMD44 | SPWMD43 | SPWMD42 | SPWMD41 | SPWMD40 | BRM42 | BRM41 | BRM40 |
| BFH | SCONF | 0*****00 | WDR | | | | | | OME | ALEI |
| C8H | T2CON | 00H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2 | CP/RL2 |
| C9H | T2MOD | *****00 | | | | | | | T2OE | DCEN |
| D8H | P4 | ****1111 | | | | | P4.3 | P4.2 | P4.1 | P4.0 |

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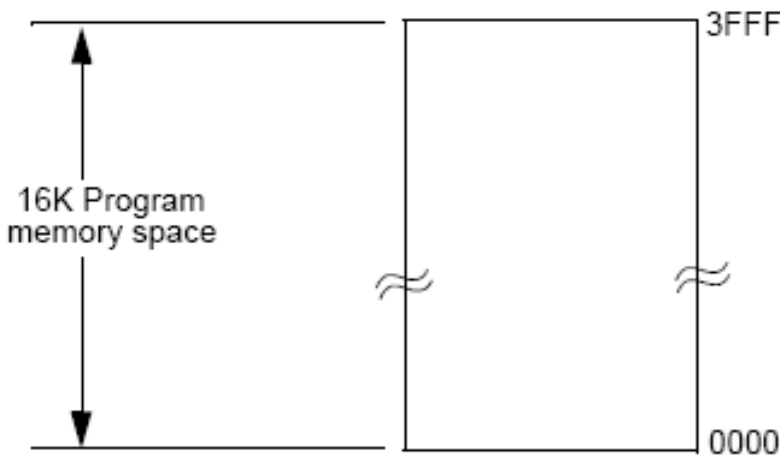
Extension Function Description

1. Memory Structure

The SM8954A is the general 8052 hardware core as a single chip micro controller. Its memory structure follows general 8052 structure.

1.1 Program Memory

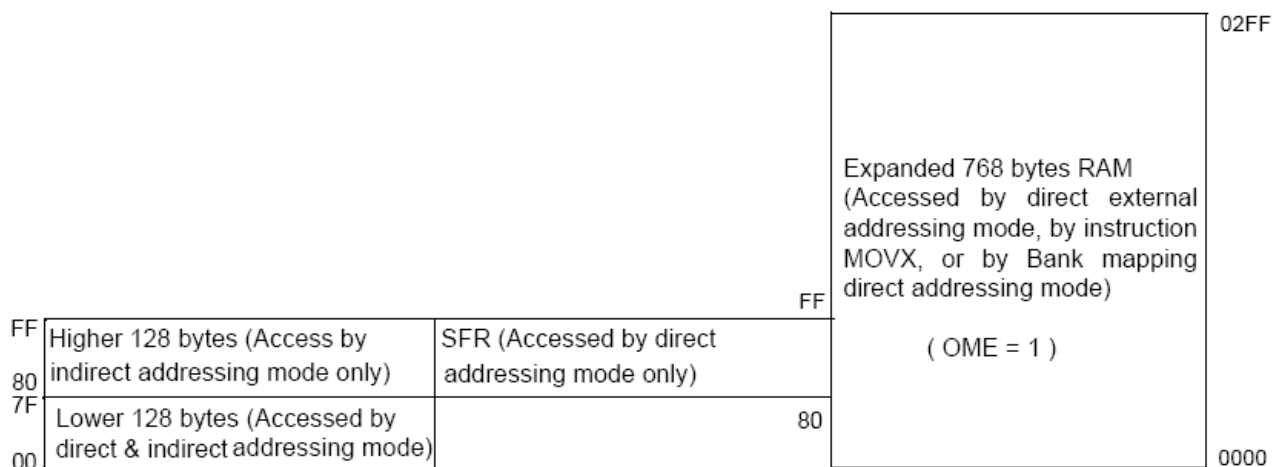
The SM8954A has 16K byte on-chip flash memory which used as general program memory. The address range for the 16K byte is \$0000 to \$3FFF.



Note: The single flash block address structure for doing as well as program ROM flash.

1.2 Data Memory

The SM8954A has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX),



On-chip expanded RAM address structure.



1.2.1 Data Memory - Lower 128 byte (\$00 to \$7F)

Data Memory \$00 to \$FF is the same as 8052.
The address \$00 to \$7F can be accessed by direct and indirect addressing modes.
Address \$00 to \$1F is register area.
Address \$20 to \$2F is memory bit area.
Address \$30 to \$7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte (\$80 to \$FF)

The address \$80 to \$FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.
Address \$80 to \$FF is data area.

1.2.3 Data Memory - Expanded 768bytes (\$0000 to \$02FF)

From external address \$0000 to \$02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX):

Internal RAM Control Register (RCON, \$85)

| | bit-7 | | | | | | bit-0 | |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|
| | Unused | Unused | Unused | Unused | Unused | Unused | RAMS1 | RAMS0 |
| Read / Write: | - | - | - | - | - | - | R/W | R/W |
| Reset value: | * | * | * | * | * | * | 0 | 0 |

SM8954A has 768 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 1 and bit 0 (RAMS1, RAMS0) of RCON. The default setting of RAMS1, RAMS0 bits is 00 (page0).

| RAMS1 | RAMS0 | MOVX @Ri i=0,1 mapping to expended RAM address |
|-------|-------|--|
| 0 | 0 | \$0000 ~ \$00FF |
| 0 | 1 | \$0100 ~ \$01FF |
| 1 | 0 | \$0200 ~ \$02FF |

The port 0, port2, port3.6 and port3.7 can be used as general purpose I/O pin while port0 is open-drain structure.

System Control Register (SCONF, \$BF)

| | bit-7 | | | | | | bit-0 | |
|---------------|-------|--------|--------|--------|--------|--------|-------|------|
| | WDR | Unused | Unused | Unused | Unused | Unused | OME | ALEI |
| Read / Write: | R/W | - | - | - | - | - | R/W | R/W |
| Reset value: | 0 | * | * | * | * | * | 0 | 0 |

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow. WDR will be set to 1, The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

OME : 768 bytes on-chip RAM enable bit. The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768 byte RAM. The default setting of OME bit is 0 (disable).

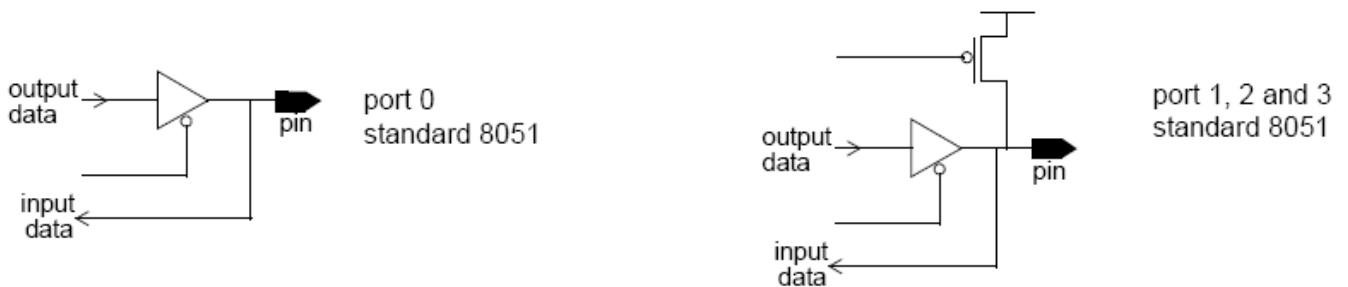


ALEI : ALE output inhibit bit, to reduce EMI. Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

1.3 I/O Pin Configuration

The ports 1, 2 and 3 of standard 8051 have internal pull-up resistor, and port 0 has open-drain outputs. Each I/O pin can be used independently as an input or an output. For I/O ports to be used as an input pin, the port bit latch must contain a '1' which turns off the output driver FET. Then for port 1, 2 and 3 port pin is pulled high by a weak internal pull-up, and can be pulled low by an external source. The port 0 has open-drain outputs which means its pull-ups are not active during normal port operation. Writing '1' to the port 0 bit latch will causing bit floating so that it can be used as a high-impedance input.

The port 4 used as GPIO will has the same function as port 1, 2 and 3.



2. Port 4 for PLCC or QFP package :

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, \$D8)

| | bit-7 | | | | bit-0 | | | |
|---------------|--------|--------|--------|--------|-------|------|------|------|
| | Unused | Unused | Unused | Unused | P4.3 | P4.2 | P4.1 | P4.0 |
| Read / Write: | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset value: | * | * | * | * | 1 | 1 | 1 | 1 |

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.



3. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever un-predicted reset happened

The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway.

There is a 250KHz RC oscillator embedded in chip. Set WDTE = "1" will enable the RC oscillator and the frequency is independent to the system frequency.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM8958A been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

3.1 Watch Dog Timer Registers:

Watch Dog Timer Registers - WDT Control Register (WDTC, \$9F)

| | | | | | | | | |
|---------------|-------|---|-------|--------|--------|-----|-----|-------|
| | bit-7 | | | | | | | bit-0 |
| | WDTE | R | Clear | Unused | Unused | PS2 | PS1 | PS0 |
| Read / Write: | R/W | - | R/W | - | - | R/W | R/W | R/W |
| Reset value: | 0 | * | 0 | * | * | 0 | 0 | 0 |

WDTE : Watch Dog Timer enable bit

CLEAR : Watch Dog Timer reset bit

PS[2:0] : Overflow period select bits

| PS [2:0] | Overflow Period (ms) |
|----------|----------------------|
| 000 | 16.384 |
| 001 | 32.768 |
| 010 | 65.536 |
| 011 | 131.072 |
| 100 | 262.144 |
| 101 | 524.288 |
| 110 | 1048.576 |
| 111 | 2097.152 |



Watch Dog Key Register - (WDTKEY, \$97H)

| | bit-7 | | | | | | bit-0 | |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| | WDT KEY7 | WDT KEY6 | WDT KEY5 | WDT KEY4 | WDT KEY3 | WDT KEY2 | WDT KEY1 | WDT KEY0 |
| Read / Write: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

By default, the WDTC is read only. User need to write values 1EH, E1H sequentially to the WDTKEY(\$97H) register to enable the WDTC write attribute, That is

```
MOV WDTKEY, # 1EH
MOV WDTKEY, # 0E1H
```

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY(\$97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # 0E1H
MOV WDTKEY, # 1EH
```

Watch Dog Timer Register - System Control Register (SCONF, \$BF)

| | bit-7 | | | | | bit-0 | |
|---------------|-------|--------|--------|--------|--------|-------|------|
| | WDR | Unused | Unused | Unused | Unused | OME | ALEI |
| Read / Write: | R/W | - | - | - | - | R/W | R/W |
| Reset value: | 0 | * | * | * | * | 0 | 0 |

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened

4. Reduce EMI Function

The SM8954A allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.



5. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module contain 1 kind of PWM sub module: SPWM (Specific PWM). SPWM has five 8-bit channels.

5.1 SPWM Function Description:

The 8-bit SPWM channel is composed of an 8-bit register which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The SPFS[1:0] settings of SPWMC (\$A3) register are dividend of Fosc to be SPWM clock, $F_{osc}/2^{(SPFS[1:0]+1)}$. The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is $[F_{osc}/2^{(SPFS[1:0]+1)}/32$.

5.2 SPWM Registers - P1CON, SPWMC, SPWMD[4:0]

SPWM Registers - Port1 Configuration Register (P1CON, \$9B)

| | bit-7 | | | | | bit-0 | | |
|---------------|--------|--------|--------|--------|--------|--------|--------|--------|
| | SPWME4 | SPWME3 | SPWME2 | SPWME1 | SPWME0 | Unused | Unused | Unused |
| Read / Write: | R/W | R/W | R/W | R/W | R/W | - | - | - |
| Reset value: | 0 | 0 | 0 | 0 | 0 | * | * | * |

SPWME[4:0] : When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Five bits are cleared upon reset.

SPWM Registers -SPWM Control Register (SPWMC, \$A3)

| | bit-7 | | | | | | bit-0 | |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|
| | Unused | Unused | Unused | Unused | Unused | Unused | SPFS1 | SPFS0 |
| Read / Write: | - | - | - | - | - | - | R/W | R/W |
| Reset value: | * | * | * | * | * | * | 0 | 0 |

SPFS[1:0] : These two bits is 2's power parameter to form a frequency divider for input clock.

| SPFS1 | SPFS0 | Divider | SPWM clock, Fosc=20MHz | SPWM clock, Fosc=24MHz |
|-------|-------|---------|------------------------|------------------------|
| 0 | 0 | 2 | 10MHz | 12MHz |
| 0 | 1 | 4 | 5MHz | 6MHz |
| 1 | 0 | 8 | 2.5MHz | 3MHz |
| 1 | 1 | 16 | 1.25MHz | 1.5MHz |



SPWM Registers -SPWM Data Register (SPWMD[4:0], \$AC, \$A7 ~\$A4)

| | | | | | | | | |
|---------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------------|---------------|---------------|
| | bit-7 | | | | bit-0 | | | |
| | SPWMD [4:0]4 | SPWMD [4:0]3 | SPWMD [4:0]2 | SPWMD [4:0]1 | SPWMD [4:0]0 | BRM [2:0]2 | BRM [2:0]1 | BRM [2:0]0 |
| Read / Write: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

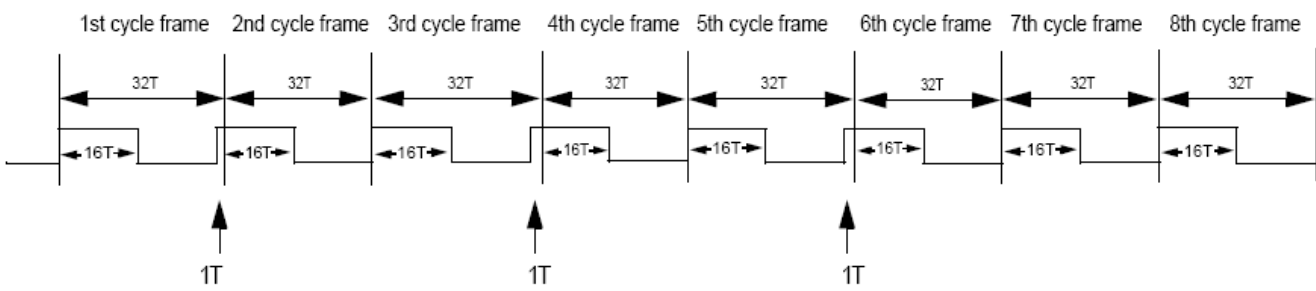
SPWMD[4:0] : content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[2:0] : will insert certain narrow pulses among an 8-SPWM-cycle frame

| N = BRM[2:0] | Number of SPWM cycles inserted in an 8-cycle frame |
|--------------|--|
| 000 | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | 7 |

Example of SPWM timing diagram:

```
MOV SPWMC , #03H ; Set output frequency (Divider = 16)
MOV SPWMD0 , #83H ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM[2:0] = 3
MOV P1CON , #08H ; Enable P1.3 as SPWM output pin
```



(narrow pulse inserted by BRM0[2:0] setting, here BRM0[2:0]=3)

$$\text{SPWM clock} = 1 / T = F_{osc} / 2^{(SPFS[1:0]+1)}$$

$$\text{The SPWM output cycle frame frequency} = \text{SPWM clock} / 32 = [F_{osc}/2^{(SPFS[1:0]+1)}]/32$$

If user use $F_{osc}=20\text{MHz}$, $SPFS[1:0]$ of $SPWMC=\#03H$, then
 $\text{SPWM clock} = 20\text{MHz}/2^4 = 20\text{MHz}/16 = 1.25\text{MHz}$
 $\text{SPWM output cycle frame frequency} = (20\text{MHz}/2^4)/32=39.1\text{KHz}$



Operating Conditions

| Symbol | Description | Min. | Typ. | Max. | Unit. | Remarks |
|---------|-----------------------|------|------|------|-------|--------------------------------|
| TA | Operating temperature | -40 | 25 | 85 | °C | Ambient temperature under bias |
| VCC5 | Supply voltage | 4.5 | 5.0 | 5.5 | V | For C Version |
| VCC3 | Supply voltage | 3 | 3.3 | 3.6 | V | For L Version |
| Fosc 25 | Oscillator Frequency | 3.0 | 25 | 25 | MHz | For 5V, 3.3V application |
| Fosc 40 | Oscillator Frequency | 3.0 | 40 | 40 | MHz | For 5V application |

DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 3.0V to 5.5V)

| Symbol | Parameter | Valid | Min. | Max. | Unit | Test Conditions |
|--------|----------------------------|------------------------|--------|---------|------|---------------------------------|
| VIL1 | Input Low Voltage | port 0,1,2,3,4,#EA | -0.5 | 0.8 | V | |
| VIL2 | Input Low Voltage | RES, XTAL1 | 0 | 0.8 | V | |
| VIH1 | Input High Voltage | port 0,1,2,3,4,#EA | 2.0 | Vcc+0.5 | V | |
| VIH2 | Input High Voltage | RES, XTAL1 | 70%Vcc | Vcc+0.5 | V | |
| VOL1 | Output Low Voltage | port 0, ALE, #PSEN | | 0.45 | V | IOL=8mA (5V) / IOL=6mA (3.3V) |
| VOL2 | Output Low Voltage | port 1,2,3,4 | | 0.45 | V | IOL=6.5mA (5V) / IOL=5mA (3.3V) |
| VOH1 | Output High Voltage | port 0 | 2.4 | | V | IOH=-800uA (only for VCC =5V) |
| | | | 90%Vcc | | V | IOH=-80uA |
| VOH2 | Output High Voltage | port 1,2,3,4,ALE,#PSEN | 2.4 | | V | IOH=-60uA (only for VCC =5 V) |
| | | | 90%Vcc | | V | IOH=-10uA |
| IIL | Logical 0 Input Current | port 1,2,3,4 | | -75 | uA | Vin=0.45V |
| ITL | Logical Transition Current | port 1,2,3,4 | | -650 | uA | Vin=2.0V |
| ILI | Input Leakage Current | port 0, #EA | | ±10 | uA | 0.45V<Vin<Vcc |
| R RES | Reset Pull-down Resistance | RES | 50 | 300 | Kohm | |
| C IO | Pin Capacitance | | | 10 | pF | Freq=1MHz, Ta=25 °C |
| I CC | Power Supply Current | Vdd | | 20 | mA | Active mode, 16MHz |
| | | | | 6.5 | mA | Idle mode, 16MHz |
| | | | | 50 | uA | Power down mode |

Note1: Under steady state (non-transient) conditions, IOL must be externally

Limited as follows : Maximum IOL per port pin : 10mA

Maximum IOL per 8-bit port : port 0 :26mA

port 1,2,3 :15mA

Maximum total IOL for all output pins : 71mA

If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Note2 : Minimum VCC for Power-down is 2V.

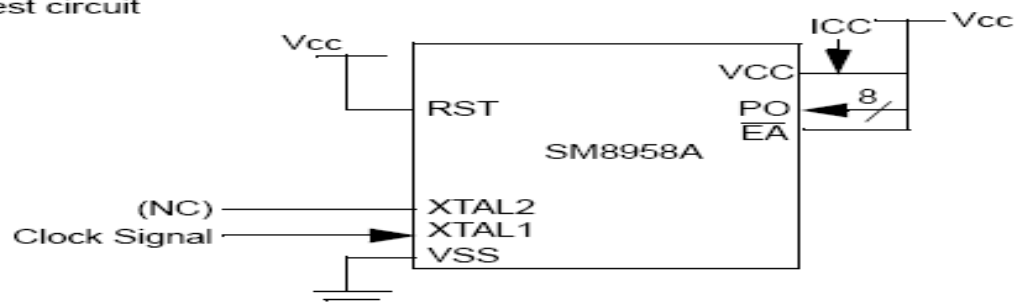


AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

| Symbol | Parameter | Valid Cycle | fosc=16MHz | | | Variable fosc | | | Unit | Remarks |
|----------|-----------------------------------|-------------|------------|------|-----|---------------|--------|----------|------|---------|
| | | | Min. | Typ. | Max | Min. | Typ. | Max | | |
| T LHLL | ALE pulse width | RD/WRT | 115 | | | 2xT - 10 | | | nS | |
| T AVLL | Address Valid to ALE low | RD/WRT | 43 | | | T - 20 | | | nS | |
| T LLAX | Address Hold after ALE low | RD/WRT | 53 | | | T - 10 | | | nS | |
| T LLIV | ALE low to Valid Instruction In | RD | | | 240 | | | 4xT - 10 | nS | |
| T LLPL | ALE low to #PSEN low | RD | 53 | | | T - 10 | | | nS | |
| T PLPH | #PSEN pulse width | RD | 173 | | | 3xT - 15 | | | nS | |
| T PLIV | #PSEN low to Valid Instruction In | RD | | | 177 | | | 3xT - 10 | nS | |
| T PXIX | Instruction Hold after #PSEN | RD | 0 | | | 0 | | | nS | |
| T PXIZ | Instruction Float after #PSEN | RD | | | 87 | | | T + 25 | nS | |
| T AVIV | Address to Valid Instruction In | RD | | | 292 | | | 5xT - 20 | nS | |
| T PLAZ | #PSEN low to Address Float | RD | | | 10 | | | 10 | nS | |
| T RLRH | #RD pulse width | RD | 365 | | | 6xT - 10 | | | nS | |
| T WLWH | #WR pulse width | WRT | 365 | | | 6xT - 10 | | | nS | |
| T RLDV | #RD low to Valid Data In | RD | | | 302 | | | 5xT - 10 | nS | |
| T RHDX | Data Hold after #RD | RD | 0 | | | 0 | | | nS | |
| T RHDZ | Data Float after #RD | RD | | | 145 | | | 2xT + 20 | nS | |
| T LLDV | ALE low to Valid Data In | RD | | | 590 | | | 8xT - 10 | nS | |
| T AVDV | Address to Valid Data In | RD | | | 542 | | | 9xT - 20 | nS | |
| T LLYL | ALE low to #WR High or #RD low | RD/WRT | 178 | | 197 | 3xT - 10 | | 3xT + 10 | nS | |
| T AVYL | Address Valid to #WR or #RD low | RD/WRT | 230 | | | 4xT - 20 | | | nS | |
| T QVWH | Data Valid to #WR High | WRT | 403 | | | 7xT - 35 | | | nS | |
| T QVWX | Data Valid to #WR transition | WRT | 38 | | | T - 25 | | | nS | |
| T WHQX | Data hold after #WR | WRT | 73 | | | T + 10 | | | nS | |
| T RLAZ | #RD low to Address Float | RD | | | | | | 5 | nS | |
| T YALH | #WR or #RD high to ALE high | RD/WRT | 53 | | 72 | T - 10 | | T + 10 | nS | |
| T CHCL | clock fall time | | | | | | | | nS | |
| T CLCX | clock low time | | | | | | | | nS | |
| T CLCH | clock rise time | | | | | | | | nS | |
| T CHCX | clock high time | | | | | | | | nS | |
| T, TCLCL | clock period | | | 63 | | | 1/fosc | | nS | |

ICC Active mode test circuit

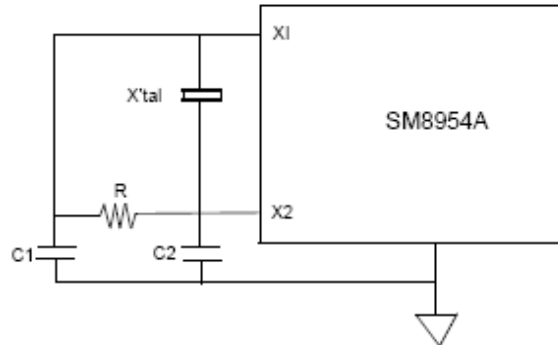


Specifications subject to change without notice contact your sales representatives for the most recent information.
ISSFD-M017 Ver:D SM8954A



Application Reference

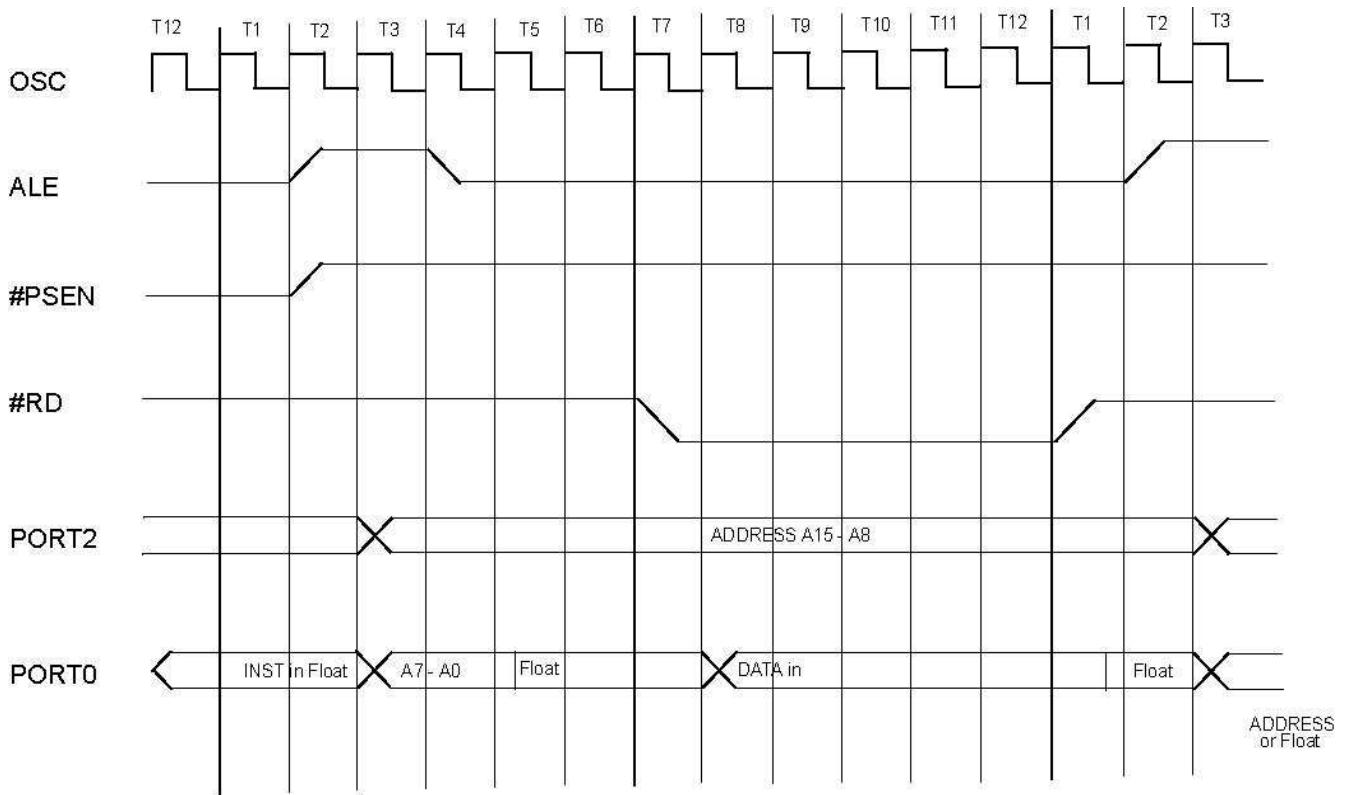
| Valid for SM8954A | | | | |
|-------------------|-------|-------|-------|-------|
| X'tal | 3MHz | 6MHz | 9MHz | 12MHz |
| C1 | 30 pF | 30 pF | 30 pF | 30 pF |
| C2 | 30 pF | 30 pF | 30 pF | 30 pF |
| R | open | open | open | open |
| | | | | |
| X'tal | 16MHz | 25MHz | 33MHz | 40MHz |
| C1 | 30 pF | 15 pF | 5 pF | 2 pF |
| C2 | 30 pF | 15 pF | 5 pF | 2 pF |
| R | open | 62KΩ | 6.8KΩ | 4.7KΩ |



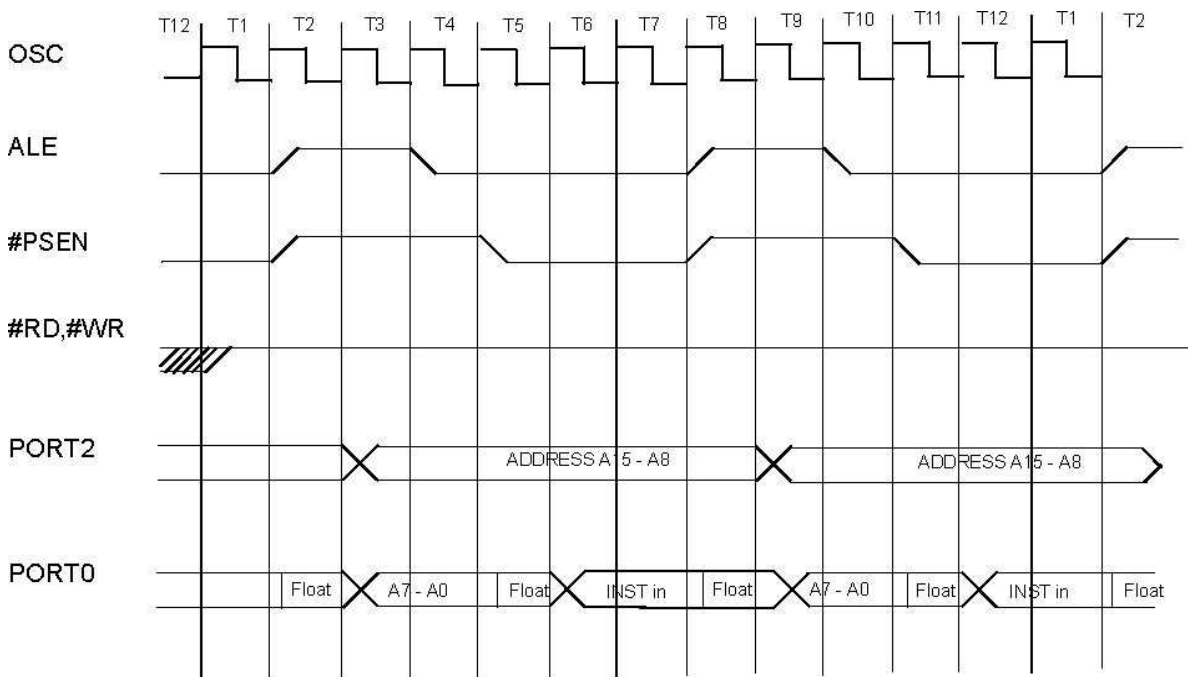
NOTE: Oscillation circuit may differ with different crystal or ceramic resonator in higher oscillation frequency which is due to each crystal or ceramic resonator having its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate values of external components.



Data Memory Read Cycle Timing



Program Memory Read Cycle Timing

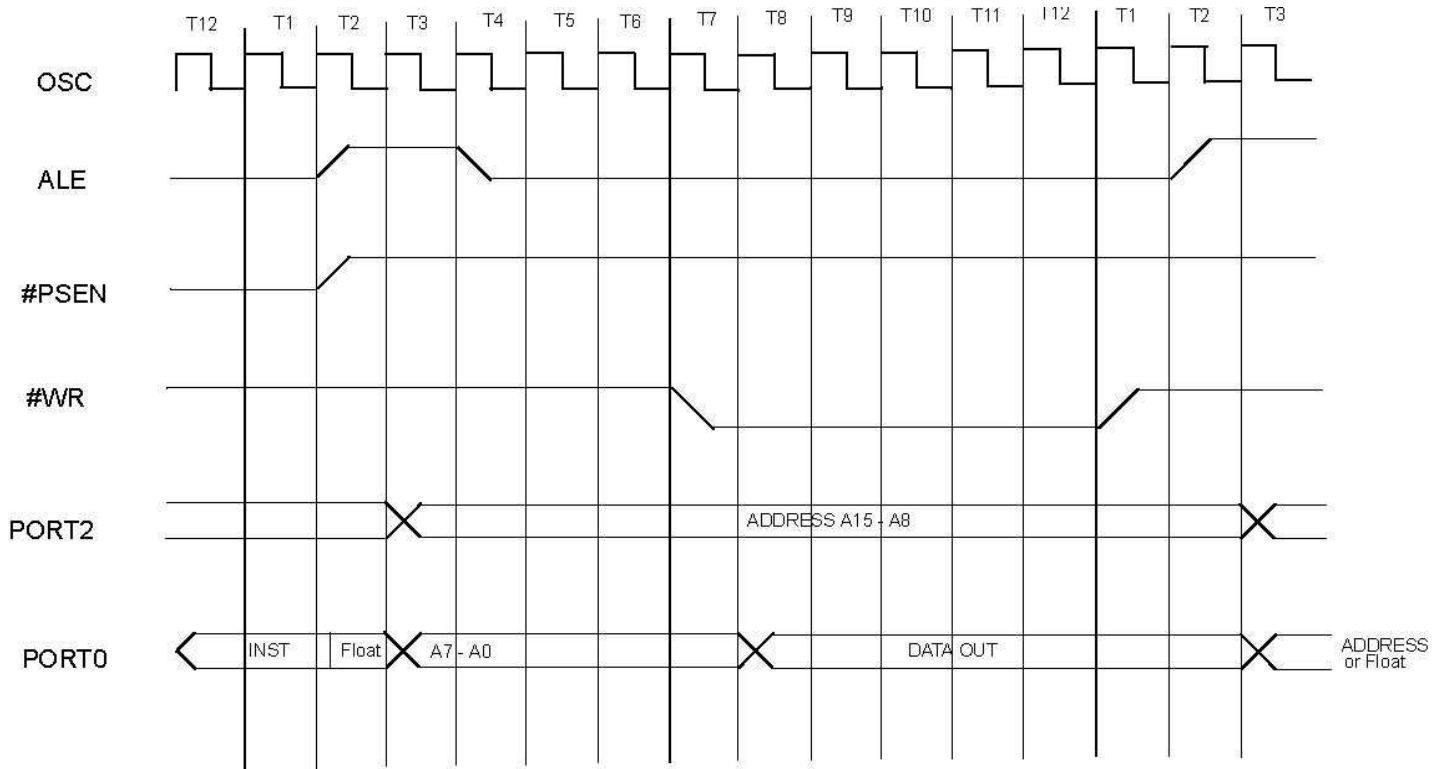


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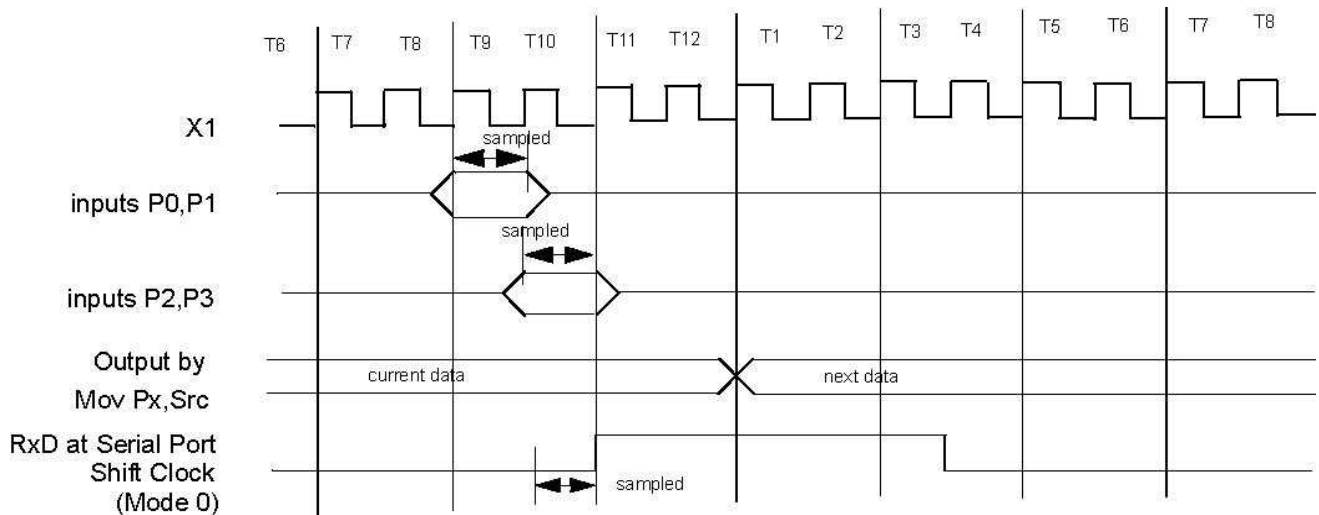
01/2012



Data Memory Write Cycle Timing

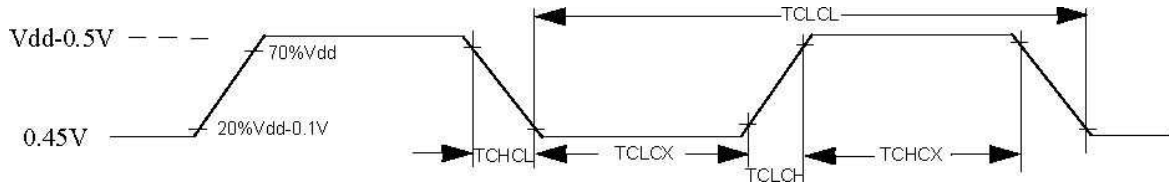


I/O Ports Timing

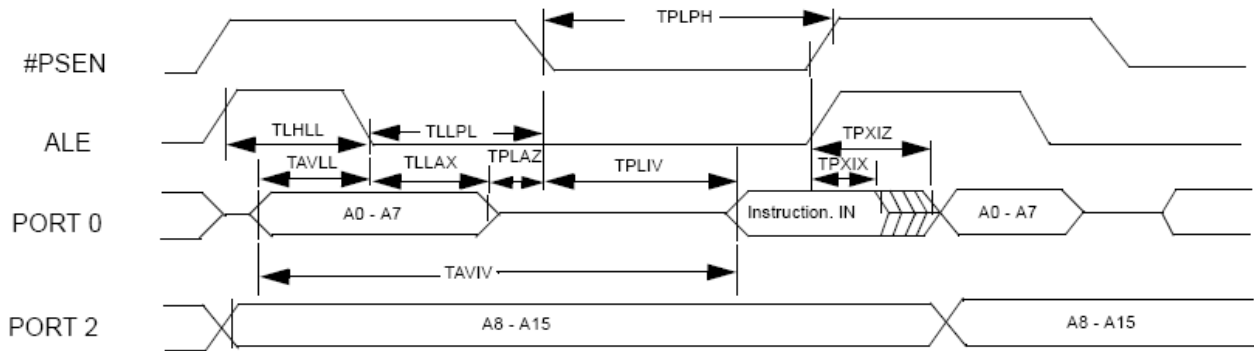




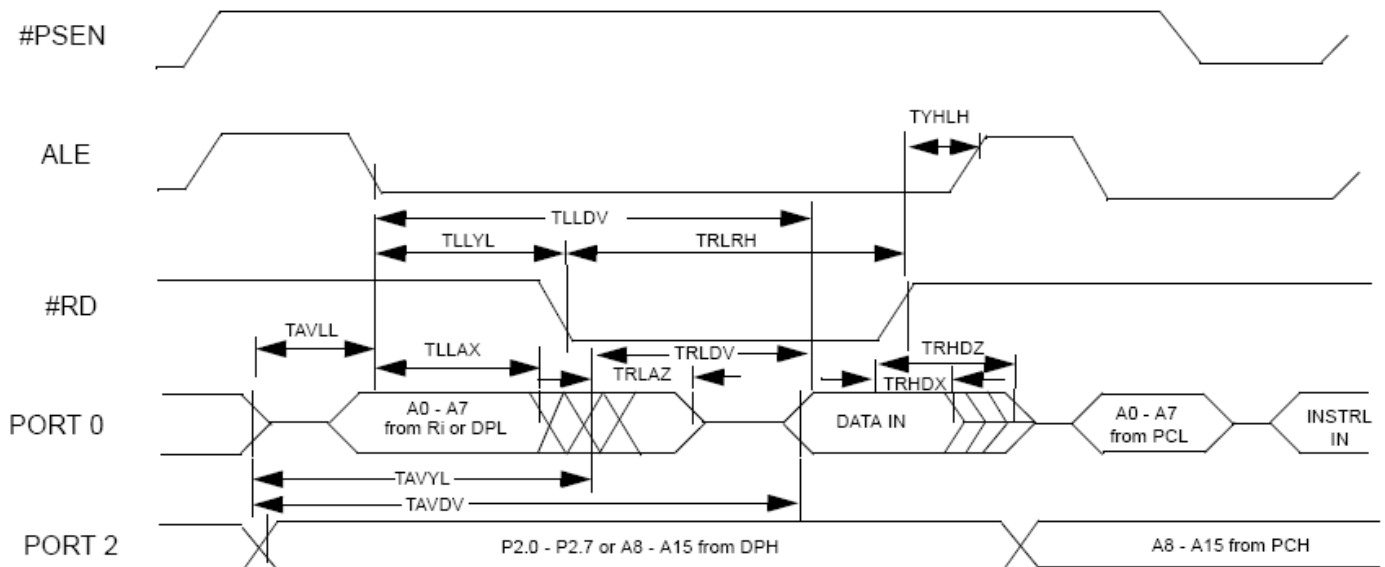
Timing Critical, Requirement of External Clock (V_{ss}=0.0V is assumed)



Tm.I External Program Memory Read Cycle



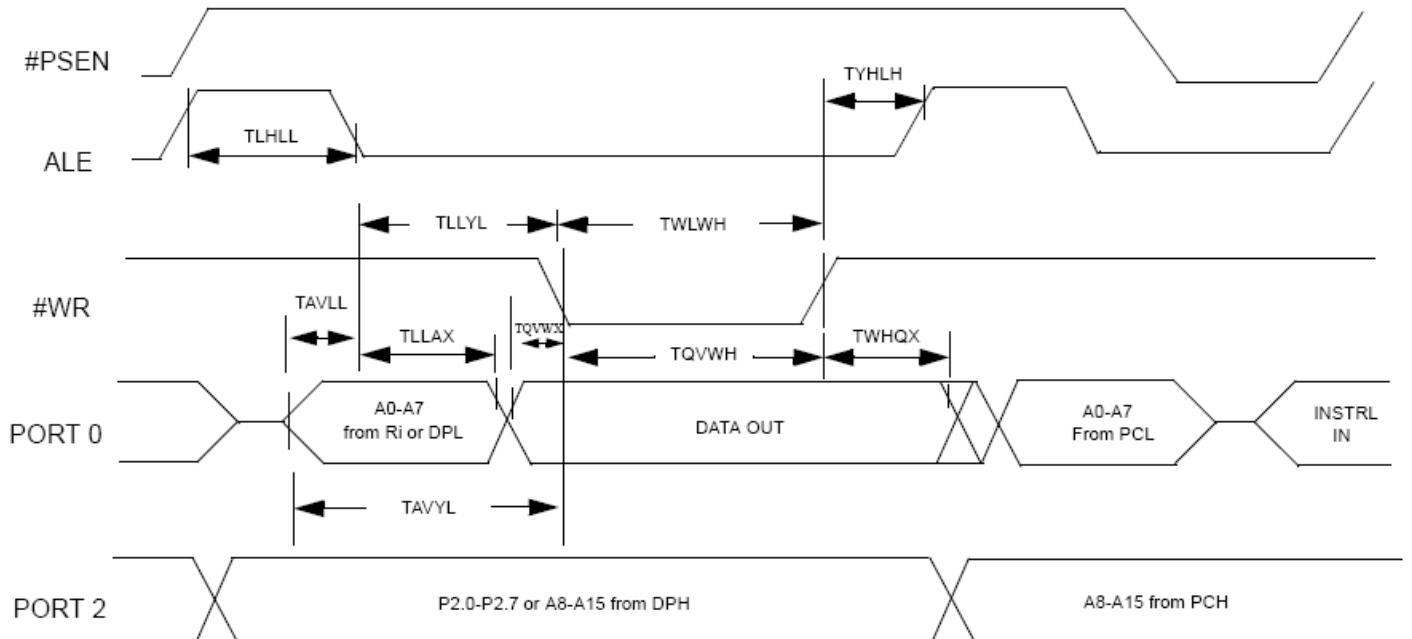
Tm.II External Data Memory Read Cycle



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Tm.III External Data Memory Write Cycle





| MCU writer list | | |
|---|--|--|
| Company | Contact info | Programmer Model Number |
| <u>Advantech</u> 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw | Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw | Lab Tool - 48XP/UXP Lab Tool – 848/848XP |
| <u>Hi-Lo</u> 4F.,No.18,Lane 79,Rueiguang Rd.,Neihu,Taipei,Taiwan R.O.C. Web site: http://www.hilosystems.com.tw | Tel: 02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw | All - 100 series |
| <u>Leap</u> 6th F1-4, Lane 609, Chungshin Rd., Sec. 5, Sanchung, Taipei , Taiwan, ROC Web site: http://www.leap.com.tw | Tel: 886-2-29991860 Fax:02-29990015 E-mail: service@leap.com.tw | Leap-48 |
| <u>Xeltek Electronic Co., Ltd</u> Bldg 6-31 Meizhiguo garden, #2 Jiangjun Ave., Jiangning, Nanjing, China 211100 Web site: http://www.xeltek-cn.com | Tel: + 86-25-52765201, E-mail: fl@xeltek.com.cn zxl@xeltek.com.cn | Superpro 280U Superpro 580U Superpro 3000U Superpro 9000U |
| <u>Guangzhou Zhiyuan Electronic Co.,Ltd</u> Floor 2,No.7 building,Huangzhou Industrial Estate,Chebei Road,Tianhe district,Guangzhou,China 510660 Web site: http://www.embedtools.com/ | TEL: +86-20-28872449 E-mail: mcu@programtec.com | SmartPRO 5000U/X8 |
| <u>TianJin Weilei technology ltd</u> Rm 357,Venturetech Center,12 Keyan West Road Nankai District,Tianjin,P.R.C, 300192 Web site: http://www.weilei.com.cn/ | TEL: + 86-22-87891218#801 E-mail: weilong@weilei.com.cn cm@weilei.com.cn | VP-890;VP-980;VP-880;VP-680 VP-480;VP-380;VP-280;VP-190 |
| <u>GuangZhou Chang Xingjinggong Technology Development Co., Ltd.</u> Room 102 , No.167 , CuiJing street , ChangXing road , TianHe district , GuangZhou. Web site: http://www.top2048.com/ | TEL: + 86-20-61391469 E-mail: chen@top2048.com | TOP-2007 |