Table of Contents

Product List

SM39R08A5W10MP

Description

The SM39R08A5 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 8K-byte embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.
SM39R08A5 contains 256B on-chip RAM, up to 8 GPIOs (10L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.
The high performance of SM39R08A5 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

SM39R08A5ihhkL yymmv
i: process identifier {U = 1.8V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
yy: year
mm: month
v: version identifier{ A, B,…}

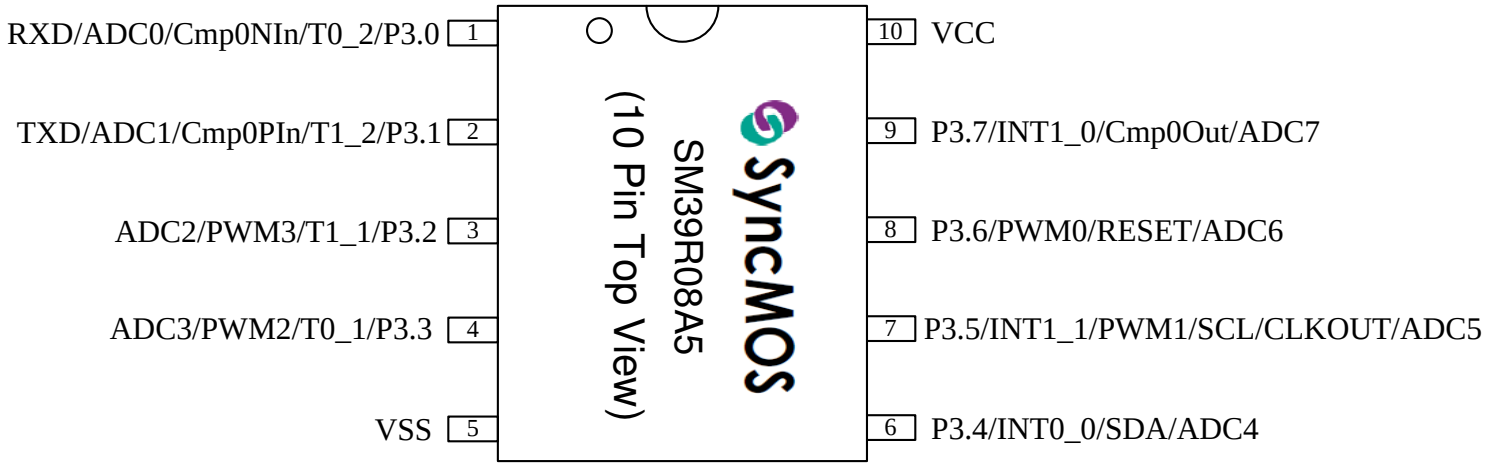
Postfix	Package	Pin / Pad Configuration
M	MSOP (118 mil)	Page 4

Features

- Operating Voltage: 1.8V ~ 5.5V
- 1~8T modes are software programmable.
- Instruction-set compatible with MCS-51.
- 22.1184MHz Internal RC oscillator, with programmable clock divider
- 8K Bytes on-chip flash program memory.
- 256 bytes RAM as standard 8052,
- One serial peripheral interfaces in full duplex mode.
  1.1 Synchronous mode, fixed baud rate,
  1.2 8-bit UART mode, variable baud rate.
  1.3 9-bit UART mode, fixed baud rate,
  1.4 9-bit UART mode, variable baud rate.
- Additional Baud Rate Generator
- Two 16-bit Timer/Counters. (Timer 0, 1)
- 8 GPIOs(10L MSOP)
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode)
- 10 bit PWM x 4 channel
- 8 channel 10-bit analog-to-digital converter (ADC)
- On-Chip Comparator x 1
- On–chip flash memories support IAP/ICP and EEPROM functions.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- EMI reduction mode (ALE output inhibited).
- LVI/LVR.
- IO PAD ESD over 4KV.
- Enhance user code protection.
- External interrupt 0, 1 with four priority levels.
- Power management unit for IDLE and power down modes.

Pin Configuration

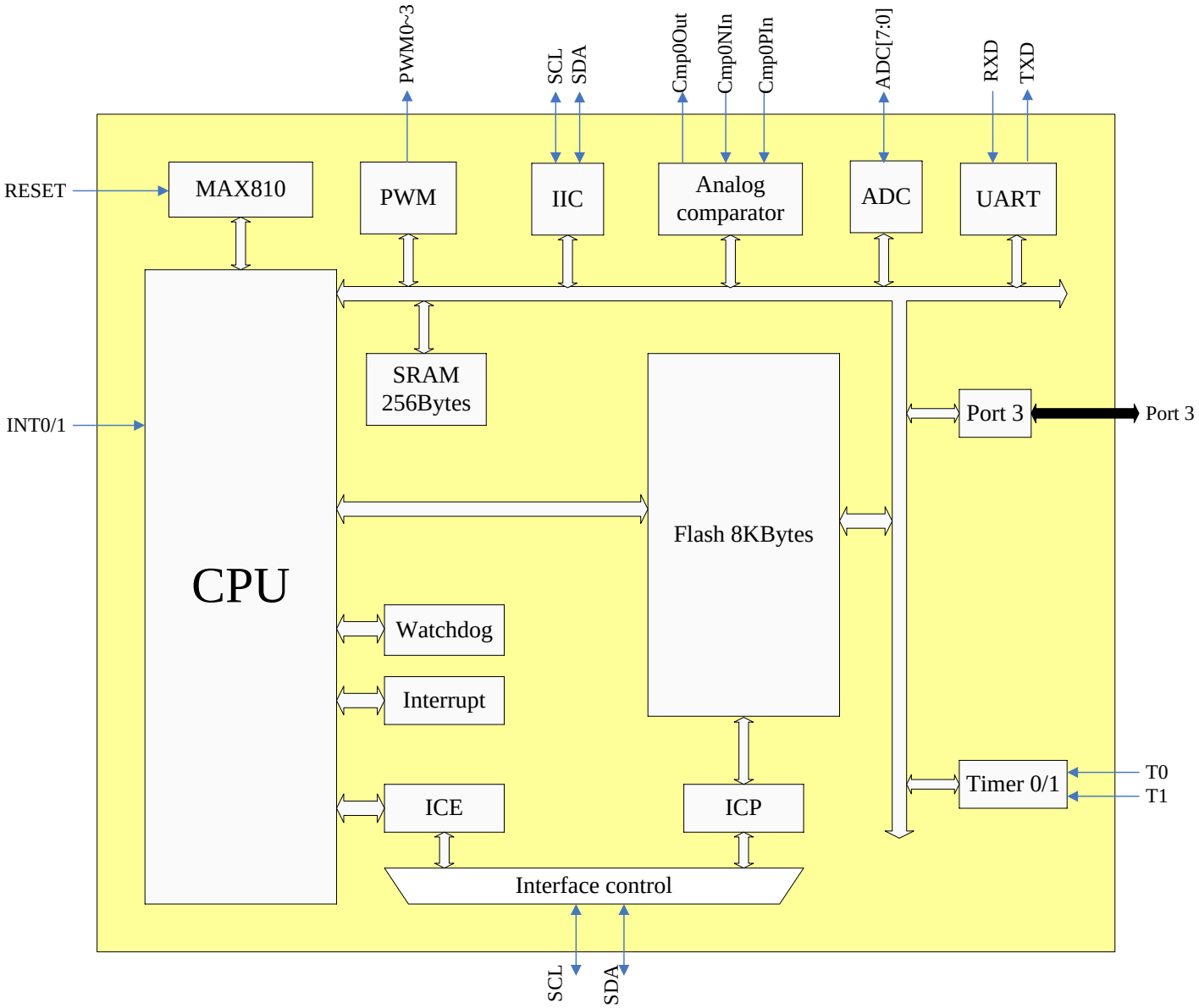
10 Pin MSOP



Notes：

1. The pin Reset/P3.6 factory default is GPIO(P3.6). User can configure it to Reset by a flash programmer.

Block Diagram



Pin Description

10 Pin	Symbol	I/O	Description
1	- P3.0 - RXD - T0_2 - Cmp0Nin - ADC0	I/O	- Bit 0 of port 3 - Serial interface receive data - Timer 0 external input 2 - Comparator 0 negative input - ADC input channel 0
2	- P3.1 - TXD - T1_2 - Cmp0PIn - ADC1	I/O	- Bit 1 of port 3 - Serial interface transmit data - Timer 1 external input 2 - Comparator 0 positive input - ADC input channel 1
3	- P3.2 - PWM3 - ADC2 - T1_1	I/O	- Bit 2 of port 3 - PWM channel 3 - ADC input channel 2 - Timer 1 external input 1
4	- P3.3 - PWM2 - ADC3 - T0_1	I/O	- Bit 3 of port 3 - PWM channel 2 - ADC input channel 3 - Timer 0 external input 1
5	VSS	I	Power supply
6	- P3.4 - INT0_0 - SDA - ADC4	I/O	- Bit 4 of port 3 - External interrupt 0 - IIC SDA pin & On-Chip Instrumentation Command and data I/O pin synchronous to SCL in ICE and ICP functions - ADC input channel 4
7	- P3.5 - INT1_1 - PWM1 - SCL - CLKOUT - ADC5	I/O	- Bit 5 of port 3 - External interrupt 1 - PWM channel 1 - IIC SCL pin & On-Chip Instrumentation Clock I/O pin of ICE and ICP functions - Clock output - ADC input channel 5
8	- P3.6 - RESET - PWM0 - ADC6	I/O	- Bit 6 of port 3 - Reset pin - PWM channel 0 - ADC input channel 6
9	- P3.7 - INT1_0 - Cmp0Out - ADC7	I/O	- Bit 7 of port 3 - External interrupt 1 - Comparator 0 output - ADC input channel 7
10	VDD	I	Power supply

Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICEBT	CMP0CON		**FF**
F0	B						OPPIN	TAKEY	**F7**
E8									**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC		LVC	SWRES	**E7**
D8			P3M0	P3M1					**DF**
D0	PSW								**D7**
C8							PWMMDH	PWMMDL	**CF**
C0	IRCON								**C7**
B8	IEN1	IP1	SRELH		PWMD0H	PWMD0L	PWMD1H	PWMD1L	**BF**
B0	P3	PWMD2H	PWMD2L	PWMD3H	PWMD3L	PWMC	WDTC	WDTK	**B7**
A8	IEN0	IP0	SRELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	**AF**
A0		RSTS							**A7**
98	SCON	SBUF	IEN2						**9F**
90		AUX						IRCON2	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	**8F**
80		SP	DPL	DPH	DPL1	DPH1		PCON	**87**

Note: Special Function Registers reset values and description for SM39R08A5

Register	Location	Reset value	Description
SP	81h	07h	Stack Pointer
DPL	82h	00h	Data Pointer 0 low byte
DPH	83h	00h	Data Pointer 0 high byte
DPL1	84h	00h	Data Pointer 1 low byte
DPH1	85h	00h	Data Pointer 1 high byte
PCON	87h	00h	Power Control
TCON	88h	00h	Timer/Counter Control
TMOD	89h	00h	Timer Mode Control
TL0	8Ah	00h	Timer 0, low byte
TL1	8Bh	00h	Timer 1, low byte
TH0	8Ch	00h	Timer 0, high byte
TH1	8Dh	00h	Timer 1, high byte
CKCON	8Eh	10h	Clock control register
IFCON	8Fh	00h	Interface control register

AUX	91h	00h	Auxiliary register
SCON	98h	00h	Serial Port Control Register
SBUF	99h	00h	Serial Port Data Buffer
IEN2	9Ah	00h	Interrupt Enable Register 2
RSTS	A1h	00h	Reset status register
IEN0	A8h	00h	Interrupt Enable Register 0
IP0	A9h	00h	Interrupt Priority Register 0
SRELL	AAh	00h	Serial Port Reload Register, low byte
ADCC1	ABh	00h	ADC Control 1 Register
ADCC2	ACh	00h	ADC Control 2 Register
ADCDH	ADh	00h	ADC data high byte
ADCDL	AEh	00h	ADC data low byte
ADCCS	AFh	00h	ADC clock select
P3	B0h	FFh	Port 3
PWMD2H	B1h	00h	PWM 2 Data register high byte
PWMD2L	B2h	00h	PWM 2 Data register low byte
PWMD3H	B3h	00h	PWM 3 Data register high byte
PWMD3L	B4h	00h	PWM 3 Data register low byte
PWMC	B5h	00h	PWM control register
WDTC	B6h	04h	Watchdog timer control register
WDTK	B7h	00h	Watchdog timer refresh key.
IEN1	B8h	00h	Interrupt Enable Register 1
IP1	B9h	00h	Interrupt Priority Register 1
SRELH	BAh	00h	Serial Port Reload Register, high byte
PWMD0H	BCh	00h	PWM 0 Data register high byte
PWMD0L	BDh	00h	PWM 0 Data register low byte
PWMD1H	BEh	00h	PWM 1 Data register high byte
PWMD1L	BFh	00h	PWM 1 Data register low byte
IRCON	C0h	00h	Interrupt Request Control Register
PWMMDH	CEh	00h	PWM Max Data Register, high byte.
PWMMDL	CFh	00h	PWM Max Data Register, low byte.
PSW	D0h	00h	Program Status Word
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1
ACC	E0h	00h	Accumulator
ISPFAH	E1h	0Fh	ISP Flash Address-High register
ISPFAL	E2h	FFh	ISP Flash Address-Low register
ISPFD	E3h	FFh	ISP Flash Data register
ISPFC	E4h	00h	ISP Flash control register
LVC	E6h	20h	Low voltage control register
SWRES	E7h	00h	Software Reset register
B	F0h	00h	B Register
OPPIN	F6H	00h	Op/Cmp pin select

TAKEY	F7h	00h	Time Access Key register
IICS	F8h	00h	IIC status register
IICCTL	F9h	04h	IIC control register
IICA1	FAh	A0h	IIC channel Address 1 register
IICA2	FBh	60h	IIC channel Address 2 register
IICRWD	FCh	00h	IIC channel Read / Write Data buffer
IICEBT	FDh	00h	IIC Enable Bus Transaction
CMP0CON	FEh	00h	Comparator 0 control

Function Description

1. General Features

SM39R08A5 is an 8-bit micro-controller. All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1. Embedded Flash

The program can be loaded into the embedded 8KB Flash memory via its writer. The high-quality Flash has a 100K-write cycle life, suitable for re-programming and data recording as EEPROM.

1.2. IO Pads

The SM39R08A5 has an I/O port: Port 3. Port 3 is 8-bit port. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As described in section 5.

The RESET Pin can be configured as I/O port P3.6, when the user uses on-chip hardware RESET mechanism.

1.3. Instruction timing Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. SM39R08A5 is a 1T to 8T MCU, i.e., its machine cycle is one-clock to eight-clock. In the other words, it can execute one instruction within one clock to only eight clocks.

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS			-	-	CLKOUT		10H

ITS: Instruction timing select.

ITS [6:4]	Instruction timing
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

The default is in 2T mode, and it can be changed to another Instruction timing mode if CKCON [6:4] (at address 8Eh) is change any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

1.4. The Clock Output Selection

The SM39R08A5 can generate a clock output signal at P3.5. The CKCON [1:0] (at address 8Eh) can change any time.

CLKOUT: Clock output select.

CKCON [1:0]	Mode.
00	GPIO (P3.5)

01	Fosc
10	Fosc/2
11	Fosc/4

1.5. RESET

1.5.1. Hardware RESET function

SM39R08A5 provides on-chip hardware RESET mechanism，the reset duration is programmable by writer or ICP。

on-chip hardware RESET duration
25ms (default)
200ms
100ms
50ms
16ms
8ms
4ms

1.5.2. Software RESET function

SM39R08A5 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that “OR” with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Software Reset function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
SWRES	Software Reset register	E7h	SWRES [7:0]								00H

1.5.3. Reset status

Mnemonic: RSTS Address: A1h

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

PDRF: Pad reset flag.
When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.

WDTF: Watchdog timer reset flag.
When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.

SWRF: Software reset flag.
When MCU is reset by software, SWRF flag will be set to one by hardware. This flag clear by software.

LVRF: Low voltage reset flag.
When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.
When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

1.5.4. Time Access Key register (TAKEY)

Mnemonic: TAKEY — Address: F7H

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Software reset register (SWRES) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

1.5.5. Software Reset register (SWRES)

Mnemonic: SWRES — Address: E7H

7	6	5	4	3	2	1	0	Reset
SWRES [7:0]								00H

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.
SWRES [7:0] = FFh, software reset.
SWRES [7:0] = 00h ~ FEh, MCU no action.

1.5.6. Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable SWRES write attribute
MOV SWRES, #0FFh ; software reset MCU
```

1.6. Clocks

The default clock is the 22.1184MHz Internal OSC. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation.

The internal clock sources are from the internal OSC with difference frequency division as given in Table 1-1, the clock source can set by writer or ICP.

Table 1-1: Selection of clock source

Clock source
22.1184MHz from internal OSC
11.0592MHz from internal OSC
5.5296MHz from internal OSC
2.7648MHz from internal OSC
1.3824MHz from internal OSC

There may be having a little variance in the frequency from the internal OSC. The max variance as giving in Table 1-1

Table 1-1: Temperature with variance

Temperature	Max Variance
25℃	±2%

2. Instruction Set

All SM39R08A5 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the SM39R08A5 Microcontroller core.

Table 2-1: Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

Table 2-2: Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

Table 2-3: Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

Table 2-4: Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long iump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immed. to ind. and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5: Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

3. Memory Structure

The SM39R08A5 memory structure follows general 8052 structure. It is 8KB program memory.

3.1. Program Memory

The SM39R08A5 has 8KB on-chip flash memory which can be used as general program memory or EEPROM. The address range for the 8K byte is $0000 to $1FFF. It can be used to record any data as EEPROM. The procedure of this EEPROM application function is described in the section 15.

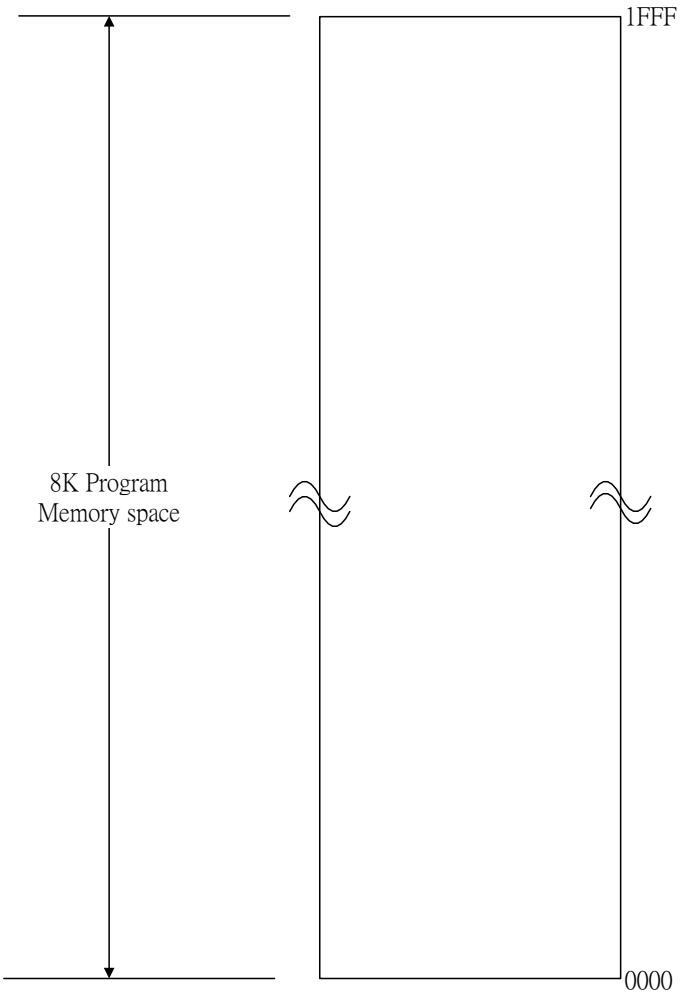


Fig. 3-1: SM39R08A5 programmable Flash

3.2. Data Memory

The SM39R08A5 has 256Bytes on-chip SRAM; 256 Bytes of it are the same as general 8052 internal memory structure

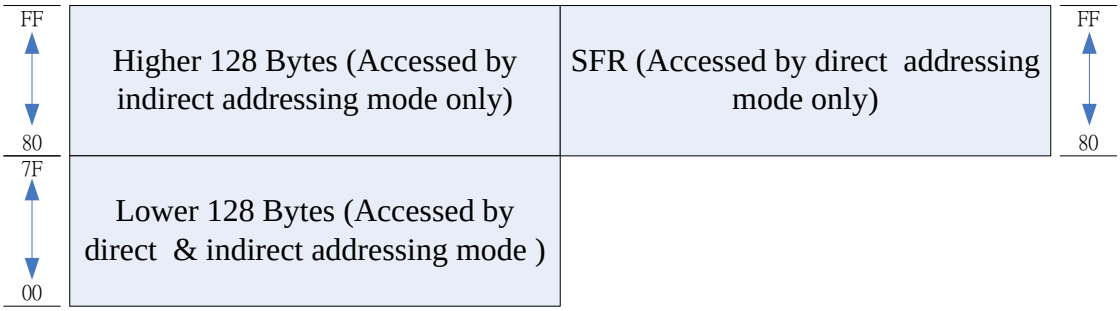


Fig. 3-2: RAM architecture

3.2.1. Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.2.2. Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

4. CPU Engine

The SM39R08A5 engine is composed of four components:

a. Control unit
b. Arithmetic – logic unit
c. Memory control unit
d. RAM and SFR control unit

The SM39R08A5 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following chapter describes the main engine register.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
8051 Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	PSW.1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer low 0	82h	DPL[7:0]								00H
DPH	Data pointer high 0	83h	DPH[7:0]								00H
DPL1	Data pointer low 0	84h	DPL1[7:0]								00H
DPH1	Data pointer high 0	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H
IFCON	Interface control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H

4.1. Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

Mnemonic: ACC **Address: E0h**

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC05	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2. B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B **Address: F0h**

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3. Program Status Word

Mnemonic: PSW **Address: D0h**

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS [1:0]		OV	F1	P	00h

CY: Carry flag.
AC: Auxiliary Carry flag for BCD operations.
F0: General purpose Flag 0 available for user.
RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.
F1: General purpose Flag 1 available for user.
P: Parity flag, affected by hardware to indicate odd/even number of "one" bits in the Accumulator, i.e. even parity.

4.4. Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

Mnemonic: SP **Address: 81h**

7	6	5	4	3	2	1	0	Reset
SP [7:0]								07h

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5. Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR, @DPTR respectively).

Mnemonic: DPL **Address: 82h**

7	6	5	4	3	2	1	0	Reset
DPL [7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH **Address: 83h**

7	6	5	4	3	2	1	0	Reset
DPH [7:0]								00h

DPH [7:0]: Data pointer High 0

4.6. Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the SM39R08A5 core the standard data pointer is called DPTR; the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 **Address: 84h**

7	6	5	4	3	2	1	0	Reset
DPL1 [7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 **Address: 85h**

7	6	5	4	3	2	1	0	Reset
DPH1 [7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H

DPS: Data Pointer selects register.
DPS = 1 is selected DPTR1.

4.7. Interface control register

Mnemonic: IFCON **Address: 8Fh**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

CDPR: code protect (Read Only)
ISPE: ISP function enable bit
ISPE = 1, enable ISP function
ISPE = 0, disable ISP function

5. GPIO

The SM39R08A5 has one I/O ports: Port 3. These are quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the SM39R08A5 may be configured by software to one of four types on a pin-by-pin basis, shown as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00H
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00H

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

The RESET Pin can be configured as I/O port P3.6, when the user uses on-chip hardware RESET mechanism.

For general-purpose applications, every pin can be assigned to either high or low independently as given below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Ports											
Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh

Mnemonic: P3 **Address: B0h**

7	6	5	4	3	2	1	0	Reset
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh

P3.7~ 0: Port3 [7] ~ Port3 [0]

6. Timer 0 and Timer 1

The SM39R08A5 has two 16-bit timer/counter registers: Timer 0 and Timer 1. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register or Timer 1 register is incremented every 12 machine cycles, which means that it counts up after every 12 periods of the clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00h
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00h
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00h
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00h
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
AUX	Auxiliary register	91h	BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H

6.1. Timer/counter mode control register (TMOD)

Mnemonic: TMOD **Address: 89h**

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
Timer 1				Timer 0				

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M[1:0]: Selects mode for Timer/Counter 0 or Timer/Counter 1.

M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8 -bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

6.2. Timer/counter control register (TCON)

Mnemonic: TCON **Address: 88h**

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.
TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.
IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.
IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.
IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

6.3. T0、T1 signal swapping

The T0、T1 signal can be configured to other I/O.

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	PTS [1:0]		PINTS[1:0]		DPS	00H

PTS [1:0]	T0	T1
0x00	-	-
0x01	P3.3(PA03)	P3.2(PA02)
0x10	P3.0(PA00)	P3.1(PA01)
0x11	-	-

7. Serial interface

The serial buffer consists of two separate registers, a transmit buffer and a receive buffer.

Writing data to the Special Function Register SBUF sets this data in serial output buffer and starts the transmission. Reading from the SBUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the first byte before transmission of the second byte is completed.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Serial interface 0											
PCON	Power control	87H	SMOD	-	-	-	-	-	STOP	IDLE	40H
AUX	Auxiliary register	91h	BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H
SCON	Serial Port control register	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SBUF	Serial Port data buffer	99H	SBUF[7:0]								00H
SRELL	Serial Port reload register low byte	AAH	SREL .7	SREL .6	SREL .5	SREL .4	SREL .3	SREL .2	SREL .1	SREL .0	00H
SRELH	Serial Port reload register high byte	BAH	-						SREL .9	SREL .8	00H

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H

BRGS: BRGS = 0 –Baud rate generator use Timer 1 TH1 SFR.
BRGS = 1 –Baud rate generator use SREL SFR.

Mnemonic: SCON **Address: 98h**

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h

SM0,SM1: Serial Port mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes in UART, Mode 0 ~ 3, are explained later.

SM2: Enables multiprocessor communication feature

REN: If set, enables serial reception. Cleared by software to disable reception.

TB8: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB8: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM2 is 0, RB8 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.

TI: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface can operate in the following 4 modes:

SM0	SM1	Mode	Description	Board Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Here Fosc is the crystal or oscillator frequency.

7.1. Mode 0

Pin RXD serves as input and output. TXD outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in SCON as follows: RI = 0 and REN = 1. In other modes, a start bit when REN = 1 starts receiving serial data.

Fig. 7-1: Transmit mode 0

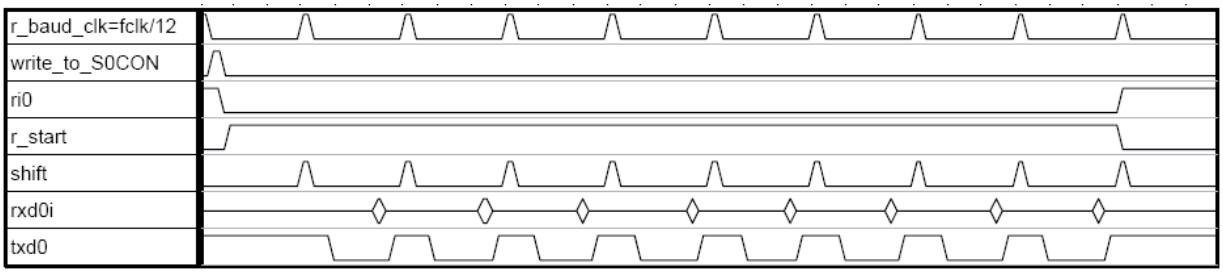


Fig. 7-2: Receive mode 0

7.2. Mode 1

Pin RXD serves as input, and TXD serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF, and stop bit sets the flag RB8 in the Special Function Register SCON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

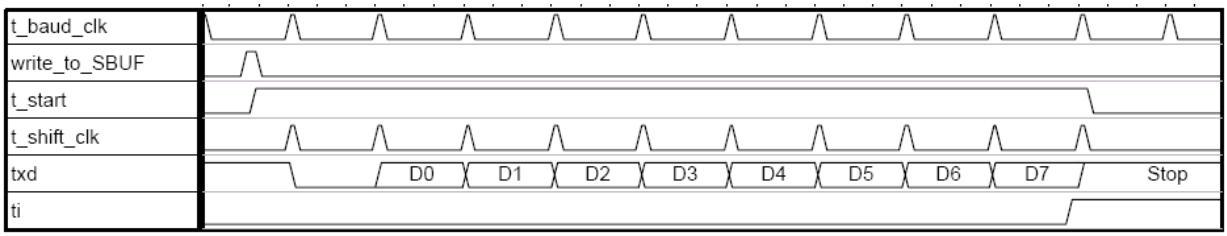


Fig. 7-3: Transmit mode 1

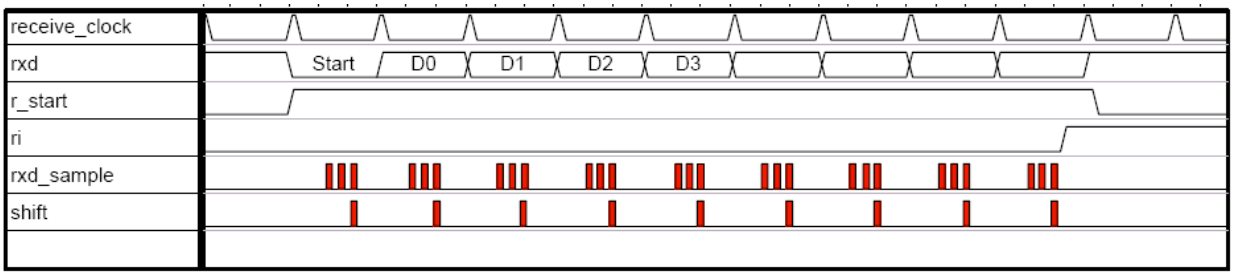


Fig. 7-4: Receive mode 1

7.3. Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in SCON is output as the 9th bit, and at receive, the 9th bit affects RB8 in Special Function Register SCON.

7.4. Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate.

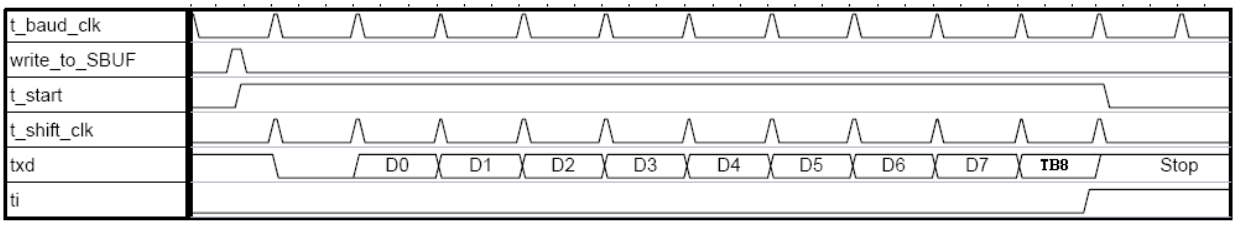


Fig. 7-5: Transmit modes 2 and 3

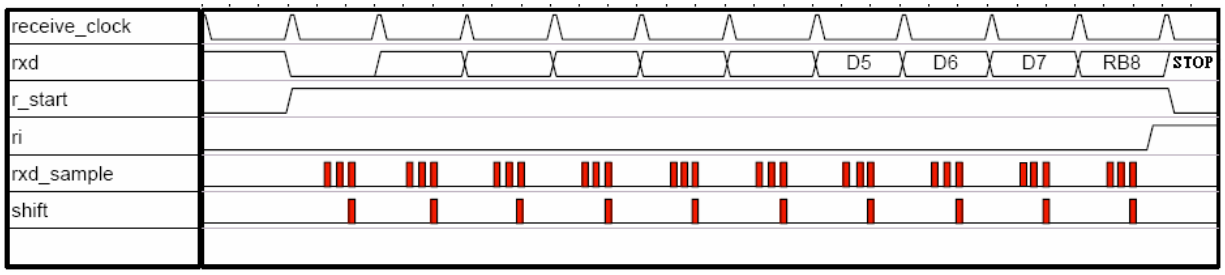


Fig. 7-6: Receive modes 2 and 3

7.5. Multiprocessor communication

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit SM2 in SCON. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM2 and receive the rest of the message, while other slaves will leave SM2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

7.6. Baud rate generator

Serial interface modes 1 and 3

(a) When BRGS = 0 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{32 \times 12 \times (256 - \text{TH1})}$$

(b) When BRGS = 1 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{64 \times (2^{10} - \text{SREL})}$$

8. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTF bit of WDTC register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The watchdog timer has a free running on-chip RC oscillator (23 KHz). The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTE bit of WDTC register. The default WDT time-out period is approximately 178.0ms (WDTM [3:0] = 0100b).

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

$$\text{WDTCLK} = \frac{23\text{KHz}}{2^{\text{WDTM}}}$$

$$\text{Watchdog reset time} = \frac{256}{\text{WDTCLK}}$$

Table 8.1 WDT time-out period

WDTM [3:0]	Divider (23 KHz RC oscillator in)	Time period @ 23KHz
0000	1	11.1ms
0001	2	22.2ms
0010	4	44.5ms
0011	8	89.0ms
0100	16	178.0ms (default)
0101	32	356.1ms
0110	64	712.3ms
0111	128	1.4246s
1000	256	2.8493s
1001	512	5.6987s
1010	1024	11.397s
1011	2048	22.795s
1100	4096	45.590s
1101	8192	91.180s
1110	16384	182.36s
1111	32768	364.72s

Note: RC oscillator (23 KHz), about ± 20% of variation

When MCU is reset, the MCU will be read WDTEN control bit status. When WDTEN bit is set to 1, the watchdog function will be disabled no matter what the WDTE bit status is. When WDTEN bit is clear to 0, the watchdog function will be enabled if WDTE bit is set to 1 by program. User can to set WDTEN on the writer or ISP.

The program can enable the WDT function by programming 1 to the WDTE bit premise that WDTEN control bit is clear to 0. After WDTE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTM [3:0]. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset.

Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active.

When Watchdog timer is overflow, the WDTF flag will set to one and automatically reset MCU. The WDTF flag can be clear by software or external reset or power on reset.

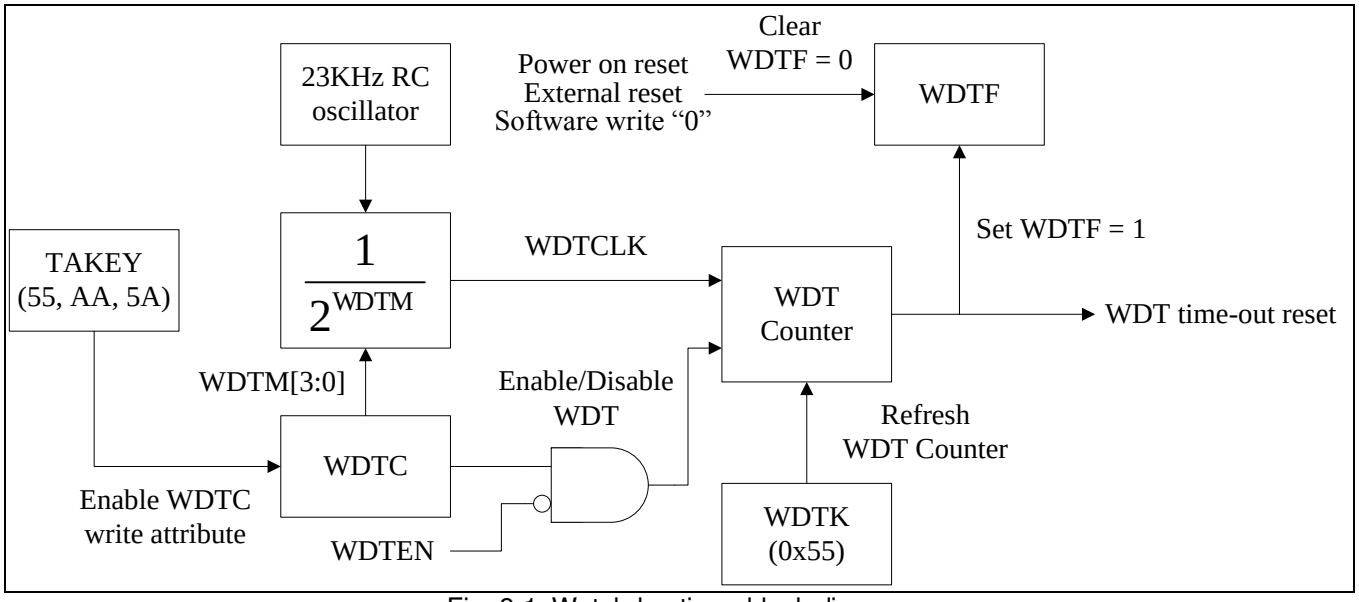


Fig. 8-1: Watchdog timer block diagram

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Watchdog Timer											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
WDTC	Watchdog timer control register	B6h		CWDTR	WDTE	-	WDTM [3:0]				04H
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]								00H
RSTS	Reset status register	A1h	-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

Mnemonic: TAKEY **Address: F7h**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTC) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

WDTF: Watchdog timer reset flag.
When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.

Mnemonic: WDTC **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	CWDTR	WDTE	-	WDTM [3:0]				04H

CWDTR: 0: watchdog reset
1: watchdog interrupt

WDTE: Control bit used to enable Watchdog timer.
The WDTE bit can be used only if WDTEN, the bit7 of information block OP3, is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.
0: Disable WDT.
1: Enable WDT.
The WDTE bit is not used if WDTEN, the bit7 of information block OP3, is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. Please see table 7.8.1 to reference the WDT time-out period.

Mnemonic: WDTK **Address: B7h**

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.
A programmer must write 0x55 into WDTK register, and then the watchdog timer will be cleared to zero.

For example, if enable WDT and select time-out reset period is 2.8493s.
First, programming the information block OP3 bit7 WDTEN to “0”.
Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah          ; enable WDTC write attribute.
MOV WDTC, #28h           ; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable WDT
                         ; function.
.
.
.
MOV WDTK, #55h           ; Clear WDT timer to 0.
```

For example 2, if enable WDT and select time-out Interrupt period is 178.0ms.
First, programming the information block OP3 bit7 WDTEN to “0”.
Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah          ; enable WDTC write attribute.
MOV WDTC, #64h           ; Set WDTM [3:0] = 0100b. Set WDTE =1 to enable WDT function
                         ; and Set CWDTR =1 to enable period interrupt function
```

9. Interrupt

The SM39R08A5 provides 9 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, and IEN1.

When the interrupt occurs, the engine will vector to the predetermined address as shown in Table 9.1. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 9-1: Interrupt vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Number *(use Keil C Tool)
IE0 – External interrupt 0	0003h	0
TF0 – Timer 0 interrupt	000Bh	1
IE1 – External interrupt 1	0013h	2
TF1 – Timer 1 interrupt	001Bh	3
RI/TI – Serial channel interrupt	0023h	4
PWMIF – PWM interrupt	0043h	8
ADCIF – A/D converter interrupt	0053h	10
LVIIF – Low Voltage Interrupt	0063h	12
IICIF – IIC interrupt	006Bh	13
WDTIF–WDT interrupt	008Bh	17
Comparator interrupt	0093h	18

*See Keil C about C51 User's Guide about Interrupt Function description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Interrupt											
AUX	Auxiliary register	91h	BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H
IEN0	Interrupt Enable 0 register	A8H	EA	-	-	ES0	ET1	EX1	ET0	EX0	00H
IEN1	Interrupt Enable 1 register	B8H	-	-	IEIIC	IELVI	-	IEADC	-	IEPWM	00H
IEN2	Interrupt Enable 2 register	9AH	-	-	-	-	-	ECmpI	IEWDT	-	00H
IRCON	Interrupt request register	C0H	-	-	IICIF	LVIIF	-	ADCIF	-	PWMIF	00H
IRCON2	Interrupt request register 2	97H	-	-	-	-	-	CmpIF	WDTIF	-	00H
IP0	Interrupt priority level 0	A9H	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00H
IP1	Interrupt priority level 1	B9H	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00H

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	PTS[1:0]		PINTS[1:0]		DPS	00H

The INT0、INT1 signal can be configured to other I/O.

PINTS [1:0]	INT0	INT1
0x00	-	P3.7
0x01	-	P3.5

Interrupt Enable 0 register (IEN0)

Mnemonic: IEN0 **Address: A8h**

7	6	5	4	3	2	1	0	Reset
EA	-	-	ES0	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.
ES0: ES0=0 – Disable Serial channel 0 interrupt.
ES0=1 – Enable Serial channel 0 interrupt.
ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.
EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.
ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.
EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Interrupt Enable 1 register (IEN1)

Mnemonic: IEN1 **Address: B8h**

7	6	5	4	3	2	1	0	Reset
-	-	IEIIC	IELVI	-	IEADC	-	IEPWM	00h

IELVI: LVI interrupt enable.
IELVI = 0 – Disable LVI interrupt.
IELVI = 1 – Enable LVI interrupt.
IEIIC: IIC interrupt enable.
IEIICS = 0 – Disable IIC interrupt.
IEIICS = 1 – Enable IIC interrupt.
IEADC: A/D converter interrupt enable
IEADC = 0 – Disable ADC interrupt.
IEADC = 1 – Enable ADC interrupt.
IEPWM: PWM interrupt enable.
IEPWM = 0 – Disable PWM interrupt.
IEPWM = 1 – Enable PWM interrupt.

Interrupt Enable 2 register (IEN2)

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	ECmpI	IEWDT	-	00H

ECmpI: Enable Comparator 0 interrupt
IEWDT: WDT interrupt enable.
IEWDT = 0 – Disable WDT interrupt.
IEWDT = 1 – Enable WDT interrupt.

Interrupt request register (IRCON)

Mnemonic: IRCON **Address: C0h**

7	6	5	4	3	2	1	0	Reset
-	-	IICIF	LVIIF	-	ADCIF	-	PWMIF	00H

LVIIF: LVI interrupt flag. Clear by hardware automatically
IICIF: IIC interrupt flag. Clear by hardware automatically
ADCIF: A/D converter end interrupt flag.
PWMIF: PWM interrupt flag. Clear by hardware automatically

Interrupt request register 2 (IRCON2)

Mnemonic: IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	CmpIF	WDTIF	-	00H

CmpIF: Comparator interrupt flag
HW will clear this flag automatically when enter interrupt vector.
SW can clear this flag also.(in case analog comparator INT disable)
WDTIF: WDT interrupt flag.

All interrupt sources are combined in groups:

Table 9-2: Priority level groups

Groups		
External interrupt 0	-	PWM interrupt
Timer 0 interrupt	WDT interrupt	-
External interrupt 1	Comparator interrupt	ADC interrupt
Timer 1 interrupt	-	-
Serial channel interrupt	-	LVI interrupt
-	-	IIC interrupt

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first.

Mnemonic: IP0 **Address: A9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h

Mnemonic: IP1 **Address: B9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

Table 9-3: Priority levels

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 9-4: Groups of priority

Bit	Group		
IP1.0, IP0.0	External interrupt 0	-	PWM interrupt
IP1.1, IP0.1	Timer 0 interrupt	WDT interrupt	-
IP1.2, IP0.2	External interrupt 1	Comparator interrupt	ADC interrupt
IP1.3, IP0.3	Timer 1 interrupt	-	-
IP1.4, IP0.4	Serial channel interrupt	-	LVI interrupt
IP1.5, IP0.5	-	-	IIC interrupt

Table 9-5: Polling sequence

Interrupt source	Sequence
External interrupt 0	Polling sequence ↓
PWM interrupt	
Timer 0 interrupt	
WDT interrupt	
External interrupt 1	
Comparator interrupt	
ADC interrupt	
Timer 1 interrupt	
Serial channel 0 interrupt	
LVI interrupt	
IIC interrupt	

10. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	-	-	-	-	-	STOP	IDLE	40h

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.
Stop bit is always read as 0
IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.
Idle bit is always read as 0

10.1. Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

10.2. Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state only if interrupts asserted from external INT0/1, LVI and WDT interrupt, or hardware reset by WDT and LVR.

11. PWM - Pulse Width Modulation

SM39R08A5 provides four-channel PWM outputs.
The interrupt vector is 43h.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
PWM											
PWMC	PWM Control register	B5h	PWMCS[2:0]			-	PWM3EN	PWM2EN	PWM1EN	PWM0EN	00H
PWMD0H	PWM 0 Data register high byte	BCh	PWMP0	-	-	-	-	-	PWMD0[9:8]		00H
PWMD0L	PWM 0 Data register low byte	BDh	PWMD0[7:0]								00H
PWMD1H	PWM 1 Data register high byte	BEh	PWMP1	-	-	-	-	-	PWMD1[9:8]		00H
PWMD1L	PWM 1 Data register low byte	BFh	PWMD1[7:0]								00H
PWMD2H	PWM 2 Data register high byte	B1h	PWMP2	-	-	-	-	-	PWMD2[9:8]		00H
PWMD2L	PWM 2 Data register low byte	B2h	PWMD2[7:0]								00H
PWMD3H	PWM 3 Data register high byte	B3h	PWMP3	-	-	-	-	-	PWMD3[9:8]		00H
PWMD3L	PWM 3 Data register low byte	B4h	PWMD3[7:0]								00H
PWMMDH	PWM Max Data register high byte	CEh	-	-	-	-	-	-	PWMMD[9:8]		00H
PWMMDL	PWM Max Data register low byte	CFh	PWMMD[7:0]								FFH

Mnemonic: PWMC **Address: B5h**

7	6	5	4	3	2	1	0	Reset
PWMCS[2:0]			-	PWM3EN	PWM2EN	PWM1EN	PWM0EN	00H

PWMCS[2:0]: PWM clock select.

PWMCS [2:0]	Mode
000	Fosc
001	Fosc/2
010	Fosc/4
011	Fosc/6
100	Fosc/8
101	Fosc/12
110	Timer 0 overflow
111	P3.4

PWM3EN: PWM channel 3 enable control bit.
PWM3EN = 1 – PWM channel 3 enable.
PWM3EN = 0 – PWM channel 3 disable.
PWM2EN: PWM channel 2 enable control bit.
PWM2EN = 1 – PWM channel 2 enable.
PWM2EN = 0 – PWM channel 2 disable.
PWM1EN: PWM channel 1 enable control bit.
PWM1EN = 1 – PWM channel 1 enable.
PWM1EN = 0 – PWM channel 1 disable.
PWM0EN: PWM 0 enable control bit.
PWM0EN = 1 – PWM channel 0 enable.
PWM0EN = 0 – PWM channel 0 disable.

Mnemonic: PWMD0H **Address: BCh**

7	6	5	4	3	2	1	0	Reset
PWMP0	-	-	-	-	-	PWMD0[9:8]		00H

Mnemonic: PWMD0L **Address: BDh**

7	6	5	4	3	2	1	0	Reset
PWMD0[7:0]								00H

PWMP0: PWM channel 0 idle polarity select.
"0" – PWM channel 0 will idle low.
"1" – PWM channel 0 will idle high.
PWMD0[9:0]: PWM channel 0 data register.

Mnemonic: PWMD1H **Address: BEh**

7	6	5	4	3	2	1	0	Reset
PWMP1	-	-	-	-	-	PWMD1[9:8]		00H

Mnemonic: PWMD1L **Address: BFh**

7	6	5	4	3	2	1	0	Reset
PWMD1[7:0]								00H

PWMP1: PWM channel 1 idle polarity select.
"0" – PWM channel 1 will idle low.
"1" – PWM channel 1 will idle high.
PWMD1[9:0]: PWM channel 1 data register.

Mnemonic: PWMD2H **Address: B1h**

7	6	5	4	3	2	1	0	Reset
PWMP2	-	-	-	-	-	PWMD2[9:8]		00H

Mnemonic: PWMD2L **Address: B2h**

7	6	5	4	3	2	1	0	Reset
PWMD2[7:0]								00H

PWMP2: PWM channel 2 idle polarity select.
"0" – PWM channel 2 will idle low.
"1" – PWM channel 2 will idle high.
PWMD2[9:0]: PWM channel 2 data register.

Mnemonic: PWMD3H **Address: B3h**

7	6	5	4	3	2	1	0	Reset
PWMP3	-	-	-	-	-	PWMD3[9:8]		00H

Mnemonic: PWMD3L **Address: B4h**

7	6	5	4	3	2	1	0	Reset
PWMD3[7:0]								00H

PWMP3: PWM channel 3 idle polarity select.
"0" – PWM channel 3 will idle low.
"1" – PWM channel 3 will idle high.
PWMD3[9:0]: PWM channel 3 data register.

Mnemonic: PWMMDH **Address: CEh**

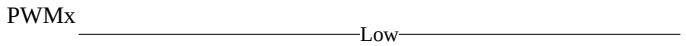
7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	PWMMD[9:8]		00H

Mnemonic: PWMMDL **Address: CFh**

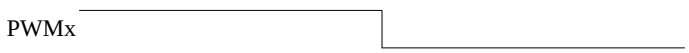
7	6	5	4	3	2	1	0	Reset
PWMMD[7:0]								FFH

PWMMD[9:0]: PWM Max Data register.
PWM count from 0000h to PWMMD[9:0]. When PWM count data equal PWMMD[9:0] is overflow.

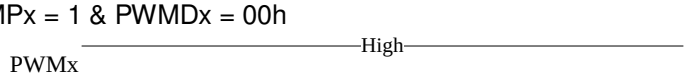
PWMPx = 0 & PWMDx = 00h



PWMPx = 0 & PWMDx ≠ 00h



PWMPx = 1 & PWMDx = 00h



PWMPx = 1 & PWMDx ≠ 00h

$$\text{PWM period} = \frac{\text{PWMMD}+1}{\text{PWM clock}}$$

$$\text{Leader pulse} = \frac{\text{PWMDx}}{\text{PWM clock}}$$

12. IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detects START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

The interrupt vector is 6Bh.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
IIC function											
IICCTL	IIC control register	F9h	IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]			04H
IICS	IIC status register	F8h	-	MPIF	LAIF	RXIF	TXIF	RXAK	TXAK	RW,BB	00H
IICA1	IIC Address 1 register	FAh	IICA1[7:1]							MATCH1or RW1	A0H
IICA2	IIC Address 2 register	FBh	IICA2[7:1]							MATCH2 or RW2	60H
IICRWD	IIC Read/Write register	FCh	IICRWD[7:0]								00H
IICEBT	IIC Enaable Bus Transaction	FDh	FU_EN			-					00H

Mnemonic: IICCTL **Address: F9h**

7	6	5	4	3	2	1	0	Reset
IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]			04h

IICEN: Enable IIC module
IICEN = 1 is Enable
IICEN = 0 is Disable.
MSS: Master or slave mode select.
MSS = 1 is master mode.
MSS = 0 is slave mode.
*The software must set this bit before setting others register.
MAS: Master address select (master mode only)
MAS = 0 is to use IICA1.
MAS = 1 is to use IICA2.
AB_EN: Arbitration lost enable bit. (Master mode only)
If set AB_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.
BF_EN: Bus busy enable bit. (Master mode only)
If set BF_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when MStart is set. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IICBR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/512 for users' convenience.

IICBR[2:0]	Baud rate
000	Fosc/32
001	Fosc/64
010	Fosc/128
011	Fosc/256
100	Fosc/512
101	Fosc/1024
110	Fosc/2048
111	Fosc/4096

Mnemonic: IICS **Address: F8H**

7	6	5	4	3	2	1	0	Reset
-	MPIF	LAIF	RXIF	TXIF	RXAK	TxAK	RW	00H

MPIF: The Stop condition Interrupt Flag
The stop condition occurred and this bit will be set. Software need to clear this bit

LAIF: Arbitration lost bit. (Master mode only)
The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit

RxIF: The data Receive Interrupt Flag (RXIF) is set after the IICRWD (IIC Read Write Data Buffer) is loaded with a newly receive data.

TxIF: The data Transmit Interrupt Flag (TXIF) is set when the data of the IICRWD (IIC Read Write Data Buffer) is downloaded to the shift register.

RxAK: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data transmit on the bus.

TxAK: The Acknowledge status transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and transmit to master to indicate the receive status.

RW: **Master Mode:**
Bus busy bit
If detect scl=0 or sda=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.
Slave Mode:
The slave mode read (received) or wrote (transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only)

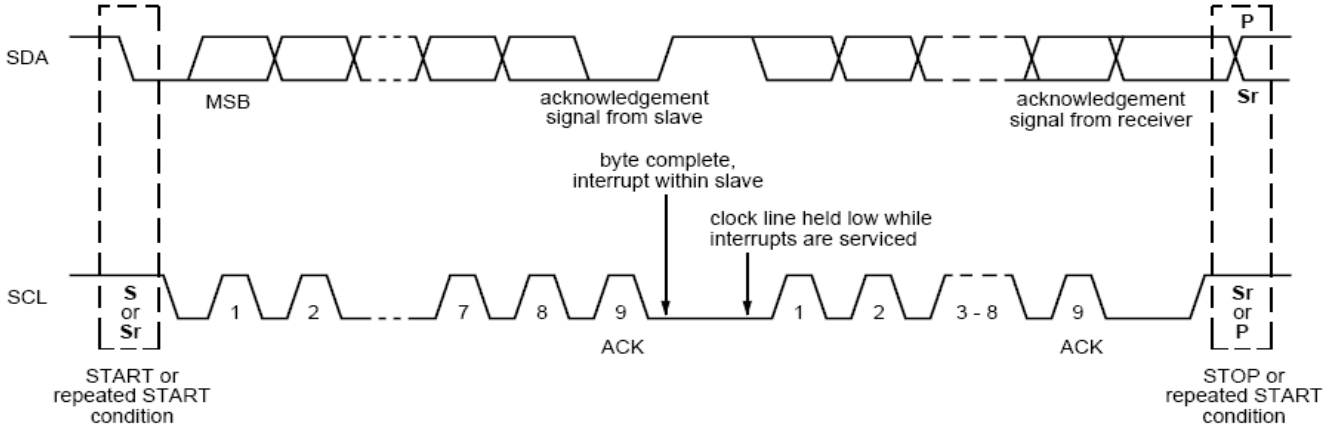


Fig. 11-1: Acknowledgement bit in the 9th bit of a byte transmission

Mnemonic: IICA1 **Address: FAH**

7	6	5	4	3	2	1	0	Reset
IICA1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IICA1[7:1]: IIC Address registers
This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received

Match1: When IICA1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets or send first data, this bit will clear automatically.

Master mode:

IICA1[7:1]: IIC Address registers
This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It appears at the 8th bit after the IIC address as shown in Fig. 14-2. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode.

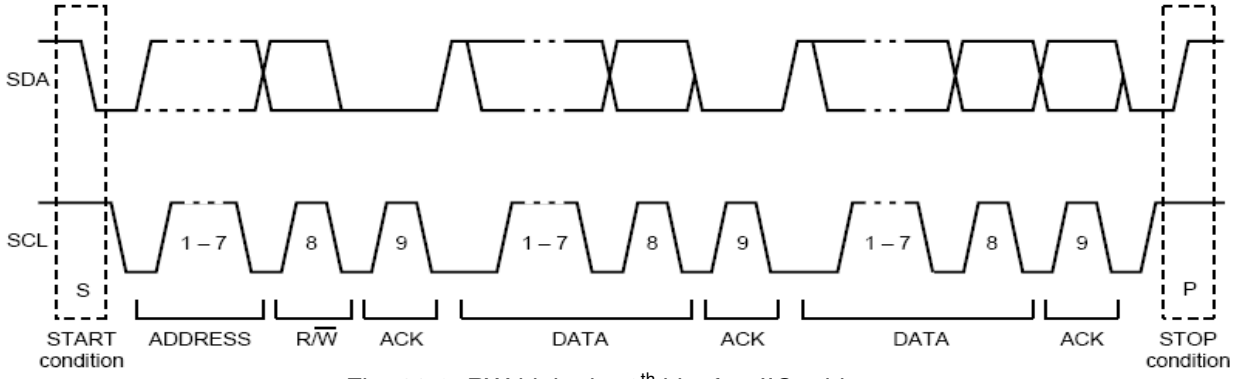


Fig. 11-2: RW bit in the 8th bit after IIC address

Mnemonic: IICA2 **Address: FBh**

7	6	5	4	3	2	1	0	Reset
IICA2[7:1]							Match2 or RW2	60h
R/W							R or R/W	

Slave mode:

IICA2[7:1]: IIC Address registers
This is the second 7-bit address for this slave module.
It will be checked when an address (from master) is received

Match2: When IICA2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets or send first data, this bit will clear automatically.

Master mode:

IICA2[7:1]: IIC Address registers
This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master transmit mode.

Mnemonic: IICRWD **Address: FCh**

7	6	5	4	3	2	1	0	Reset
IICRWD[7:0]								00h

IICRWD[7:0]: IIC read write data buffer.
In receiving (read) mode, the received byte is stored here.
In transmitting mode, the byte to be shifted out through SDA stays here.

Mnemonic: IICEBT **Address: FDH**

7	6	5	4	3	2	1	0	Reset
FU_EN		-	-	-	-	-	-	00H

Master Mode：

00: reserved
01: IIC bus module will enable read/write data transfer on SDA and SCL.
10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IICA1/IICA2(selected by MAS control bit)
11: IIC bus module generate a stop condition on the SDA/SCL.

Slave mode:

01: FU_EN[7:6] should be set as 01 only. The other value is inhibited.
Notice:
1. FU_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).
2. FU_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.
3. In transmit data mode (slave mode), the output data should be filled into IICRWD before setting FU_EN[7:6] as 01.
4. FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

13. LVI – Low Voltage Interrupt

The interrupt vector 63h.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Watchdog Timer											
RSTS	Reset status register	A1h	-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H
LVC	Low voltage control register	E6h	LVI_EN	-	LVRE	LVIF	-	-	LVIS		20H

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

PDRF: Pad reset flag.
When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.
LVRF: Low voltage reset flag.
When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.
PORF: Power on reset flag.
When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

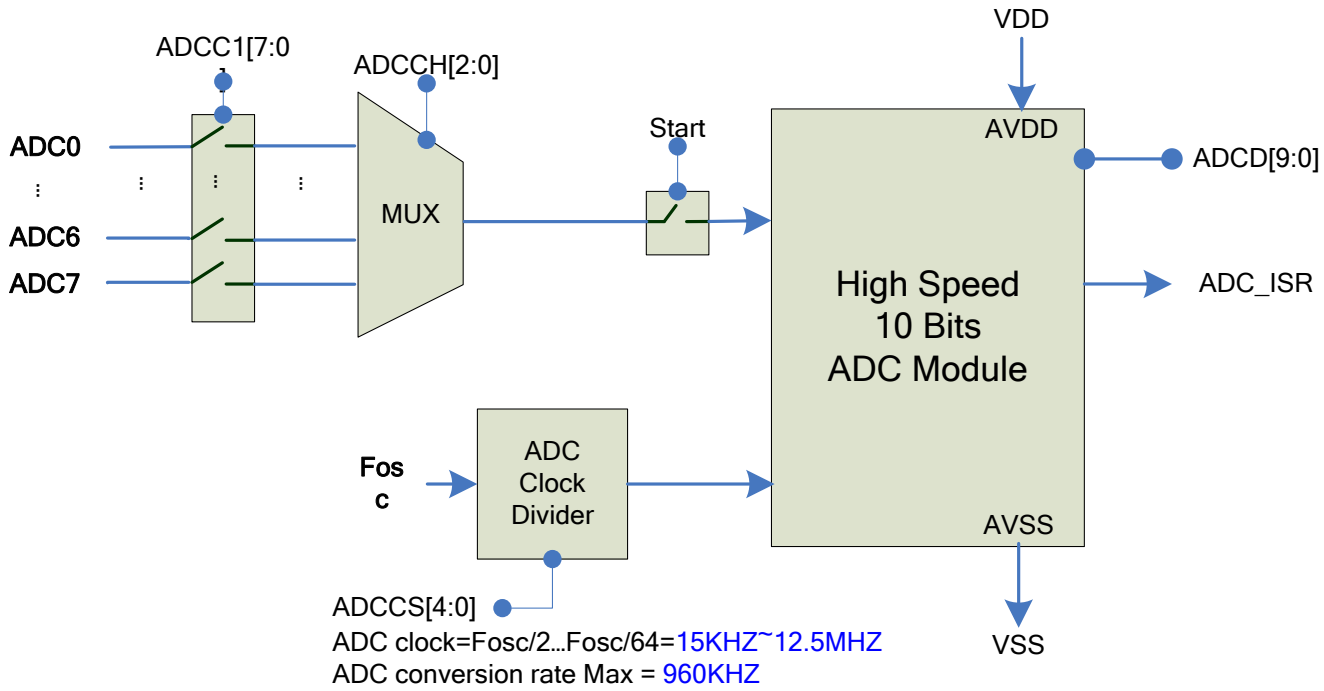
Mnemonic: LVC **Address: E6h**

7	6	5	4	3	2	1	0	Reset
LVI_EN	-	LVRE	LVIF	-	-	LVIS[1:0]		20H

LVI_EN: Low voltage interrupt function enable bit.
LVI_EN = 0 - disable low voltage detect function.
LVI_EN = 1 - enable low voltage detect function.
LVRE: External low voltage reset function enable bit.
LVRE = 0 - disable external low voltage reset function.
LVRE = 1 - enable external low voltage reset function.
LVIF: Low Voltage interrupt Flag (Read only)
LVIS LVI level select:
00: 1.7V
01: 2.60V
10: 3.2V
11: 4.0V

14. 10-bit Analog-to-Digital Converter (ADC)

The SM39R08A5 provides eight channels 10-bit ADC. The Digital output DATA [9:0] were put into ADCD [9:0].
The ADC interrupt vector is 53H.



The ADC SFR show as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
ADC											
ADCC1	ADC Control register 1	ABh	ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H
ADCC2	ADC Control register 2	ACh	Start	ADJUST	-	-	-	ADCCH[2:0]			00H
ADCDH	ADC data high byte	ADh	ADCDH [7:0]								00H
ADCDL	ADC data low byte	AEh	ADCDL [7:0]								00H
ADCCS	ADC clock select	AFh	-	-	-	ADCCS[4:0]					00H

Mnemonic: ADCC1 **Address: ABh**

7	6	5	4	3	2	1	0	Reset
ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H

ADC7EN: ADC channels 7 enable.
ADC7EN = 1 – Enable ADC channel 7
ADC6EN: ADC channels 6 enable.
ADC6EN = 1 – Enable ADC channel 6
ADC5EN: ADC channels 5 enable.
ADC5EN = 1 – Enable ADC channel 5

ADC4EN: ADC channels 4 enable.
ADC4EN = 1 – Enable ADC channel 4
ADC3EN: ADC channels 3 enable.
ADC3EN = 1 – Enable ADC channel 3
ADC2EN: ADC channels 2 enable.
ADC2EN = 1 – Enable ADC channel 2
ADC1EN: ADC channels 1 enable.
ADC1EN = 1 – Enable ADC channel 1
ADC0EN: ADC channels 0 enable.
ADC0EN = 1 – Enable ADC channel 0

Mnemonic: ADCC2 **Address: ACh**

7	6	5	4	3	2	1	0	Reset
Start	ADJUST	-	-	-	ADCCH[2:0]			00H

Start: When this bit is set, the ADC will be start conversion continuous.
ADJUST: Adjust the format of ADC conversion DATA.
ADJUST = 0: (default value)
ADC data high byte ADCD [9:2] = ADCDH [7:0].
ADC data low byte ADCD [1:0] = ADCDL [1:0].
ADJUST = 1: ADC data high byte ADCD [9:8] = ADCDH [1:0].
ADC data low byte ADCD [7:0] = ADCDL [7:0].
ADCCH[2:0]: ADC channel select.

ADCCH [2:0]	Channel
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

ADJUST = 0:

Mnemonic: ADCDH **Address: ADh**

7	6	5	4	3	2	1	0	Reset
ADCD[9]	ADCD[8]	ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	00H

Mnemonic: ADCDL **Address: AEh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	ADCD[1]	ADCD[0]	00H

ADJUST = 1:

Mnemonic: ADCDH **Address: ADh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	ADCD[9]	ADCD[8]	00H

Mnemonic: ADCDL **Address: AEh**

7	6	5	4	3	2	1	0	Reset
ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	ADCD[1]	ADCD[0]	00H

ADCD[9:0]: ADC data register.

Mnemonic: ADCCS **Address: AFh**

7	6	5	4	3	2	1	0	Reset
-	-	-	ADCCS[4]	ADCCS[3]	ADCCS[2]	ADCCS[1]	ADCCS[0]	00H

ADCCS[4:0]: ADC clock select.

*The ADC clock maximum 12.5MHz.

*The ADC Conversion rate maximum 960KHz.

ADCCS[4:0]	ADC Clock(Hz)	Clocks for ADC Conversion
00000	Fosc /2	46
00001	Fosc/4	92
00010	Fosc /6	138
00011	Fosc /8	184
00100	Fosc /10	230
00101	Fosc /12	276
00110	Fosc /14	322
00111	Fosc /16	368
01000	Fosc /18	414
01001	Fosc /20	460
01010	Fosc /22	506
01011	Fosc /24	552
01100	Fosc /26	598
01101	Fosc /28	644
01110	Fosc /30	690
01111	Fosc /32	736
10000	Fosc /34	782
10001	Fosc /36	828
10010	Fosc /38	874
10011	Fosc /40	920
10100	Fosc /42	966
10101	Fosc /44	1012
10110	Fosc /46	1058
10111	Fosc /48	1104
11000	Fosc /50	1150
11001	Fosc /52	1196
11010	Fosc /54	1242
11011	Fosc /56	1288
11100	Fosc /58	1334
11101	Fosc /60	1380
11110	Fosc /62	1426
11111	Fosc /64	1472

$$ADC\_Clock = \frac{Fosc}{2 \times (ADCCS + 1)}$$

$$ADC\_Conversion\_Rate = \frac{ADC\_Clock}{13}$$

15. EEPROM

The SM39R08A5 can generate flash control signal by internal hardware circuit. The SM39R08A5 provides internal flash control signals which can do flash program/page erase functions.

ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
ISP function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
IFCON	Interface Control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H
ISPFAH	ISP Flash Address - High register	E1h	ISPFAH [7:0]								FFH
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]								FFH
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]								FFH
ISPFC	ISP Flash Control register	E4h	-	-	-	-	-	ISPF.2	ISPF.1	ISPF.0	00H

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON **Address: 8FH**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall SM39R08A5 EEPROM function by setting ISPE bit to 1, to disable overall EEPROM function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

Mnemonic: ISPFAH **Address: E1H**

7	6	5	4	3	2	1	0	Reset
ISPFAH7	ISPFAH6	ISPFAH5	ISPFAH4	ISPFAH3	ISPFAH2	ISPFAH1	ISPFAH0	FFH

ISPFAH [7:0]: Flash address-high for EEPROM function

Mnemonic: ISPFAL **Address: E2H**

7	6	5	4	3	2	1	0	Reset
ISPFAL7	ISPFAL6	ISPFAL5	ISPFAL4	ISPFAL3	ISPFAL2	ISPFAL1	ISPFAL0	FFH

ISPFAL [7:0]: Flash address-Low for EEPROM function

Mnemonic: ISPFD **Address: E3H**

7	6	5	4	3	2	1	0	Reset
ISPFD7	ISPFD6	ISPFD5	ISPFD4	ISPFD3	ISPFD2	ISPFD1	ISPFD0	FFH

ISPFD [7:0]: Flash data for byte programming function.

Mnemonic: ISPFC **Address: E4H**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	ISPF[2]	ISPF[1]	ISPF[0]	00H

ISPF [2:0]: ISP function select bit.

ISPF[2:0]	ISP function
000	Byte program
010	Page erase

One page of flash memory is 128 byte

The choice EEPROM function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases function, user need to specify flash address at first. When performing page erase function, SM39R08A5 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $XYMN

page erase function will erase from $XY00 to $XY7F or $XY80 to $XYFF

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah      ; enable ISPE write attribute
ORL IFCON, #01H       ; enable SM39R08A5 ISP function
MOV ISPFAH, #10H     ; set flash address-high, 10H
MOV ISPFAL, #05H      ; set flash address-low, 05H
MOV ISPFD, #22H       ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H       ; start to program #22H to the flash address $1005H
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah       ; enable ISPE write attribute
ANL IFCON, #0FEH      ; disable SM39R08A5 ISP function
```

16. Comparator

SM39R08A5 had integrated a Comparator in chip. This module supports Comparator modes individually according to user's configuration. When use it as comparator, the comparator output is logical one when positive input greater than negative input, otherwise the output is a zero.

Mnemonic	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Op/Comparator											
OPPIN	Comparator pin select	F6h	-	CMP0EN	C0POS VBG	C0POS PAD	-	-	-	-	00h
CMP0CON	Comparator 0 control	FEh	HYS0EN	CMP0O	CMF0MS[1:0]		CMF0	Cmp0 OutEN	-	-	00h

Mnemonic: OPPIN **Address: F6h**

7	6	5	4	3	2	1	0	Reset
-	CMP0EN	C0POSVBG	C0POSPAD	-	-	-	-	00h

CMP0EN : Cmp0 enable.
1: Comparator_0 circuit enable and switch to corresponding signal in multi-function pin P3.0/P3.1/P3.7 by HW automatically.
C0POSVBG: Select Comparator_0 positive input source
1: set positive input source as internal reference voltage (1.2V±10%)
C0POSPAD: Select Comparator_0 positive input source
1: set positive input source as external pin

Comparator setting table:

CMP0EN	C0POSVBG	C0POSPAD	Cmp0OutEN	Comparator		
				Cmp0PIn	Cmp0NIn	Cmp0Out
0	X	X	X	IO	IO	IO
1	0	0	X	Error	Error	Error
1	0	1	0	CMP	CMP	IO
1	0	1	1	CMP	CMP	CMP
1	1	0	0	IO	CMP	IO
1	1	0	1	IO	CMP	CMP
1	1	1	X	Error	Error	Error

Mnemonic: CMP0CON **Address:FEh**

7	6	5 4	3	2	1	0	Reset
HYS0EN	CMP0O	CMF0MS[1:0]	CMF0	Cmp0 OutEN	-	-	00h

HYS0EN: Hysteresis function enable
0: disable Hysteresis at comparator_0 input
1: enable
CMP0O: Comparator_0 output (read only)
0: The positive input source was lower than negative input source
1: The positive input source was higher than negative input source
CMF0MS[1:0] : CMF0(Comparator_0 Flag) setting mode select
00: CMF0 will be set when comprator_0 output toggle
01: CMF0 will be set when comprator_0 output rising
10: CMF0 will be set when comprator_0 output falling
11: reserved
CMF0: Comparator_0 Flag

This bit is setting by hardware according to meet CMF0MS [1:0] select condition.
This bit must clear by software.

Cmp0OutEN: Comparator_0 Output Enable
0: Comparator_0 will not output to external Pin
1: Comparator_0 will output to external Pin

DC Characteristics

T_A = -40℃ to 85℃, V_{CC} = 5.0V

Symbol	Parameter	Valid	Min	Typ	Max	Units	Conditions
VIL1	Input Low-voltage	Port 3	-0.5		0.8	V	Vcc=5V
VIL2	Input Low-voltage	RES	0		0.8	V	
VIH1	Input High-voltage	Port 3	2.0		V_{CC} + 0.5	V	
VIH2	Input High-voltage	RES	70%Vcc		V_{CC} + 0.5	V	
VOL	Output Low-voltage	P3.0/P3.1/P3.4/P3.7			0.45	V	IOL=20mA Vcc=5V
		P3.2/P3.3/P3.5/P3.6			0.45	V	IOL=38mA Vcc=5V
VOH1	Output High-voltage using Strong Pull-up(1)	P3.0/P3.1/P3.4/P3.7	90%Vcc			V	IOH= -8mA
		P3.2/P3.3/P3.5/P3.6	90%Vcc			V	IOH= -15mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 3	2.4			V	IOH= -250uA
IIL	Logic 0 Input Current	Port 3			-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 3			-650	uA	Vin= 2.0V
ILI	Input Leakage Current	Port 3			±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50		300	kΩ	
CIO	Pin Capacitance				10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		2.6	3.5	mA	Active mode IRC 22.1184MHz V_{CC} =5V 25 ℃
				2.2	3	mA	Idle mode, IRC 22.1184 MHz V_{CC} =5V 25 ℃
				2	6	uA	Power down mode V_{CC} =5V 25 ℃

Notes： 1. Port in Push-Pull Output Mode

2. Port in Quasi-Bidirectional Mode

T_A = -40℃ to 85℃, V_{CC} = 3.0V

Symbol	Parameter	Valid	Min	TYP	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,3	-0.5		0.8	V	Vcc=3.0V
VIL2	Input Low-voltage	RES, XTAL1	0		0.8	V	
VIH1	Input High-voltage	Port 0,1,3	2.0		V_{CC} + 0.5	V	
VIH2	Input High-voltage	RES, XTAL1	70%Vcc		V_{CC} + 0.5	V	
VOL	Output Low-voltage	P3.0/P3.1/P3.4/P3.7			0.45	V	IOL=14mA Vcc=3V
		P3.2/P3.3/P3.5/P3.6			0.45	V	IOL=15mA Vcc=3V
VOH1	Output High-voltage using Strong Pull-up(1)	P3.0/P3.1/P3.4/P3.7	90%Vcc			V	IOH= -5mA
		P3.2/P3.3/P3.5/P3.6	90%Vcc			V	IOH= -10mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0,1,3	2.4			V	IOH= -77uA
IIL	Logic 0 Input Current	Port 0,1,3			-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,3			-650	uA	Vin=1.5V
ILI	Input Leakage Current	Port 0,1,3			±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50		300	kΩ	
CIO	Pin Capacitance				10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		2.2	3	mA	Active mode ,IRC 22.1184 MHz V_{CC} = 3.0 V 25 ℃
				2.1	3	mA	Idle mode, IRC 22.1184 Mhz V_{CC} =3.0V 25 ℃
				1	5	uA	Power down mode V_{CC} =3.0V 25 ℃

Notes： 1. Port in Push-Pull Output Mode

2. Port in Quasi-Bidirectional Mode

Absolute Maximum Ratings

SYMBOL	PARAMETER	MAX	UNIT
Maximum sourced current (Push-pull)	Total I/O pins	100	mA
Maximum sunk current	Total I/O pins	100	mA
Tj	Max. Junction Temperature	150	℃

ADC Characteristics

	Symbol	Test Condition	MIN	TYP	MAX	Unit
Operation	V_{DD}	V_{DD}	2.7		5.5	V
Resolution					10	bit
Conversion time				$13t_{ADC}$		us
Sample rate				870k		Hz
Integral Non-Linearity Error	INL		-1		1	LSB
Differential Non-Linearity	DNL		-1		1	LSB
Clock frequency	ADCCLK			11.36	-5.25	MHz

Comparator Characteristics

Ta=25℃

Symbol	Description	Test Condition		MIN	TPY	MAX	Unit
		V_{DD}	Condition				
I_{OP}	Operating current	5	-	-	10	10	uA
-	Power Down Current	5	-	-	-	0.1	uA
-	Offset voltage	5	-	-10	-	+10	mV
V_{CM}	Input voltage commom mode range	-	-	Vss	-	Vdd-1.5	V
Tp	Propagation delay	5	△ Vin=10mV	-	3	6	us

LVI& LVR Characteristics

	LVR		
	Min	Typical	Max
1.8V ~ 5.5V	VIL=1.4V	VIL=1.5V	VIL=1.6V

	LVI		
	Min	Typical	Max
LVIS[1:0] = 00	VIL=1.6V	VIL=1.7V	VIL=1.8V
LVIS[1:0] = 01	VIL=2.5V	VIL=2.6V	VIL=2.7V
LVIS[1:0] = 10	VIL=3.1V	VIL=3.2V	VIL=3.3V
LVIS[1:0] = 11	VIL=3.9V	VIL=4.0V	VIL=4.1V

Notes : The V_{LVI} always above V_{LVR} about 0.2V