AMD FT1 Processor with A55E/A50M Controller Hub GIZMO

NOTES:

1) This Gizmo schematic is for AMD FT1 Accelerated Processor Unit (APU) and A55E or A50M Controller Hub (CH) based systems. It can be used as a starting point for any design that uses this processor/chipset combination.

2) Passive components only specify a package size if it is relevant to power or current capability.

3) This schematic supports the A55E and A50M Controller Hub variants.

4) Unless Otherwise Specified:

All ceramic capacitors are in uF, 10%, 50V
All Polarized capacitors are aluminum electrolytic
Caps < 1nF are C0G or NPO type
Caps >/= 1nF are X5R type
All resistors have 1% tolerance at 1/16 Watts.
All voltages are DC

5) Interrupted lines coded with the same letter or letter combinations are electrically connected.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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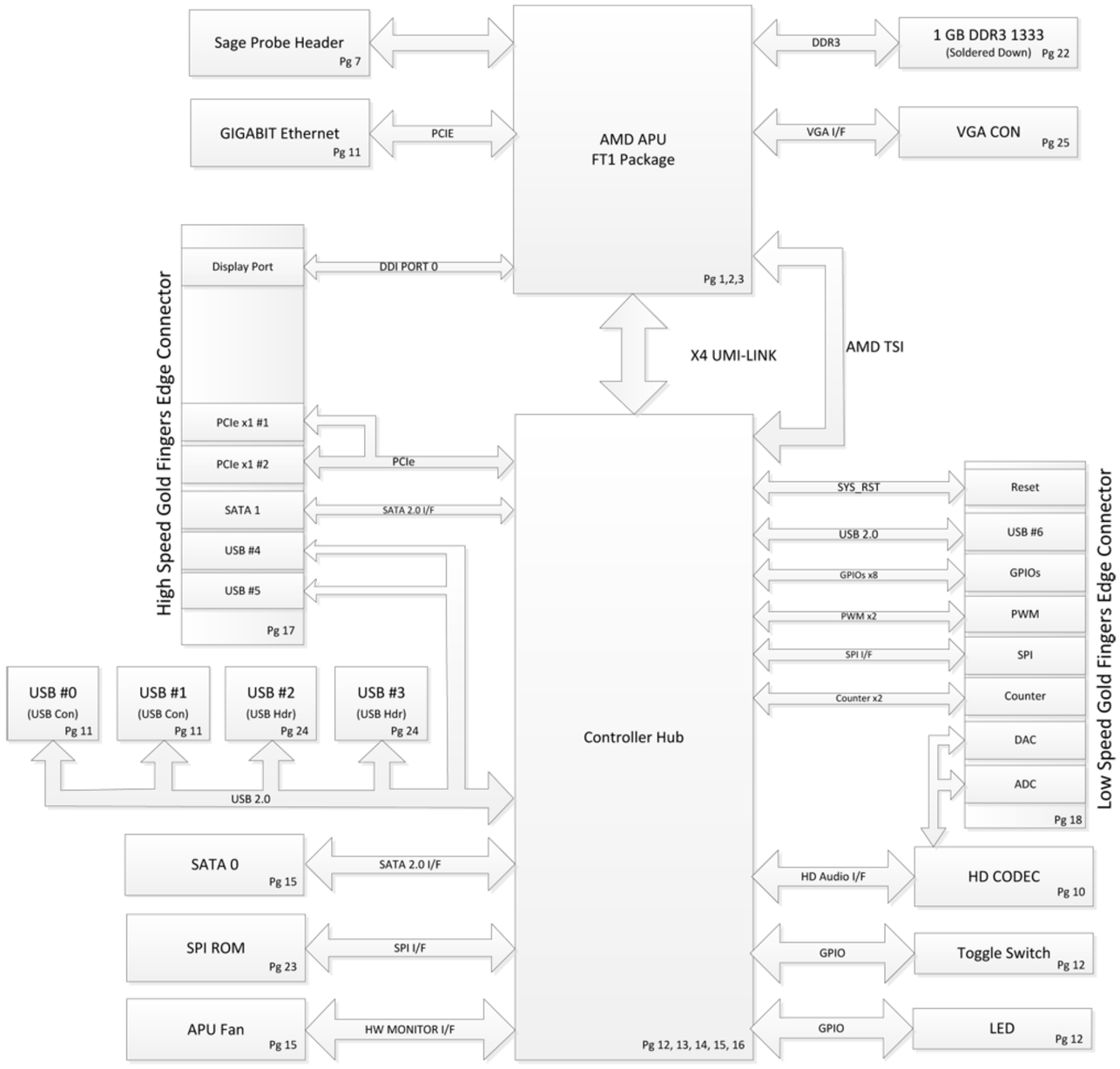
Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5
Drawn by: Victor Navarro	Page Title: COVER PAGE
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
	Date: Thursday, August 08, 2013; Sheet 1 of 23



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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
Drawn by: Victor Navarro	Page Title: BLOCK DIAGRAM	
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DC POWER SUPPLY
9 TO 24VDC

SW REG
+VDDCR_CPU (VAR) @ 10A for T56N and 3.1A for T40E
VDDCR_NB (VAR) @ 8A for T56N and 2.7A for T40E

1.8V_PG
APU_VRM_EN
SLP_S3#
SW REG
+1.0V @ 4.5A
+1.8V@2A
+APU_VDDIO_SUS@4.5A

LINEAR REG
VTT@2A

AMD FT1
VDDCR_CPU
VDDCR_NB
VDDIO_MEM_S
VDD_10
VDD_18
VDD_33

SDRAM SOLDERED DOWN
VDD 1.5V
VTT

1.8V_PG
SWITCH
+1.1V@3A

SLP_S3#
SWITCH
+3.3V@2.5A

ALWAYS_PG
SW REG
+1.1VALW@4.5A
+3.3VALW@3.5A
+5VALW@3.5A

5V
USB

SLP_S3#
SWITCH
+5V@1A

5V
VGA
AUDIO

AMD CONTROLLER HUB
VDDCR_11
VDDAN_11_PCIE
VDDAN_11_SATA
VDDAN_11_CLK
VDDIO_18_FC
VDDPL_33_PCIE
VDDPL_33_SATA
VDDPL_33_SYS
VDDIO_33_PCIGP
VDDCR_11_S
VDDAN_11_USB_S
VDDCR_11_USB_S
VDDPL_11_SYS_S
VDDCR_11_GBE_S
VDDAN_33_USB_S
VDDPL_33_USB_S
VDDIO_33_S
VDDXL_33_S
VDDAN_33_HWM_S
VDDIO_33_GBE_S
VDDIO_GBE_S
VDDIO_AZ_S

GND

DESIGN NOTE:
The power supply currents shown on this page indicate the max currents expected for this design.

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Drawn by: Victor Navarro	Page Title: POWER DISTRIBUTION
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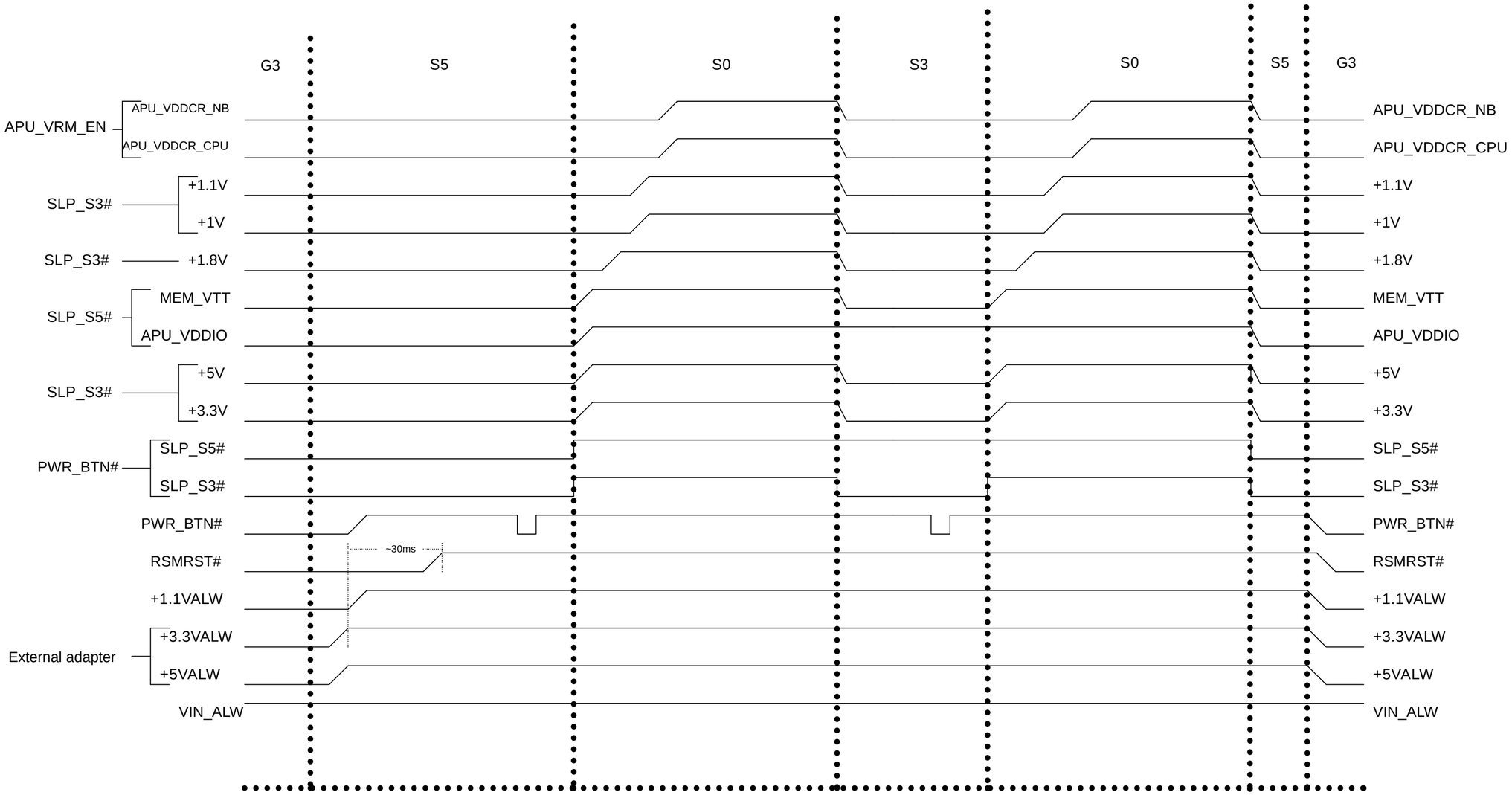

DESIGN NOTE:
While the CH does not have specific power sequence requirements between S0 rails, AMD recommends following the validated sequence defined below. See the following documents for details: AMD FT1 Processor Motherboard Design Guide (PID 45339) & AMD Hudson-1 Motherboard Design Guide (PID 47789)

-- FT1 APU Power Sequence Summary --
Group A - VDD10, VDD18, VDDIO, VDD33
Group B - VDDCR_CPU, VDDCR_NB
Group A ramp before Group B

-- A5x CH Power Sequence Summary --
+3.3VALW ramp before +1.1VALW
+3.3V ramp before +1.8V
1.8V ramp before 1.1V

+3.3VALW: 100us <= Ramp up time <= 40ms. Ramp down time >300us.
All other rails: 50us <= Ramp up time <= 40ms.

DESIGN NOTE:
This diagram outlines system power sequence signals controlled by motherboard circuits only. System reset signals controlled by the APU and CH are not shown here. See the AMD Hudson-1 FCH Datasheets (PID 48879, 47776) for a full timing sequence diagram.

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Approved by: Scott Hoot	Size: C	Document Number: GZMO_8_1_2013 — Rev: I
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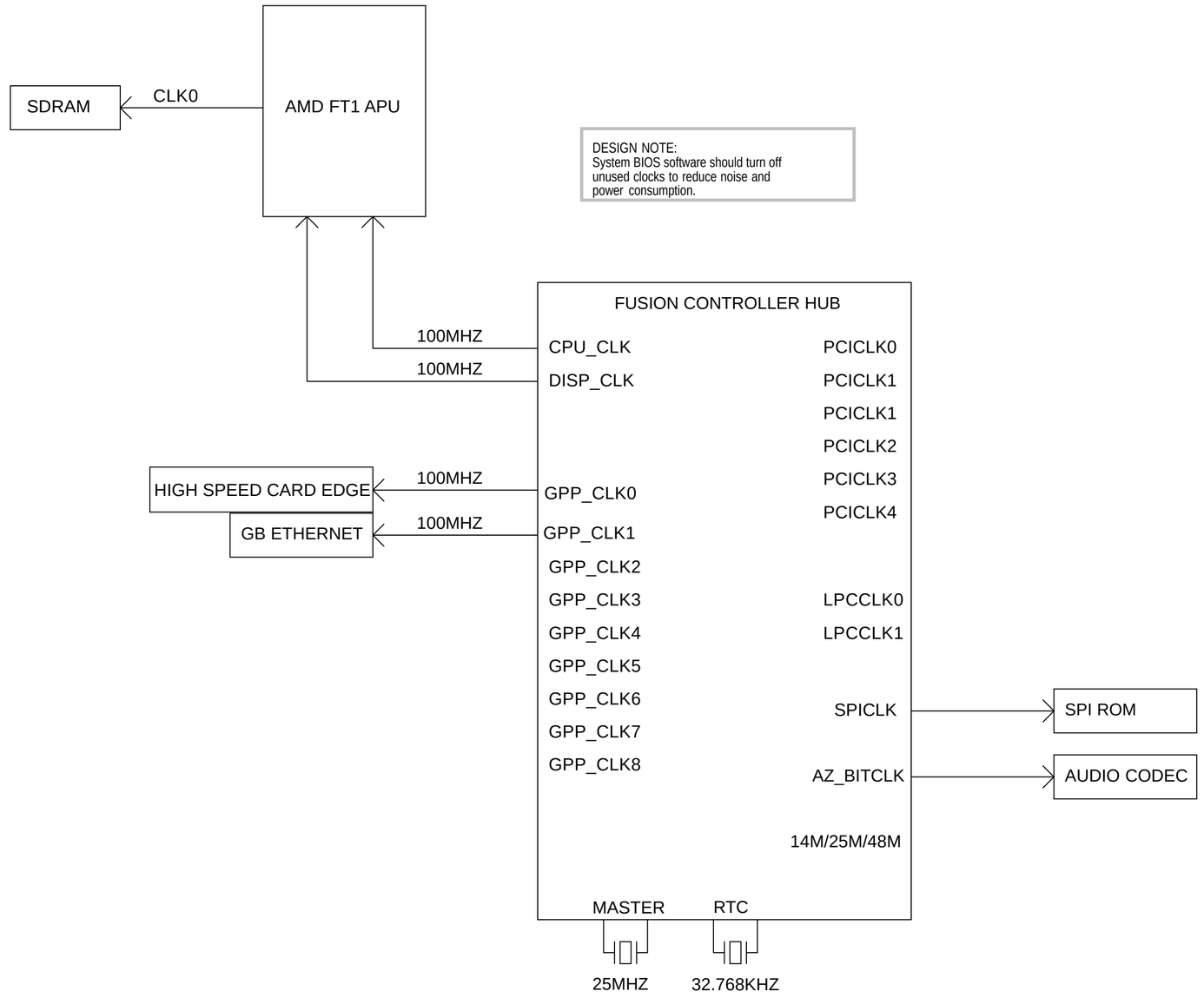

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REVISION HISTORY:

REV	DATE	NOTES
A	AUGUST, 2011	First draft
B	MAY, 2012	ECO-GZM-0001
C	JULY, 2012	ECO-GZM-0002
D	AUGUST, 2012	ECO-GZM-0003
D.2	AUGUST, 2012	ECO-PE12-0004
E	OCTOBER, 2012	ECO-PE12-0015
F	OCTOBER, 2012	ECO-PE12-0018
G	JANUARY, 2013	Updated audio jack and packaged for GizmoSphere release.
H	MARCH, 2013	Corrected coincell pin out. Updated APU_VDDCR_CPU for single phase operation. Updated capcitor selection for unit cost reduction.
I	August, 2013	Corrected AGND and DGND connection issue on U9 and U10 voltage regulators.

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Drawn by: Victor Navarro	Page Title: REVISIONS AND INSTRUCTIONS
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
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+1.8V
R1 1.0K APU_SVC
R2 1.0K APU_SVD
R3 330 LDT_RST#
R4 330 FCH_APU_PWRGD

+3.3V
R6 1.0K FCH_THERMTRIP#
R7 1.0K APU_ALERT#
R8 1.0K PROCHOT#
R9 1.0K APU_SIC
R10 1.0K APU_SID

DESIGN NOTE:
The FT1 processor offers multiple display options from the DDI (Digital Display Interface) ports. See the FT1 processor Motherboard Design Guide (PID 45339) for details. Also, see the FT1 Processor Display Option Schematic (PID 48601) for example circuits.

U1B
ANALOG/DISPLAY/MISC
PART 2 OF 5

DISPLAYPORT1: TDP1_TXP0 (A8), TDP1_TXN0 (B8), TDP1_TXP1 (B9), TDP1_TXN1 (A9), TDP1_TXP2 (D10), TDP1_TXN2 (C10), TDP1_TXP3 (A10), TDP1_TXN3 (B10)
DP MISC: DP_ZVSS (H3) — APUDP_CALR — R5 150; DP_BLON (G2) — LVDS_BLON {17}; DP_DIGON (H2) — LVDS_DIGON {17}; DP_VARY_BL (H1) — LVDS_VARY_BL {17}
DP AUX: TDP1_AUXP (B2), TDP1_AUXN (C2), TDP1_HPD (C1); LTDP0_AUXP (A3) — DP0_AUX_P {17}; LTDP0_AUXN (B3) — DP0_AUX_N {17}; LTDP0_HPD (D3) — DP0_HPD {7}
DISPLAYPORT 0: LTDP0_TXP0 (B5) — {17} DP0_TX0_P; LTDP0_TXN0 (A5) — {17} DP0_TX0_N; LTDP0_TXP1 (D6) — {17} DP0_TX1_P; LTDP0_TXN1 (C6) — {17} DP0_TX1_N; LTDP0_TXP2 (A6) — {17} DP0_TX2_P; LTDP0_TXN2 (B6) — {17} DP0_TX2_N; LTDP0_TXP3 (D8) — {17} DP0_TX3_P; LTDP0_TXN3 (C8) — {17} DP0_TX3_N
CLK: CLKIN_H (V2) — {13} APU_CLK_P; CLKIN_L (V1) — {13} APU_CLK_N; DISP_CLKIN_H (D2) — {13} DISP_CLK_P; DISP_CLKIN_L (D1) — {13} DISP_CLK_N
VGA DAC: DAC_RED (C12) — R11 150 — APU_VGA_R {23}; DAC_REDB (D13); DAC_GREEN (A12) — R12 150 — APU_VGA_G {23}; DAC_GREENB (B12); DAC_BLUE (A13) — R13 150 — APU_VGA_B {23}; DAC_BLUEB (B13); DAC_HSYNC (E1) — APU_HSYNC {23}; DAC_VSYNC (E2) — APU_VSYNC {23}; DAC_SCL (F2) — APU_DAC_SCL {23}; DAC_SDA (D4) — APU_DAC_SDA {23}; DAC_RSET (D12) — R18 499; DAC_ZVSS
SER: SVC (J1) — {20} APU_SVC; SVD (J2) — {20} APU_SVD; SIC (P3) — {12} APU_SIC; SID (P4) — {12} APU_SID
CTRL: RESET_L (T3) — {13} LDT_RST#; PWROK (T4) — {13,20} FCH_APU_PWRGD; PROCHOT_L (U1) — {13,15} PROCHOT#; THERMTRIP_L (U2) — {12} FCH_THERMTRIP#; ALERT_L (T2) — {15} APU_ALERT#
JTAG: TDI (N2) — APU_TDI; TDO (N1) — APU_TDO; TCK (P1) — APU_TCK; TMS (P2) — APU_TMS; TRST_L (M4) — APU_TRST#; DBRDY (M3) — APU_DBRDY; DBREQ_L (M1) — APU_DBREQ#
SENSE: VDDCR_NB_SENSE (F4) — G1; VDDCR_CPU_SENSE (G1) — APU_VDDIO_FB — F3 — {19} APU_VDDIO_FB; VDDIO_MEM_S_SENSE; VSS_SENSE (F1); RSVD_1 (B4), RSVD_2 (W11), RSVD_3 (V5)
TEST: TEST4 R1 TP1; TEST5 R2 TP2; TEST6 R6; TEST14 T5 TP3; TEST15 E4 TP4; TEST16 K4 TP5; TEST17 L1 TP6; TEST18 L2 FT1_TEST18; TEST19 M2 FT1_TEST19; TEST25_H K1 FT1_TEST25_P TP7; TEST25_L K2 FT1_TEST25_N TP8; TEST28_H L5 TP9; TEST28_L M5 TP10; TEST31 M21 TP11; TEST33_H J18 FT1_TEST33_P; TEST33_L J19 FT1_TEST33_N; TEST34_H U15 TP12; TEST34_L T15 TP13; TEST35 H4 FT1_TEST35; TEST36 N5 FT1_TEST36 TP14; TEST37 R5 TP15; TEST38 K3 — DMAACTIVE_L T1 — R24 1.0K — +1.8V — ALLOW_LDTSTP {13}
GET40EFSB22GVE

+1.8V
FT1_TEST25_N R14 510
FT1_TEST36 R15 1.0K
FT1_TEST35 R16 1.0K
FT1_TEST18 R17 1.0K
FT1_TEST19 R19 1.0K
FT1_TEST25_P R20 510
FT1_TEST35 R21 1.0K
DNP

FT1_TEST33_P C1 0.1uF R22 51
FT1_TEST33_N C2 0.1uF R23 51

VSS_SENSE — S1 SHORT_NL — VDDCCR_APU_FB_L {20}; VDDCCR_APU_FB_H {20}; TP16
VSS_SENSE — S2 SHORT_NL — VDDCR_NB_FB_L {20}; VDDCR_NB_FB_H {20}; TP17

LAYOUT NOTE:
Voltage feedback pairs should be routed differentially. See the AMD FT1 Processor Motherboard Design Guide (PID 45339) for details.

LAYOUT NOTE:
Place these test points near APU.

DESIGN NOTE:
All new embedded designs should implement the "AMD Embedded Probe Header" defined here instead of the previous "HDT" header. Embedded designs should ignore any schematic checklist requirements for the "HDT" header.

AMD EMBEDDED PROBE HEADER

+1.8V — R25 1.0K — R26 330
+1.8V — R27 1.0K — R28 1.0K — R29 1.0K
J1 (62001621121)
1 APU_DBRDY
3
5
7
9 APU_DBREQ#
11 LDT_RST#
13
15 APU_TRST#
2 APU_TDO
4 APU_TDI
6 APU_TMS
8 APU_TCK
10 PWR_BTN# {12}
12 SYS_RST# {12,18}
14 SCL1 {12,19}
16 SDA1 {12,19}

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Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
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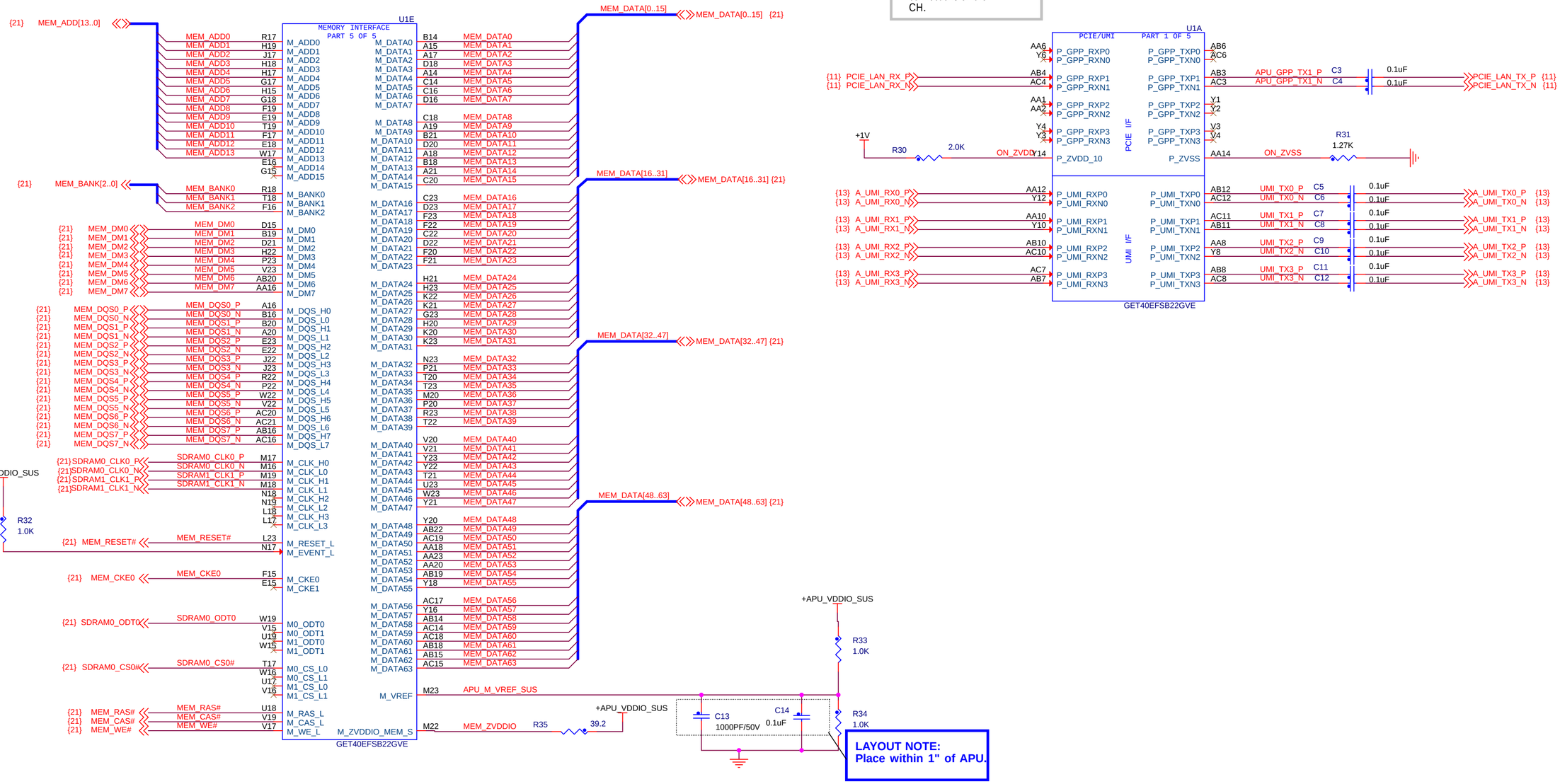

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Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
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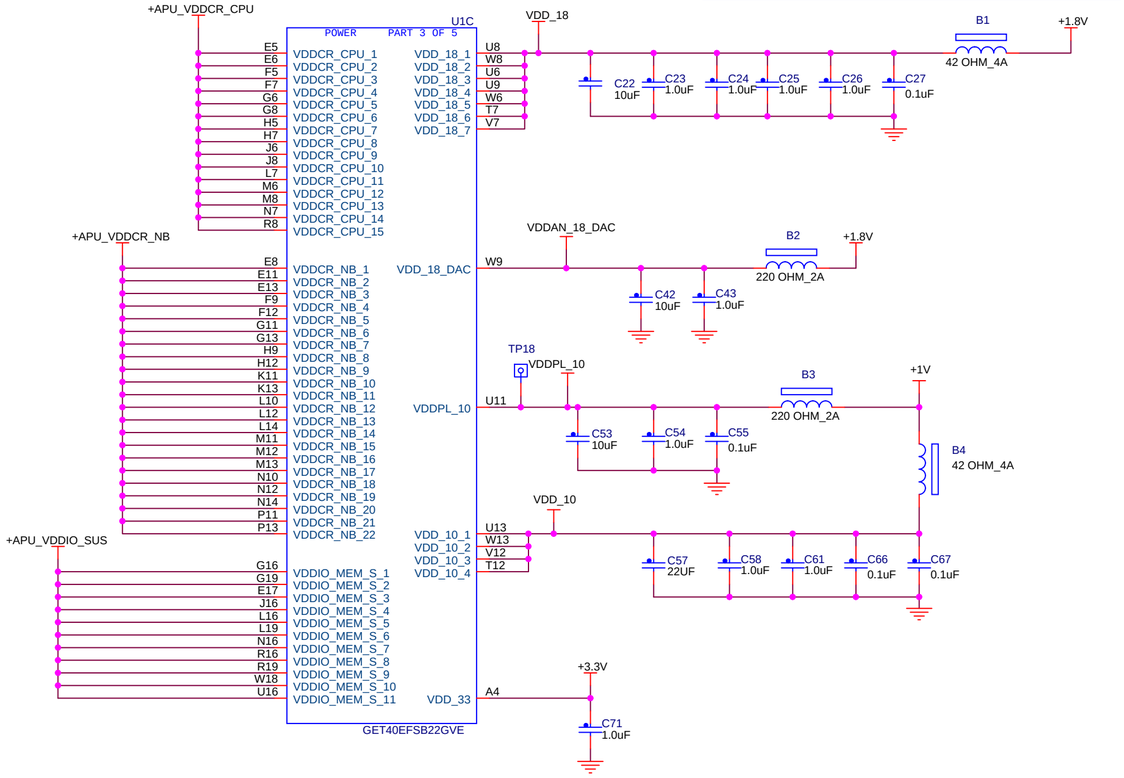
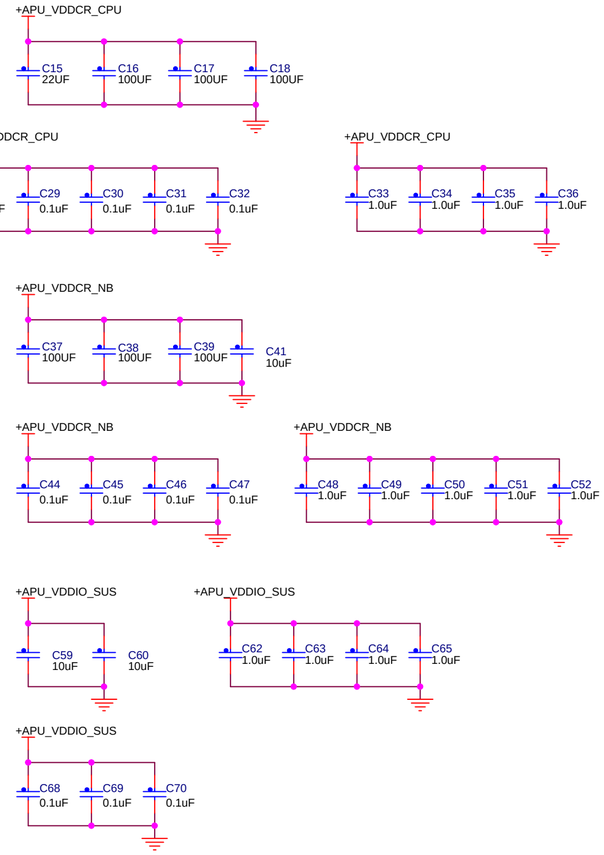
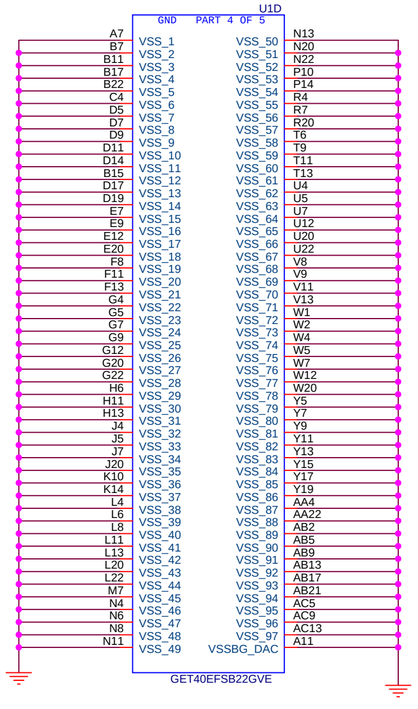
LAYOUT NOTE:
See the AMD FT1 Processor Motherboard Design Guide (PID 45339) for specific details on APU decoupling components and placement.

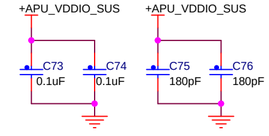




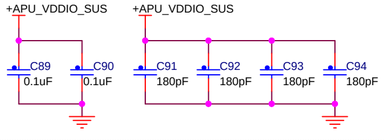


H1
HEATSINK_APU

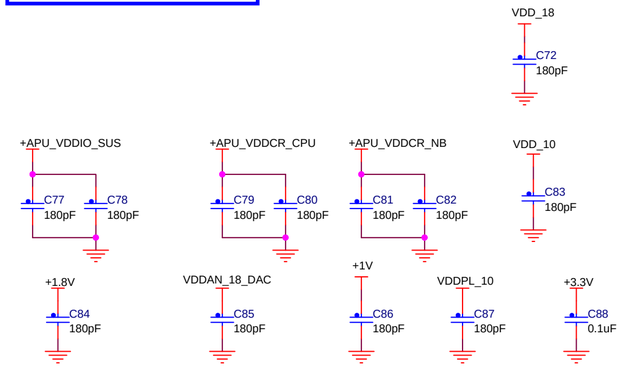
LAYOUT NOTE:
Additional capacitors are evenly spaced along VDDIO_MEM_S & VSS plane split between processor and first DIMM, if plane split is longer than 63.5 mm.
Note: not required if plane split was not implemented.



LAYOUT NOTE:
Capacitors are evenly spaced along VDDIO_MEM_S & VSS plane split bewteen processor and first DIMM.
Note: not required if plane split was not implemented.



LAYOUT NOTE:
Place EMC caps under APU.



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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
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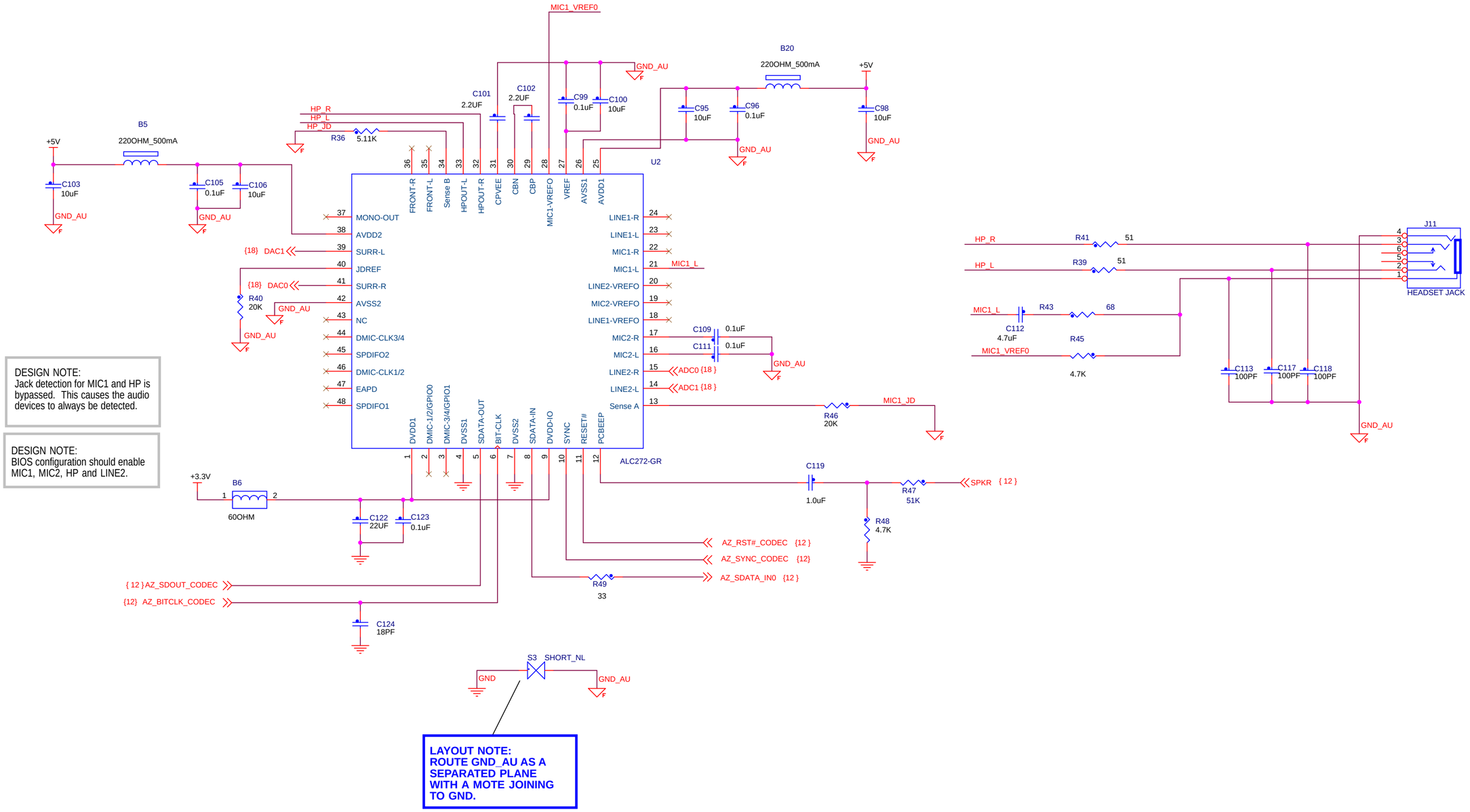

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LAYOUT NOTE:
Place caps within 200mils of IC.
Make this power trace wider than 40 mills.

+3.3VALW
C125 22UF
C126 0.1uF

DVDD12
C127 0.1uF
C128 0.1uF
C129 0.1uF
S4 SHORT_NL

EVDD12
C133 0.1uF
C134 0.1uF
S5 SHORT_NL

AVDD12
C135 0.1uF
C136 0.1uF
C137 0.1uF
C138 22UF

L2 4.7UH/2A
R50 2.49K
RSET

+3.3VALW
C130 0.1uF
C131 0.1uF
C132 0.1uF

+3.3VALW
R51 4.7K
EEDI

+3.3VALW
R52 150
R53 150
R54 150
EEDO
EEDI
LED0

C142 4.7uF
C143 1.0UF
C144 0.01UF
AVDD12

J2
LED1+ 21
LED1- 22
LED2+ 19
LED2- 20
CT 18
GND1 23
GND2 24
GND3 29
GND4 30
VCT 9
D1+ 10 MDI0+
D1- 11 MDI0-
D2+ 12 MDI1+
D2- 13 MDI1-
D3+ 14 MDI2+
D3- 15 MDI2-
D4+ 16 MDI3+
D4- 17 MDI3-
ETHERNET

C148 0.01UF

+5V_FUSE_USB_3_4
USB1
VCC 1
DATA1- 2 SBD3-
DATA1+ 3 SBD3+
GND 4
USBN3 {12}
744231091 T1
USBP3 {12}
USBN0 {12}
USB2
GND5 25
GND6 26
GND7 27
GND8 28
_VCC 5
_DATA1- 6 SBD0-
_DATA1+ 7 SBD0+
_GND 8
744231091 T2
USBP0 {12}
USB_TYPE_A_DUAL

U4
AVDD33 1
MDIP0 2
MDIN0 3
NC/FB12 4
MDIP1 5
MDIN1 6
GND1 7
NC/MDIP2 8
NC/MDIN2 9
DVDD12/AVDD12 10
NC/MDIP3 11
NC/MDIN3 12
VCTRL12A/SROUT12 48
GND4 47
RSET 46
VCTRL12DVDDSR 45
NC/VDDSR 44
NC/ENSWREG 43
CKTAL2 42
CKTAL1 41
NC/AVDD33 40
NC/LV_PLL 39
LED0 38
VDD33_2 37
DVDD12_1 13
GND2 14
HSIP 15
HSIN 16
REFCLK_P 17
REFCLK_N 18
VDDTXEVDD12 19
HSOP 20
HSON 21
EGND 22
NC/GPO 23
NC/NC 24
RTL8111DL-VB-GR

+3.3VALW
C149 0.1uF
C150 0.1uF
AVDD12

C151 0.1uF
DVDD12

{8} PCIE_LAN_TX_P
{8} PCIE_LAN_TX_N
{13} PCIE_LAN_CLK_P
{13} PCIE_LAN_CLK_N
EVDD12

C152 0.1uF
{8} PCIE_LAN_RX_P
HSOP

C153 0.1uF
{8} PCIE_LAN_RX_N
HSON

Y1
C140 10PF
25MHz
C145 10PF

DVDD12_3 36
LED1/EESK 35
LED2/EEDI 34
LED3/EEDO 33
EECS 32
GND3 31
DVDD12_2 30
VDD33_1 29
ISOLATEB 28
PERSTB 27
LANWAKEB 26
CLKREQB 25

DVDD12
EEDI
C146 0.1uF
C147 0.1uF
ISOLATEB
APU_PCIE_RST# {13}
PCIE_WAKE_UP# {12}
PCIE_LAN_CLKREQ# {12}

+3.3VALW
+3.3V
R55 1.0K
R56 15K

+5VALW
F1
0805L110SLYR
1.1A/6V
+5V_FUSE_USB_3_4
C389 100UF
C358 10uF
C360 10uF

+5V_FUSE_USB_3_4
C154 0.1uF
GND

U5
SBD3- 6
SBD3+ 4
SBD0- 3
SBD0+ 1
5
2
RCLAMP0504S.TCT

LAYOUT NOTE:
Place ESD protection diodes directly on signal traces to eliminate stubs.

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DESIGN NOTE:
BIOS must disable the internal pullup on THRMTRIP_L pin of the FCH to prevent leakage when the APU is powered down.

DESIGN NOTE:
The RC delay calculation for RSMRST# must include the CH integrated 10K pull-up to 3.3VALW.

DESIGN NOTE:
The integrated MAC function is not supported in all CH variants.
See the appropriate device databook for detailed feature support.

DESIGN NOTE:
BIOS software must program the unused CH GPIOs as outputs or enable internal pull-ups. Otherwise, external termination may be required. See the Hudson-1 FCH Schematic Checklist (PID 47791) for detailed termination requirements.

DESIGN NOTE:
Do not use pull-up resistors when the CH controls the system power supply.

U6A
FCH
PART 1 OF 5
100-CG2293

J2 PCI_PME_L_GEVENT4_L
K1 RI_L_GEVENT22_L
{18}SPI_CS3 D3 SPI_CS3_L_GBE_STAT1_GEVENT21_L
{19} SLP_S3# F1 SLP_S3_L
{19} SLP_S5# H1 SLP_S5_L
PWR_BTN# F2 PWR_BTN_L
{20} SB_PWR_GD H5 PWR_GOOD
G6 SUS_STAT_L
TP19 FCH_TEST0 B3 TEST0
TP20 FCH_TEST1 C4 TEST1_TMS
TP21 FCH_TEST2 F6 TEST2
{18} GEVENT0 AD21 GA20IN_GEVENT0_L
AE21 KBRST_L_GEVENT1_L
K2 LPC_PME_L_GEVENT3_L
J29 LPC_SMI_L_GEVENT23_L
{18} GEVENT5 H2 GEVENT5_L
{7, 18} SYS_RST# SYS_RST# J1 SYS_RESET_L_GEVENT19_L
{11} PCIE_WAKE_UP# H6 WAKE_L_GEVENT8_L
F3 IR_RX1_GEVENT20_L
{7} FCH_THERMTRIP# J6 THRMTRIP_L_SMBALERT_L_GEVENT2_L
NB_PWRGD AC19 NB_PWRGD
RSMRST# G1 RSMRST_L

AD19 CLK_REQ4_L_SATA_IS0_L_GPIO64
{18} AD19_GPIO64
{18} AA16_GPIO63 AA16 CLK_REQ3_L_SATA_IS1_L_GPIO63
AB21 SMARTVOLT1_SATA_IS2_L_GPIO50
{18} AC18_GPIO60 AC18 CLK_REQ0_L_SATA_IS3_L_GPIO60
{18} AF20_GPIO55 AF20 SATA_IS4_L_FANOUT3_GPIO55
{18} AE19_GPIO59 AE19 SATA_IS5_L_FANIN3_GPIO59
{10} SPKR AF19 SPKR_GPIO66
{18} AD22_SCL0 AD22 SCL0_GPIO43
{18} AE22_SDA0 AE22 SDA0_GPIO47
{7,19} SCL1 F5 SCL1_GPIO227
{7,19} SDA1 F4 SDA1_GPIO228
{11} PCIE_LAN_CLKREQ# AH21 CLK_REQ2_L_FANIN4_GPIO62
{18} AB18_GPIO61 AB18 CLK_REQ1_L_FANOUT4_GPIO61
TOGGLE_GPIO1 E1 IR_LED_L_LLB_L_GPIO184
AJ21 SMARTVOLT2_SHUTDOWN_L_GPIO51
H4 DDR3_RST_L_GEVENT7_L
LED_ON D5 GBE_LED0_GPIO183
D7 GBE_LED1_GEVENT9_L
G5 GBE_LED2_GEVENT10_L
K3 GBE_STAT0_GEVENT11_L
AA20 CLK_REQG_L_GPIO65_OSCIN
GPIO

H3 BLINK_USB_OC7_L_GEVENT18_L
D1 USB_OC6_L_IR_TX1_GEVENT6_L
E4 USB_OC5_L_IR_TX0_GEVENT17_L
D4 USB_OC4_L_IR_RX0_GEVENT16_L
E8 USB_OC3_L_AC_PRES_TDO_GEVENT15_L
F7 USB_OC2_L_TCK_GEVENT14_L
E7 USB_OC1_L_TDI_GEVENT13_L
F8 USB_OC0_L_TRST_L_GEVENT12_L
USB OC

HD AUDIO
{10} AZ_BITCLK_CODEC R58 33 AZ_BITCLK M3 AZ_BITCLK
{10} AZ_SDOUT_CODEC R60 33 N1 AZ_SDOUT
{16} AZ_SDATA_OUT L2 AZ_SDIN0_GPIO167
{10} AZ_SDATA_IN0 AZ_SDATA_IN0 M2 AZ_SDIN1_GPIO168
M1 AZ_SDIN2_GPIO169
M4 AZ_SDIN3_GPIO170
{10} AZ_SYNC_CODEC R62 33 AZ_SYNC N2 AZ_SYNC
{10} AZ_RST#_CODEC R63 33 AZ_RST# P2 AZ_RST_L

GBE_COL T1 GBE_COL
GBE_CRS T4 GBE_CRS
GBE_MDIO L6 GBE_MDCK
L5 GBE_MDIO
T9 GBE_RXCLK
U1 GBE_RXD3
U3 GBE_RXD2
T2 GBE_RXD1
U2 GBE_RXD0
GBE_RXERR T5 GBE_RXCTL_RXDV
V5 GBE_RXERR
P5 GBE_TXCLK
M5 GBE_TXD3
P9 GBE_TXD2
T7 GBE_TXD1
P7 GBE_TXD0
M7 GBE_TXCTL_TXEN
P4 GBE_PHY_PD
M9 GBE_PHY_RST_L
GBE_PHY_INTR V7 GBE_PHY_INTR
GBE LAN

TP22 E23 PS2_DAT_SDA4_GPIO187
TP23 E24 PS2_CLK_SCL4_GPIO188
F21 SPI_CS2_L_GBE_STAT2_GPIO166
G29 FC_RST_L_GPO160
PS2

D27 PS2KB_DAT_GPIO189
F28 PS2KB_CLK_GPIO190
F29 PS2M_DAT_GPIO191
E27 PS2M_CLK_GPIO192

USB MISC
USBCLK_14M_25M_48M_OSC A10
USB_RCOMP G19 USB_RCOMP
R57 11.8K

USB 1.1
J10 USB_FSD1P_GPIO186
H11 USB_FSD1N
H9 USB_FSD0P_GPIO185
J8 USB_FSD0N

USB 2.0
B12 USB_HSD13P
A12 USB_HSD13N
F11 USB_HSD12P
E11 USB_HSD12N
E14 USB_HSD11P
E12 USB_HSD11N
J12 USB_HSD10P
J14 USB_HSD10N
A13 USB_HSD9P
B13 USB_HSD9N
D13 USB_HSD8P
C13 USB_HSD8N
G12 USB_HSD7P
G14 USB_HSD7N
G16 USB_HSD6P → USBP6 {22}
G18 USB_HSD6N → USBN6 {22}
D16 USB_HSD5P → USBP5 {22}
C16 USB_HSD5N → USBN5 {22}
B14 USB_HSD4P → USBP4 {18}
A14 USB_HSD4N → USBN4 {18}
E18 USB_HSD3P → USBP3 {11}
E16 USB_HSD3N → USBN3 {11}
J16 USB_HSD2P → USBP2 {17}
J18 USB_HSD2N → USBN2 {17}
B17 USB_HSD1P → USBP1 {17}
A17 USB_HSD1N → USBN1 {17}
A16 USB_HSD0P → USBP0 {11}
B16 USB_HSD0N → USBN0 {11}

EMBEDDED CTRL
SCL2_GPIO193 D25 R197 10.0K
SDA2_GPIO194 F23 R198 10.0K
SCL3_LV_GPIO195 B26 → APU_SIC {7}
SDA3_LV_GPIO196 E26 → APU_SID {7}
EC_PWM0_EC_TIMER0_GPIO197 F25
EC_PWM1_EC_TIMER1_GPIO198 E22
EC_PWM2_EC_TIMER2_GPIO199 F22 → FCH_GPIO199 {16}
EC_PWM3_EC_TIMER3_GPIO200 E21 → FCH_GPIO200 {16}
KSI_0_GPIO201 G24
KSI_1_GPIO202 G25
KSI_2_GPIO203 E28
KSI_3_GPIO204 E29
KSI_4_GPIO205 D29
KSI_5_GPIO206 D28
KSI_6_GPIO207 C29
KSI_7_GPIO208 C28
KSO_0_GPIO209 B28
KSO_1_GPIO210 A27
KSO_2_GPIO211 B27
KSO_3_GPIO212 D26
KSO_4_GPIO213 A26
KSO_5_GPIO214 C26
KSO_6_GPIO215 A24
KSO_7_GPIO216 B25
KSO_8_GPIO217 A25
KSO_9_GPIO218 D24
KSO_10_GPIO219 B24
KSO_11_GPIO220 C24
KSO_12_GPIO221 B23
KSO_13_GPIO222 A23
KSO_14_GPIO223 D22
KSO_15_GPIO224 C22
KSO_16_GPIO225 A22
KSO_17_GPIO226 B22

{19} ALWAYS_PG 0 R59 RSMRST#

+3.3VALW
R64 4.7K SCL1
R65 4.7K SDA1
R66 10.0K GBE_MDIO
R75 1.0K TOGGLE_GPIO1

+3.3V
R200 2.2K AD22_SCL0
R199 2.2K AE22_SDA0
R68 10.0K NB_PWRGD

R69 10.0K GBE_PHY_INTR
R70 10.0K GBE_COL
R71 10.0K GBE_CRS
R72 10.0K GBE_RXERR

+3.3VALW
R74 220
D1 LTST-C190KSKT
VF=2.1
I=5mA
YLW
ON
LED_ON

+3.3VALW
R73 1.0K DNP
PWR_BTN# {7}
C156 0.1uF
SW2 B3U-1000P
POWER SWITCH

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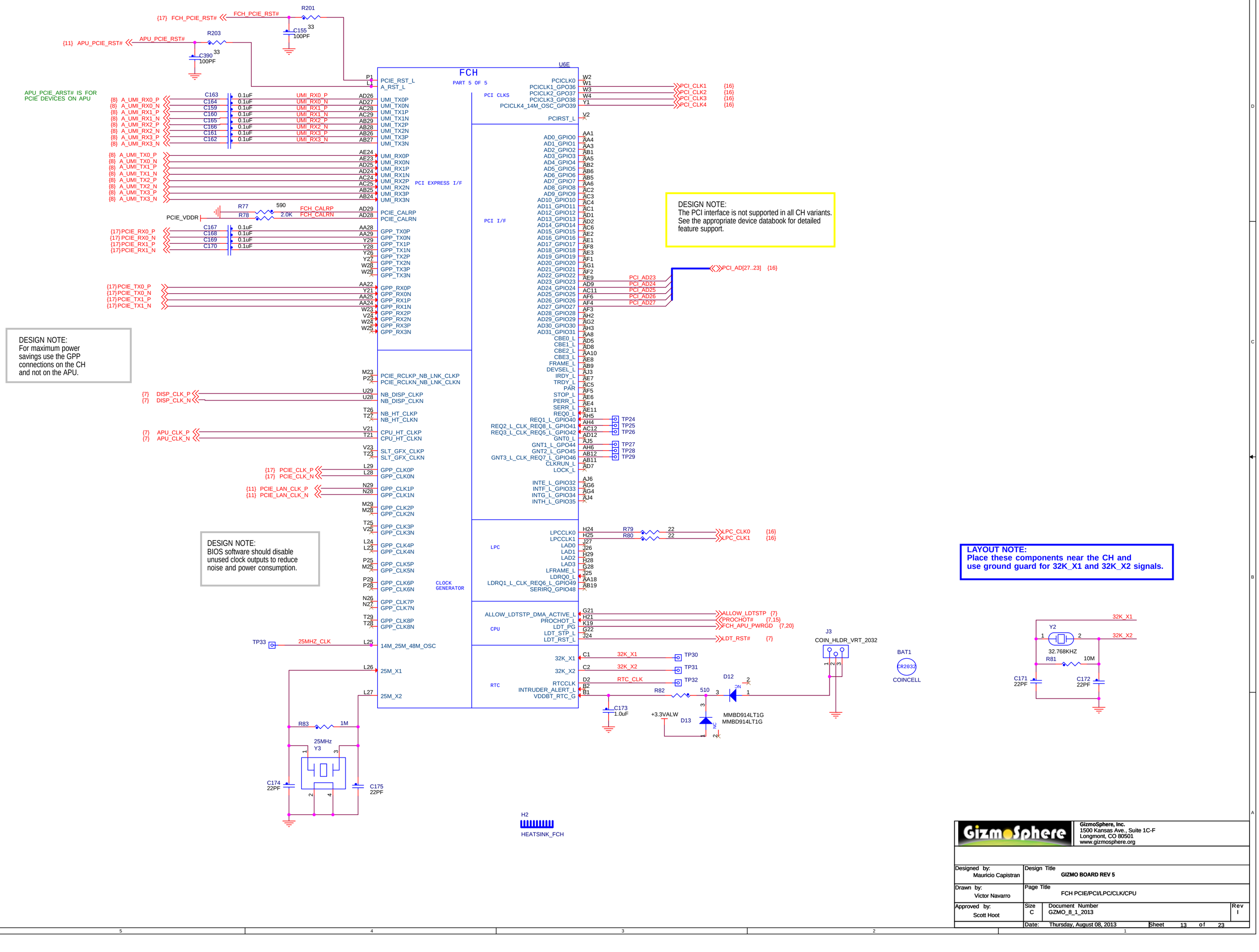
Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
Drawn by: Victor Navarro	Page Title: FCH ACPI/USB/AUD/GPIO	
Approved by: Scott Hoot	Size: C	Document Number: GZMO_8_1_2013 Rev: I
	Date: Thursday, August 08, 2013	Sheet 12 of 23



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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
Drawn by: Victor Navarro	Page Title: FCH PCIE/PCI/LPC/CLK/CPU	
Approved by: Scott Hoot	Size: C	Document Number: GZMO_8_1_2013 Rev: I
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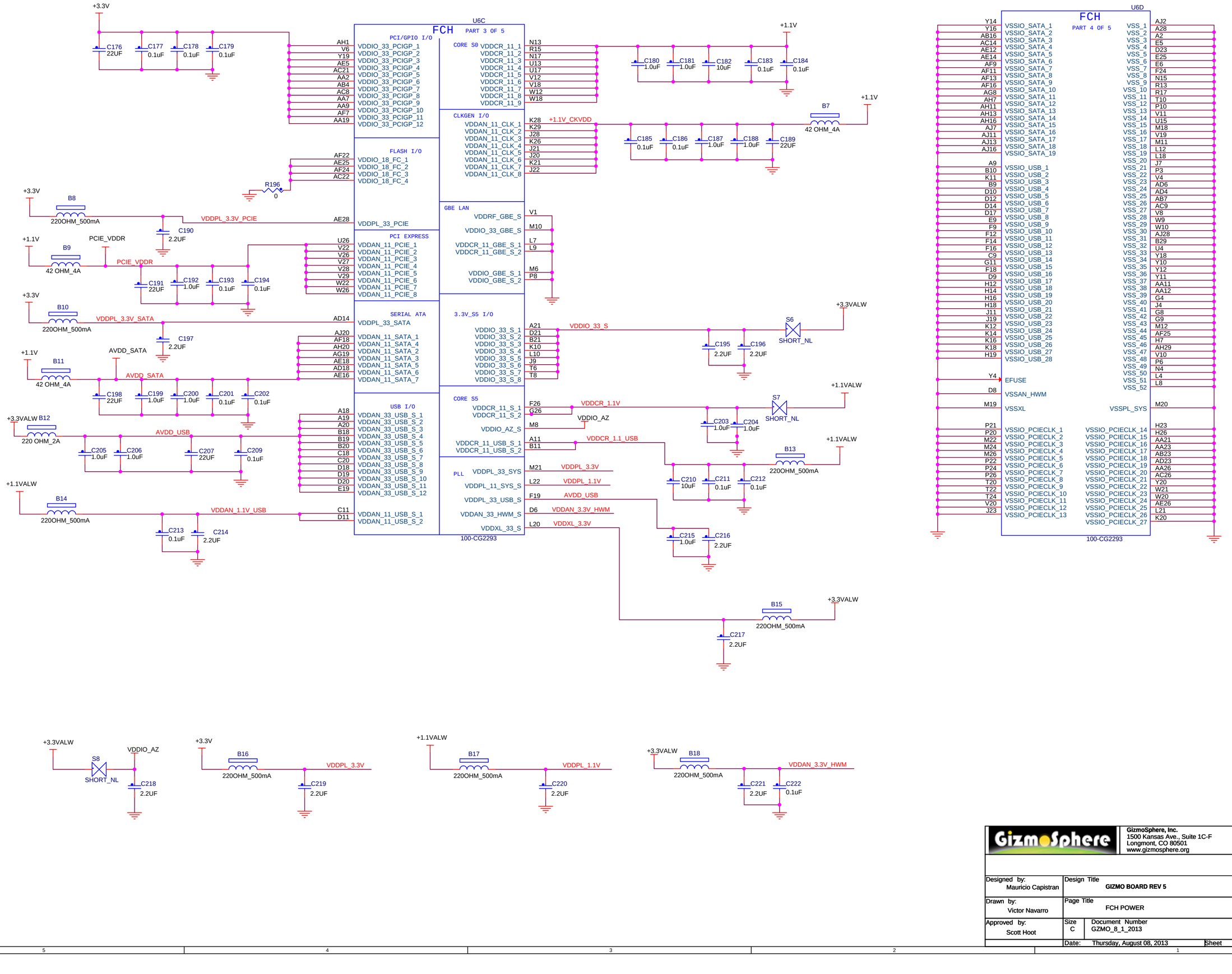
LAYOUT NOTE:
Place all power decoupling caps as close to the CH as possible.



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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5
Drawn by: Victor Navarro	Page Title: FCH POWER
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
	Date: Thursday, August 08, 2013; Sheet 14 of 23

LAYOUT NOTE:
AMD recommends limiting SATA traces to only 1 via. See the Hudson-1 Motherboard Design Guide (PID 47789) for details.

SATA POWER

J4 — 471554001

{17} SATA_C_TX0_P	SATA_C_TX0_P	C223 0.01UF	SATA_TX0_P
{17} SATA_C_TX0_N	SATA_C_TX0_N	C224 0.01UF	SATA_TX0_N
{17} SATA_C_RX0_N	SATA_C_RX0_N	C225 0.01UF	SATA_RX0_N
{17} SATA_C_RX0_P	SATA_C_RX0_P	C226 0.01UF	SATA_RX0_P
	SATA_C_TX1_P	C227 0.01UF	SATA_TX1_P
	SATA_C_TX1_N	C228 0.01UF	SATA_TX1_N
	SATA_C_RX1_N	C229 0.01UF	SATA_RX1_N
	SATA_C_RX1_P	C230 0.01UF	SATA_RX1_P

J4: TX+ (2), TX- (3), RX- (5), RX+ (6), GND (1), GND#4 (4), GND#7 (7), pins 8 and 9 unused

+5V — F8 0805L110SLYR 1.1A/6V

J5 — 171825-4

C231 10uF, C354 100UF

HOUSING P/N: 171822-4
CRIMP AWG 20-26 P/N:170262-4

LAYOUT NOTE:
Keep SATA calibration nets very short.

AVDD_SATA — R84 931, R85 1.0K — SATA_CALP, SATA_CALN

R195 10.0K

FCH

U6B — PART 2 OF 5

SATA_TX0P	AH9	SATA_TX0_P
SATA_TX0N	AJ9	SATA_TX0_N
SATA_RX0N	AJ8	SATA_RX0_N
SATA_RX0P	AH8	SATA_RX0_P
SATA_TX1P	AH10	SATA_TX1_P
SATA_TX1N	AJ10	SATA_TX1_N
SATA_RX1N	AG10	SATA_RX1_N
SATA_RX1P	AF10	SATA_RX1_P
SATA_TX2P	AG12	
SATA_TX2N	AF12	
SATA_RX2N	AJ12	
SATA_RX2P	AH12	
SATA_TX3P	AH14	
SATA_TX3N	AJ14	
SATA_RX3N	AG14	
SATA_RX3P	AF14	
SATA_TX4P	AG17	
SATA_TX4N	AF17	
SATA_RX4N	AJ17	
SATA_RX4P	AH17	
SATA_TX5P	AJ18	
SATA_TX5N	AH18	
SATA_RX5N	AH19	
SATA_RX5P	AJ19	
SATA_CALRP	AB14	SATA_CALP
SATA_CALRN	AA14	SATA_CALN
SATA_ACT_L_GPIO67	AD11	
SATA_X1	AD16	
SATA_X2	AC16	

SERIAL ATA

SPI ROM

{18} SPI_DATAIN	SPI_DATAIN	J5
{18} SPI_DATAOUT	SPI_DATAOUT	E2
{18} SPI_CLK	SPI_CLK	K4
	SPI_CS#	K9
	RESET#	G2
SPI_DI_GPIO164		
SPI_DO_GPIO163		
SPI_CLK_GPIO162		
SPI_CS1_L_GPIO165		
ROM_RST_L_GPIO161		

R194 0 DNP

NC1, NC2 — G27, Y2

100-CG2293

GPIOD

FC_CLK	AH28
FC_FBCLKOUT	AG28
FC_FBCLKIN	AF26
FC_OE_L_GPIOD145	AF28
FC_AVD_L_GPIOD146	AG29
FC_WE_L_GPIOD148	AG26
FC_CE1_L_GPIOD149	AF27
FC_CE2_L_GPIOD150	AE29
FC_INT1_GPIOD144	AF29
FC_INT2_GPIOD147	AH27
FC_ADQ0_GPIOD128	AJ27
FC_ADQ1_GPIOD129	AJ26
FC_ADQ2_GPIOD130	AH25
FC_ADQ3_GPIOD131	AH24
FC_ADQ4_GPIOD132	AG23
FC_ADQ5_GPIOD133	AH23
FC_ADQ6_GPIOD134	AJ22
FC_ADQ7_GPIOD135	AG21
FC_ADQ8_GPIOD136	AF21
FC_ADQ9_GPIOD137	AH22
FC_ADQ10_GPIOD138	AJ23
FC_ADQ11_GPIOD139	AF23
FC_ADQ12_GPIOD140	AJ24
FC_ADQ13_GPIOD141	AJ25
FC_ADQ14_GPIOD142	AG25
FC_ADQ15_GPIOD143	AH26

HW MONITOR

FANOUT0_GPIO52	W5	FCH_FANOUT0
FANOUT1_GPIO53	W6	PWM1(FANOUT1) {18}
FANOUT2_GPIO54	Y9	PWM2(FANOUT2) {18}
FANIN0_GPIO56	W7	
FANIN1_GPIO57	V9	COUNTER1(FANIN1) {18}
FANIN2_GPIO58	W8	COUNTER2(FANIN2) {18}
TEMPIN0_GPIO171	B6	TEMPIN0
TEMPIN1_GPIO172	A6	TEMPIN1
TEMPIN2_GPIO173	A5	TEMPIN2
TEMPIN3_TALERT_L_GPIO174	B5	APU_ALERT# {7}
TEMP_COMM	C7	
VIN0_GPIO175	A3	FCH_VIN0
VIN1_GPIO176	B4	FCH_VIN1
VIN2_GPIO177	A4	FCH_VIN2
VIN3_GPIO178	C5	FCH_VIN3
VIN4_GPIO179	A7	FCH_VIN4
VIN5_GPIO180	B7	FCH_VIN5
VIN6_GBE_STAT3_GPIO181	B8	FCH_VIN6
VIN7_GBE_LED3_GPIO182	A8	FCH_VIN7

DESIGN NOTE:
The HWM features (TEMPIN, VIN) are not supported, but these pins may still be used for GPIO functions.

TEMPIN0 — RN1A 1 — 8 10K
TEMPIN1 — RN1B 2 — 7 10K
TEMPIN2 — RN1C 3 — 6 10K
FCH_VIN0 — RN1D 4 — 5 10K
FCH_VIN1 — RN2A 1 — 8 10K
FCH_VIN2 — RN2B 2 — 7 10K
FCH_VIN3 — RN2C 3 — 6 10K
FCH_VIN4 — RN2D 4 — 5 10K
FCH_VIN5 — RN3A 1 — 8 10K
FCH_VIN6 — RN3B 2 — 7 10K
FCH_VIN7 — RN3C 3 — 6 10K

ROM

+3.3VALW — R88 10.0K, R87 1.0K

U7 — W25Q16CVSSIG

SPI_CS#	1	/CS	VCC 8
SPI_DATAIN	2	DO	/HOLD 7 RESET#
	3	/WP	CLK 6 SPI_CLK
GND	4	GND	DIO 5 SPI_DATAOUT

R89 10.0K, C234 0.1uF — GND

LAYOUT NOTE:
CHECK FOR THE SOIC8 FOOTPRINT

MEM Decoupling Caps

+3.3VALW — C232 1.0UF, C233 0.1uF — GND

APU or System Fan

LAYOUT NOTE:
The FANTACH signal was removed to save space in Layout

+5V — R86 1.0K

R90 10.0K — PMBT4403,215 Q1 — +5V

FCH_FANOUT0 — R91 100 — Q2 MMBT3904LT1G

R92 10.0K

D2 ZHCS350TA

R93 10.0K

{7,13} PROCHOT# — R94 20K

22uF may not be enogh.
Verify if 100uF capacitor
footprint is compatible

C391 22UF

J6 — DF13-2P-1.25DSA
FEMALE HOUSING P/N: DF13-2S-1.25C
CRIMP P/N: DF13-2630SCF
FAN P/N: MB40100V2-000U-A99

V+	RED
G	BLACK

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Drawn by: Victor Navarro	Page Title: FCH SATA/SPI/HWM/GPIOD
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
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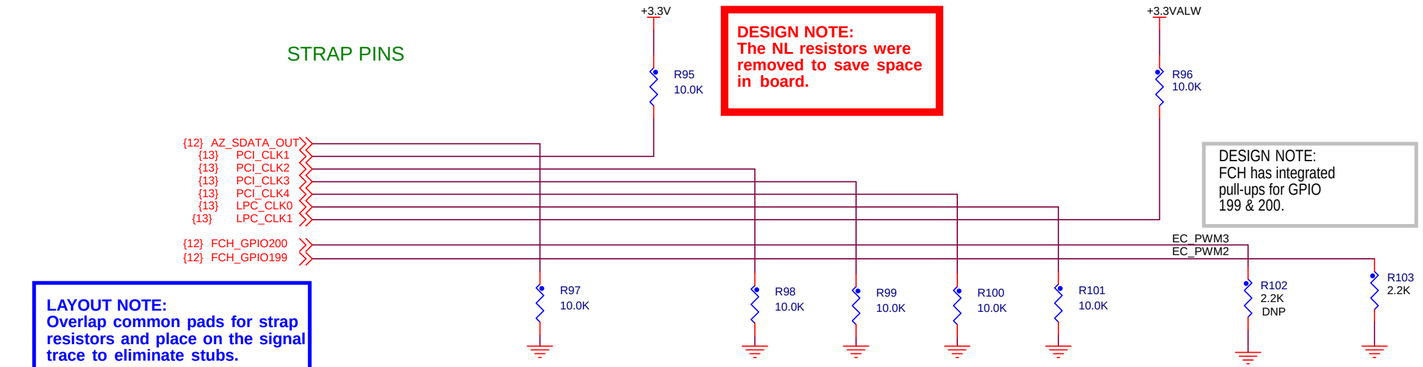
STRAP PINS



DESIGN NOTE:
The NL resistors were removed to save space in board.

DESIGN NOTE:
FCH has integrated pull-ups for GPIO 199 & 200.

DESIGN NOTE:
Designs that strap LPCCLK0 high (EC enabled) can only connect LPCCLK0 to an LPC device in the S5 power domain (or not use it). Failure to do so may result in incorrect strap capture. PCI clocks can be used as a substitute for LPC clocks to devices in the S0 power domain if needed.

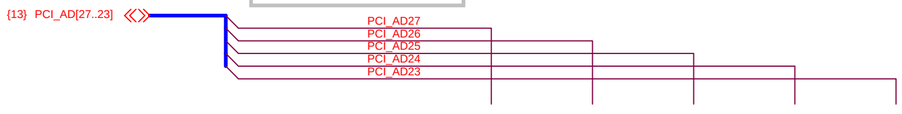
DESIGN NOTE:
Designs that use GPIO 199/200 for GPIO functions must ensure that they are not driven at the deassertion of RSMRST#. Failure to do so may result in incorrect strap capture.

LAYOUT NOTE:
Overlap common pads for strap resistors and place on the signal trace to eliminate stubs.

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 EC_PWM3 / GPIO199 EC_PWM2
PULL HIGH	LOW POWER MODE (Not Supported)	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled (Not Supported)	DEBUG STRAP ENABLE	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (DEFAULT)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	DEBUG STRAP DISABLE DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = Reserved

DEBUG STRAPS

DESIGN NOTE:
The CH has integrated 15K pull-ups on PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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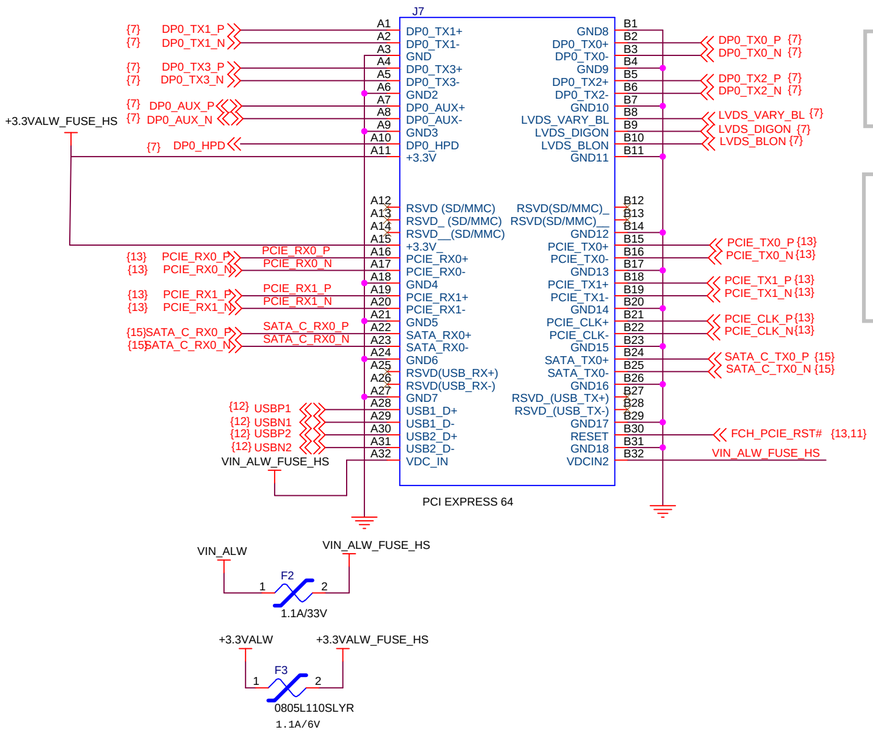
Drawn by: Victor Navarro	Page Title: FCH STRAPS
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
	Date: Thursday, August 08, 2013; Sheet 16 of 23



DESIGN NOTE:
PCIe lanes can be independent and connected to two different devices; or ganged and connected to a single device.

DESIGN NOTE:
PCIE_RXx_x signals are outputs from the FCH GPP bridge and should be connected to the inputs of an external PCIe device.

PCIE_TXx_x signalse are inputs to the FCH GPP bridge and should be connected to the outputs of an external PCIe device.

DESIGN NOTE:
This SATA port supports port multiplier devices allowing for multiple SATA drives connected to this single port.

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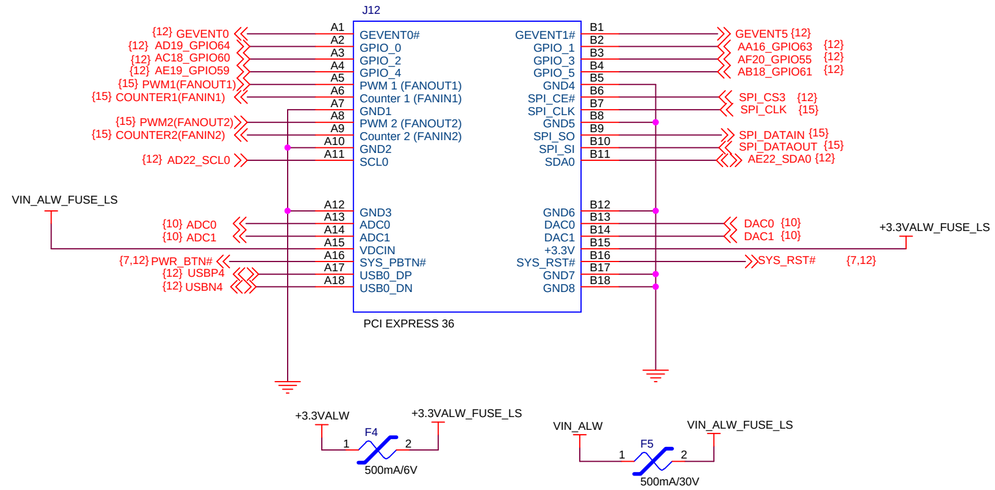
Drawn by: Victor Navarro	Page Title: HIGH SPEED CARD EDGE	
Approved by: Scott Hoot	Size: C	Document Number: GZMO_8_1_2013 — Rev: I
	Date: Thursday, August 08, 2013	Sheet 17 of 23



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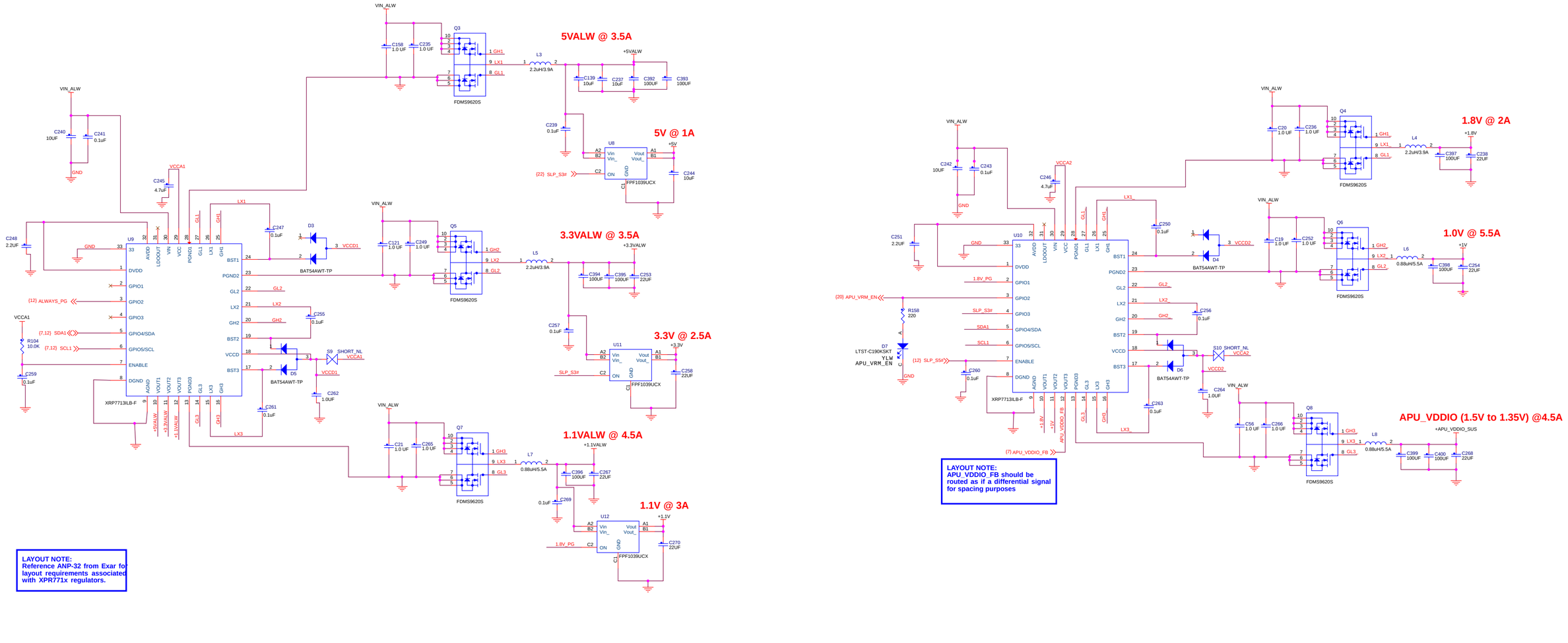
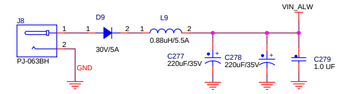
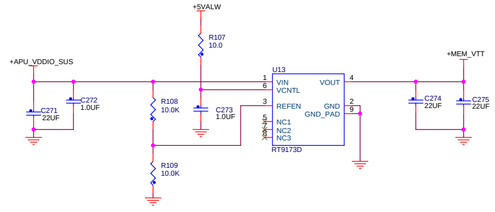
Designed by: Mauricio Capistran	Design Title **GIZMO BOARD REV 5**	
Drawn by: Victor Navarro	Page Title LOW SPEED CARD EDGE	
Approved by: Scott Hoot	Size C	Document Number GZMO_8_1_2013 Rev I
	Date: Thursday, August 08, 2013	Sheet 18 of 23



POWER JACK



POWER VTT RAM



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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
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Approved by: Scott Hoot	Size: D	Document Number: GZMO_8_1_2013 — Rev: I
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DESIGN NOTE:
This regulator is designed to provide VDDCR_CPU@11A and VDDCR_NB@10A. If a lower TDP processor is used, supply capacity may be reduced.

U14 ISL6265AHRTZ

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

LAYOUT NOTE:
BOTTOM PAD CONNECT TO GND THROUGH 6 VIAS

LAYOUT NOTE:
NO PART TO PLACE

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Drawn by: Victor Navarro	Page Title: POWER MANAGEMENT APU
Approved by: Scott Hoot	Size: C; Document Number: GZMO_8_1_2013; Rev: I
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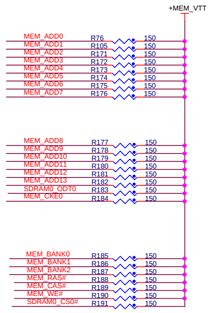
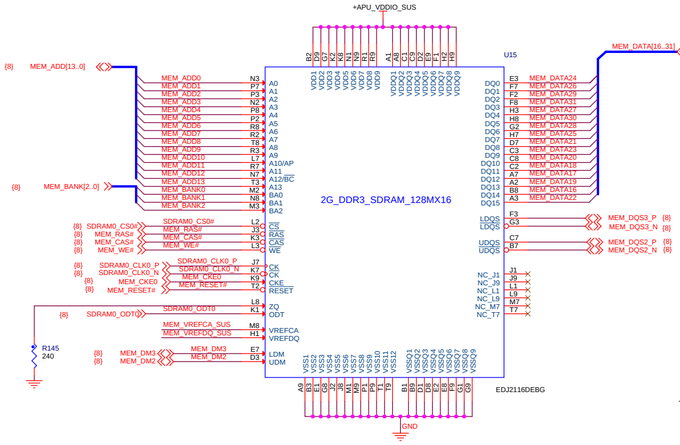
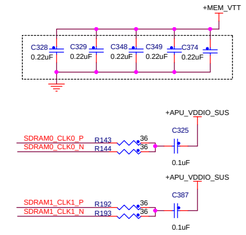
SDRAM0 Decoupling Caps

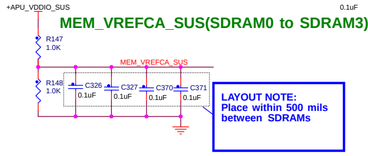
PULL UP TO VTT



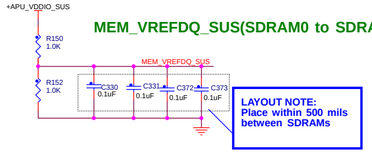




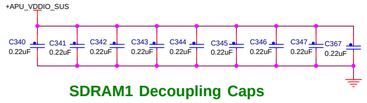
MEM_VREFCA_SUS(SDRAM0 to SDRAM3)



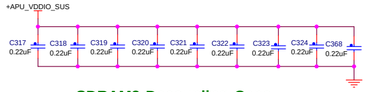
MEM_VREFDQ_SUS(SDRAM0 to SDRAM3)

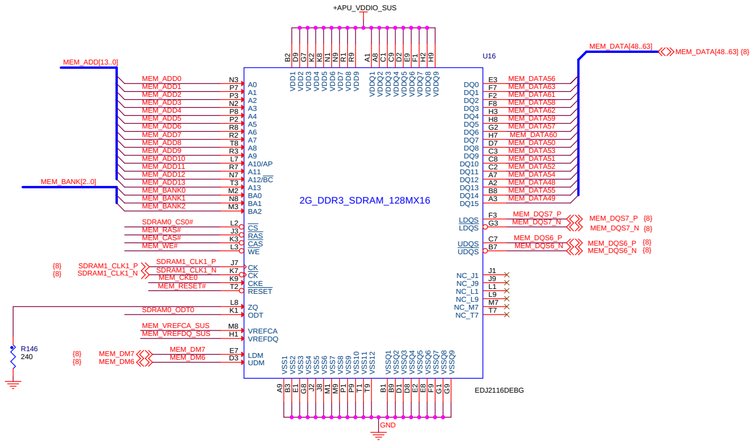


SDRAM1 Decoupling Caps

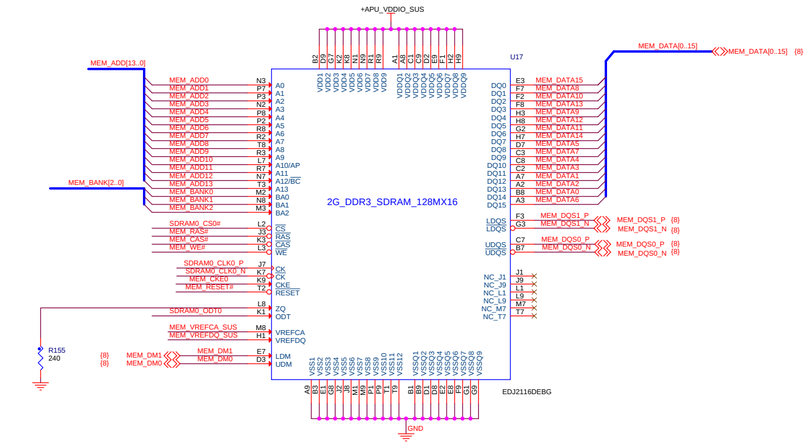


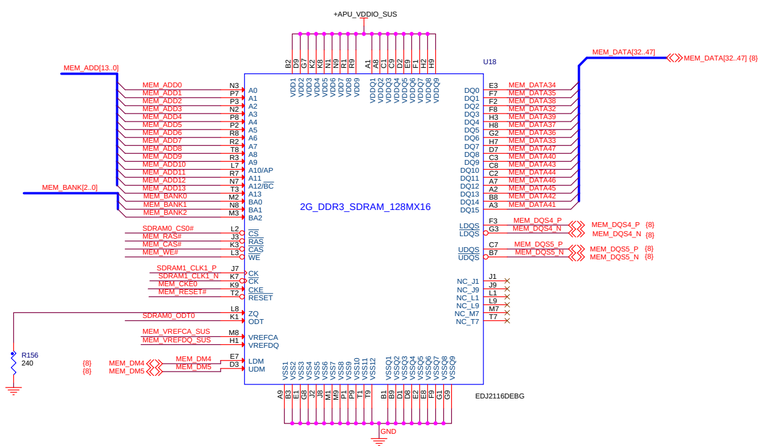
SDRAM2 Decoupling Caps





SDRAM3 Decoupling Caps





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Designed by: Mauricio Capistran	Design Title: GIZMO BOARD REV 5	
Drawn by: Victor Navarro	Page Title: RAM	
Approved by: Scott Hoot	Size: D	Document Number: GZMO_8_1_2013 — Rev: I
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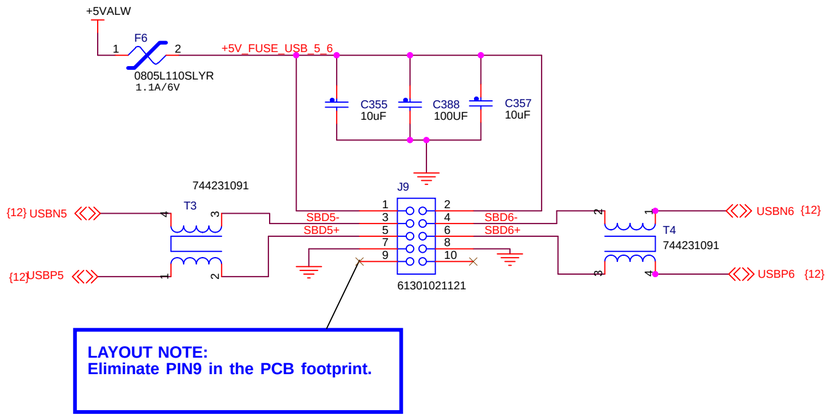

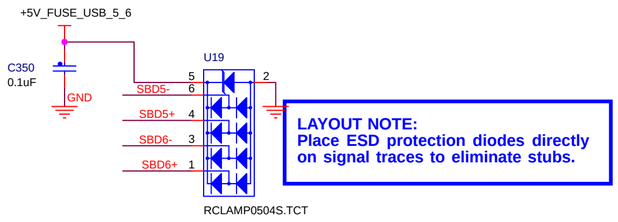

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Drawn by: Victor Navarro	Page Title USB	
Approved by: Scott Hoot	Size C	Document Number GZMO_8_1_2013 Rev I
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LAYOUT NOTE:
See the FT1 Motherboard Design Guide (PID 45339) for detailed impedance requirements for each section of the VGA routing.

LAYOUT NOTE:
Place filter inductors at 90 degrees from each other to reduce inductive cross-talk.

LAYOUT NOTE:
Place ESD protection diodes directly on signal traces to eliminate stubs.

+5V
R157 4.7K
{7} APU_DAC_SCL
R165 4.7K
{7} APU_DAC_SDA

{7} APU_VGA_R
{7} APU_VGA_G
{7} APU_VGA_B

R162 150
R163 150
R164 150
GND

L131 2 16nH/560mA
L151 2 16nH/560mA
L171 2 16nH/560mA
L141 2 16nH/560mA
L161 2 16nH/560mA
L181 2 16nH/560mA

C356 5pF/50V
C359 5pF/50V
C362 5pF/50V
GND

DESIGN NOTE:
The PI filter design shown here for the RGB signals has been updated to meet the VESA VSIS v1r2 specification.

U20 RCLAMP0504S.TCT
+5V
C352 0.47uF
GND

U21 RCLAMP0504S.TCT
+5V
C351 0.47uF
GND

+5V
F7 0805L110SLYR 1.1A/6V
B19 220 OHM_2A
C353 0.1uF
GND

J10 200-015-263R001
9 +5V
1 R
2 G
3 B
4 NC1
11 NC2
15 DDC CLK
12 DDC DAT
13 HSYNC
14 VSYNC
5 VSS_HSYNC
6 VSS_R
7 VSS_G
8 VSS_B
10 VSS_VSYNC
GND
CASE1 16
CASE2 17
GND

R_FILTER
G_FILTER
B_FILTER

DESIGN NOTE:
Typical displays will pull-up DDC lines to 5V as long as they are powered. This will result in leakage through the on-board pull-ups and protection diodes to the +5V rail in S5/S3 states. The leakage is undesireable but has not shown to cause any functional issues. A diode may be used to block leakage from the display connections but will limit ESD immunity. This is a design trade-off.

DESIGN NOTE:
The FT1 DDC/AUX pins are 5V tolerant.

U22
{7} APU_HSYNC
1 OE
2 DIN
3 GND
5 VCC
4 DOUT
SN74LVC1G125DCKT
+5V
C364 0.1uF
R166 0 DNP

LAYOUT NOTE:
Check footprint TSSOP5

U23
{7} APU_VSYNC
1 OE
2 DIN
3 GND
5 VCC
4 DOUT
SN74LVC1G125DCKT
+5V
C365 0.1uF
R167 0 DNP

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