

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR1840Y85*	8500	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 300\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR1840Y80	8000	
DCR1840Y75	7500	
DCR1840Y70	7000	

Lower voltage grades available.
 *8200V @ -40°C , 8500V @ 0°C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1840Y85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	8500V
$I_{T(AV)}$	1840A
I_{TSM}	25000A
dV/dt^*	1500V/μs
dI/dt	300A/μs

* Higher dV/dt selections available

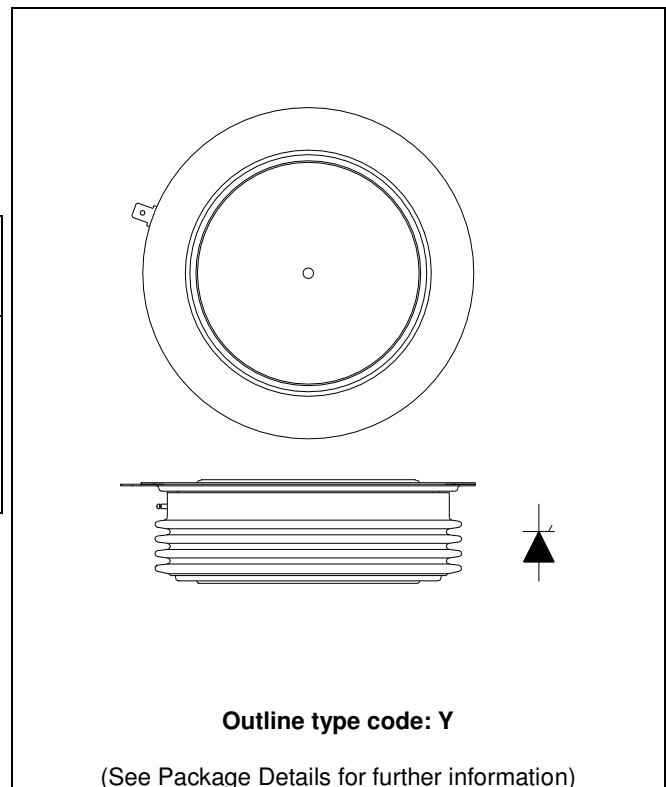


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1840	A
$I_{T(RMS)}$	RMS value	-	2890	A
I_T	Continuous (direct) on-state current	-	2770	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	25.0	kA
I^2t	I^2t for fusing	$V_R = 0$	3.125	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00835	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0134	$^{\circ}\text{C/W}$
			Cathode DC	-	0.023	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 54.0kN (with mounting compound)	Double side	-	0.002	$^{\circ}\text{C/W}$
			Single side	-	0.004	$^{\circ}\text{C/W}$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$	
F_m	Clamping force		48	59	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	300	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μs	
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$ Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Repetitive 50Hz	-	150	A/ μs
			Non-repetitive	-	300	A/ μs
$V_{T(TO)}$	Threshold voltage – Low level	100A to 1000A at $T_{case} = 125^{\circ}C$	-	0.9	V	
	Threshold voltage – High level	1000A to 7200A at $T_{case} = 125^{\circ}C$	-	1.3	V	
r_T	On-state slope resistance – Low level	100A to 1000A at $T_{case} = 125^{\circ}C$	-	0.888	m Ω	
	On-state slope resistance – High level	1000A to 7200A at $T_{case} = 125^{\circ}C$	-	0.55	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	-	3	μs	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, dI/dt = 1A/ μs , dV _{DR} /dt = 20V/ μs linear	-	1200	μs	
Q_S	Stored charge	$I_T = 2000A$, $T_j = 125^{\circ}C$, dI/dt = 1A/ μs ,	4800	8000	μC	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25°C	400	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	15	mA

CURVES

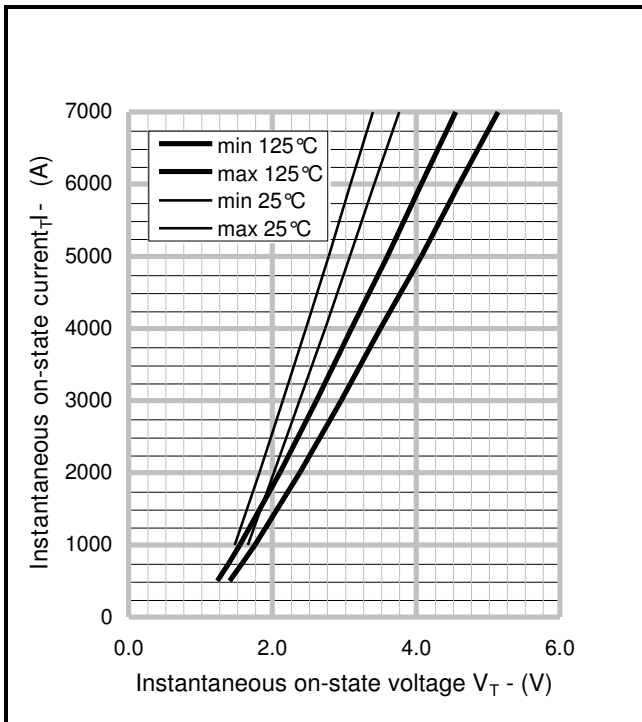


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.398265
 B = 0.121095
 C = 0.000524
 D = -0.000007

these values are valid for T_j = 125°C for I_T 500A to 7200A

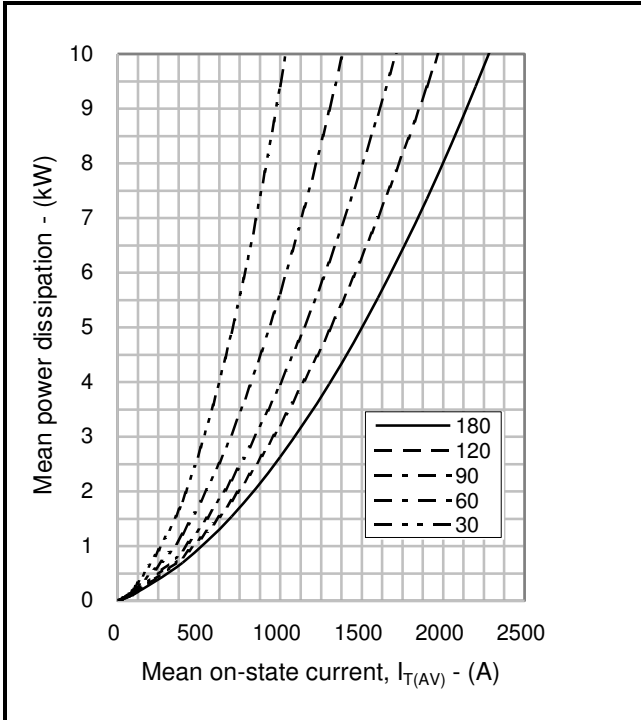


Fig.3 On-state power dissipation – sine wave

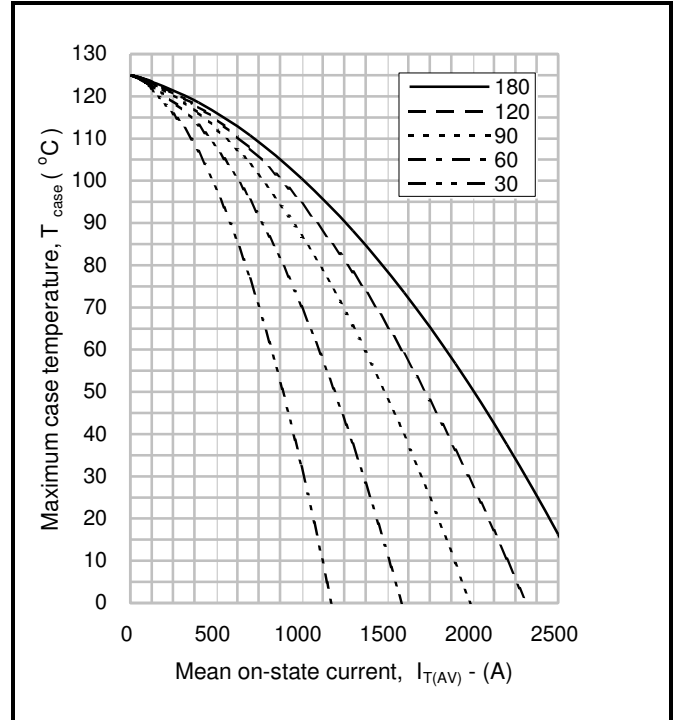


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

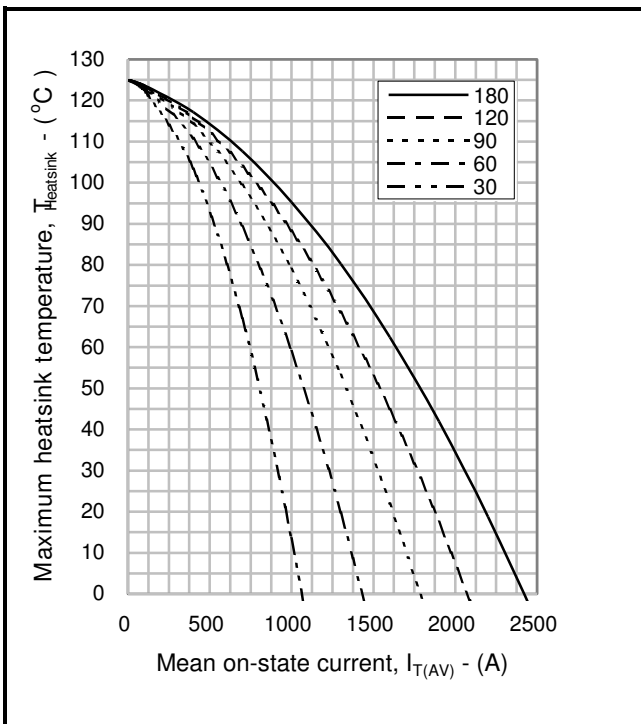


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

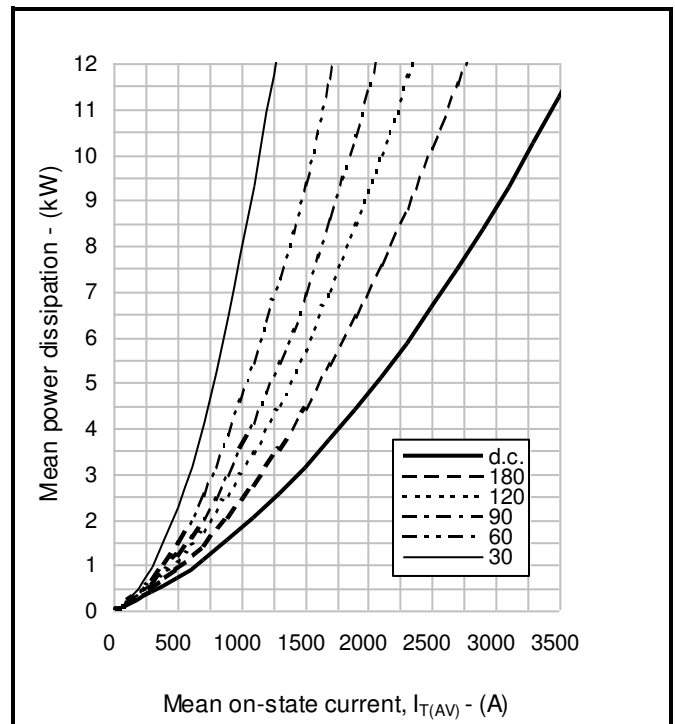


Fig.6 On-state power dissipation – rectangular wave

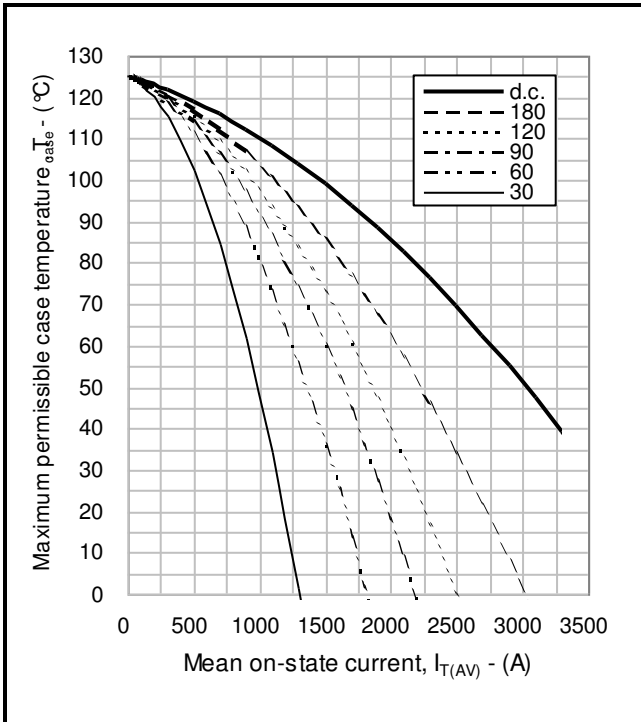


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

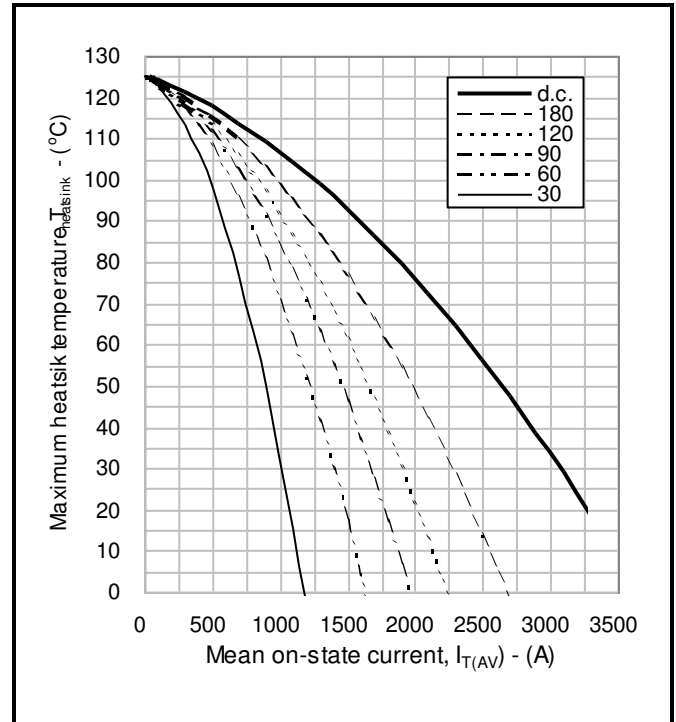


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

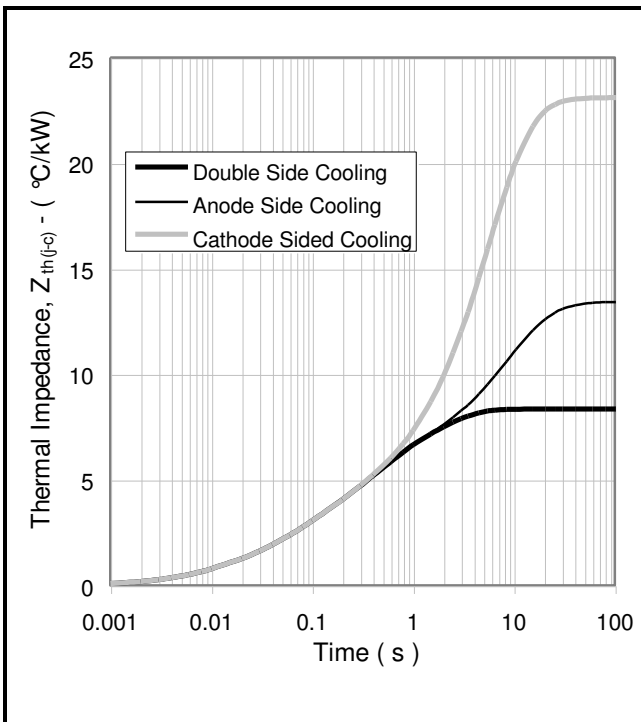


Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

		1	2	3	4
Double side cooled	R _i (°C/kW)	0.612	1.7721	3.1053	2.8608
	T _i (s)	0.010332	0.056415	0.333082	1.6323
Anode side cooled	R _i (°C/kW)	0.7009	1.9388	3.61	7.1383
	T _i (s)	0.011328	0.065993	0.419695	9.0612
Cathode side cooled	R _i (°C/kW)	0.6728	2.0168	1.7306	18.6391
	T _i (s)	0.010954	0.065544	0.30379	5.7274

$$Z_{th} = \sum [R_i \times (1 - \exp.(-t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

θ°	Double side cooling		Anode Side Cooling		Cathode Sided Cooling	
	$\Delta Z_{th}(z)$		$\Delta Z_{th}(z)$		$\Delta Z_{th}(z)$	
	sine.	rect.	sine.	rect.	sine.	rect.
180	0.94	0.65	0.94	0.64	0.94	0.64
120	1.09	0.92	1.08	0.91	1.08	0.91
90	1.24	1.07	1.23	1.06	1.24	1.06
60	1.38	1.23	1.37	1.22	1.37	1.22
30	1.49	1.40	1.47	1.38	1.48	1.39
15	1.54	1.49	1.52	1.47	1.53	1.48

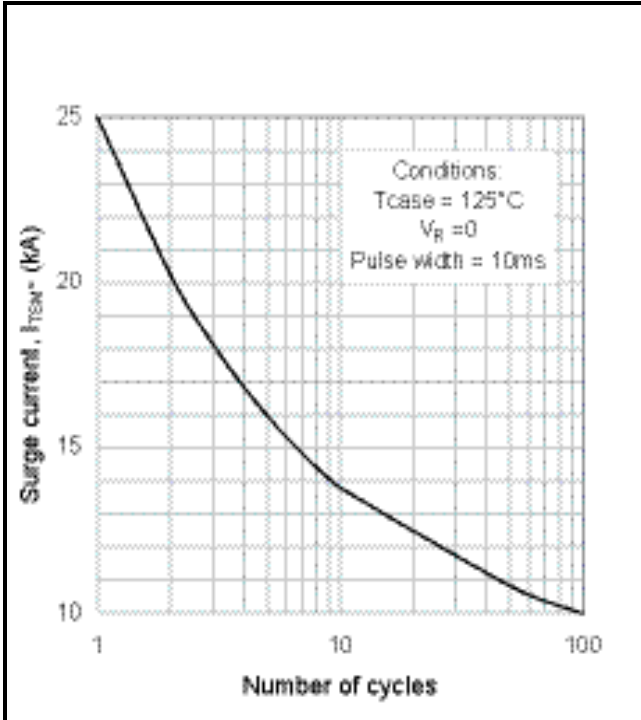


Fig.10 Multi-cycle surge current

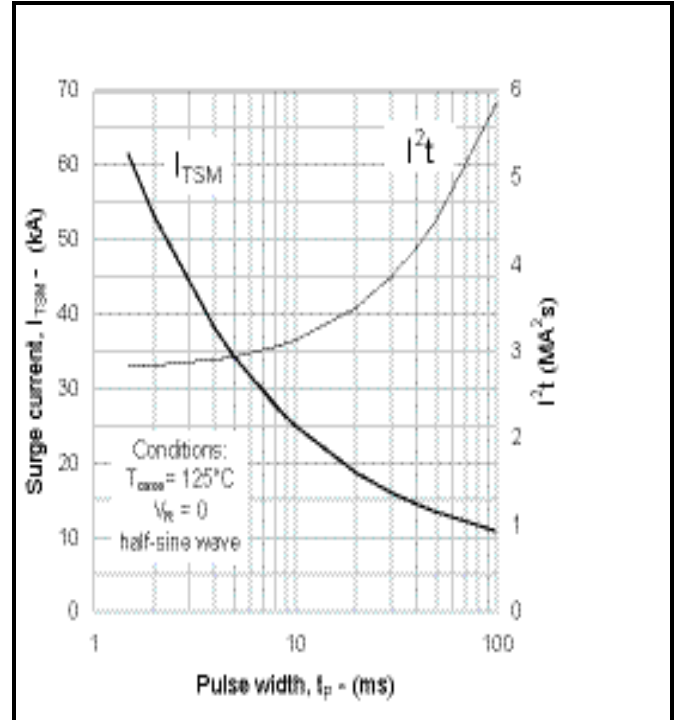


Fig.11 Single-cycle surge current

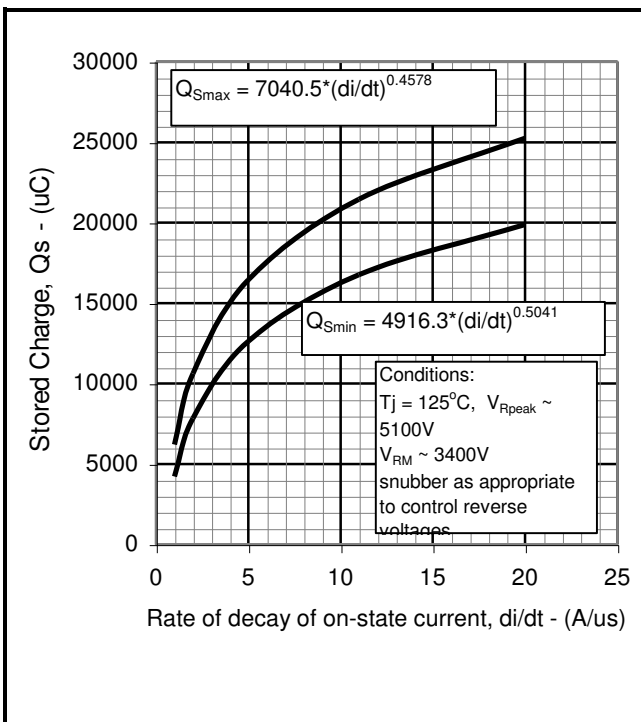


Fig.12 Stored charge

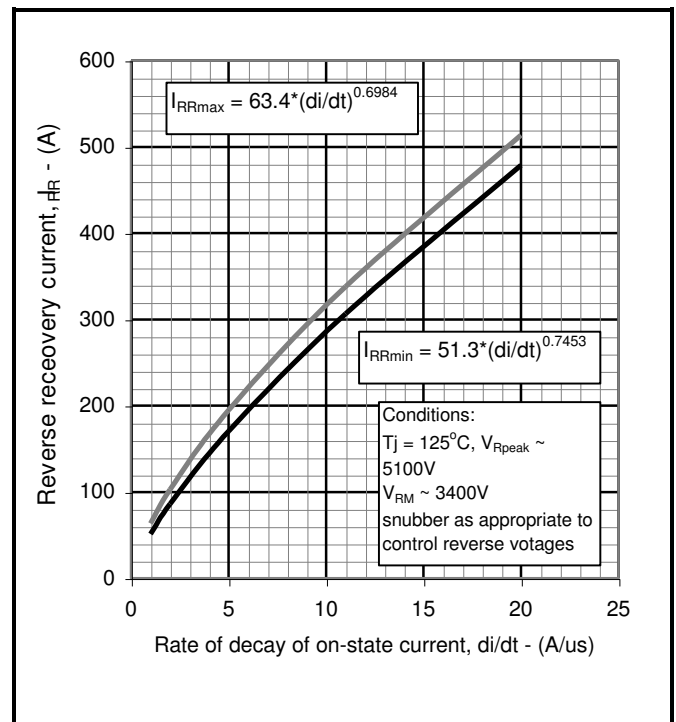


Fig.13 Reverse recovery current

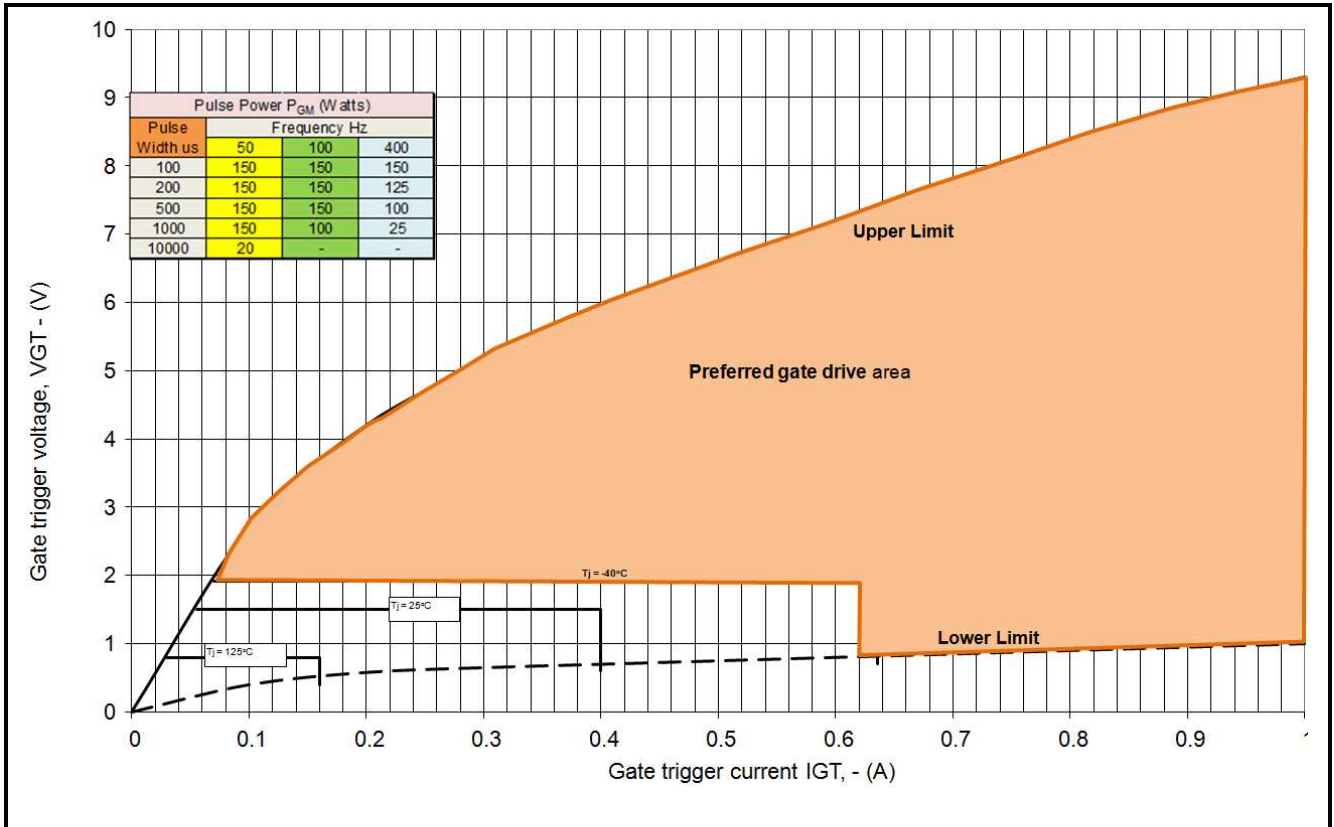


Fig14 Gate Characteristics

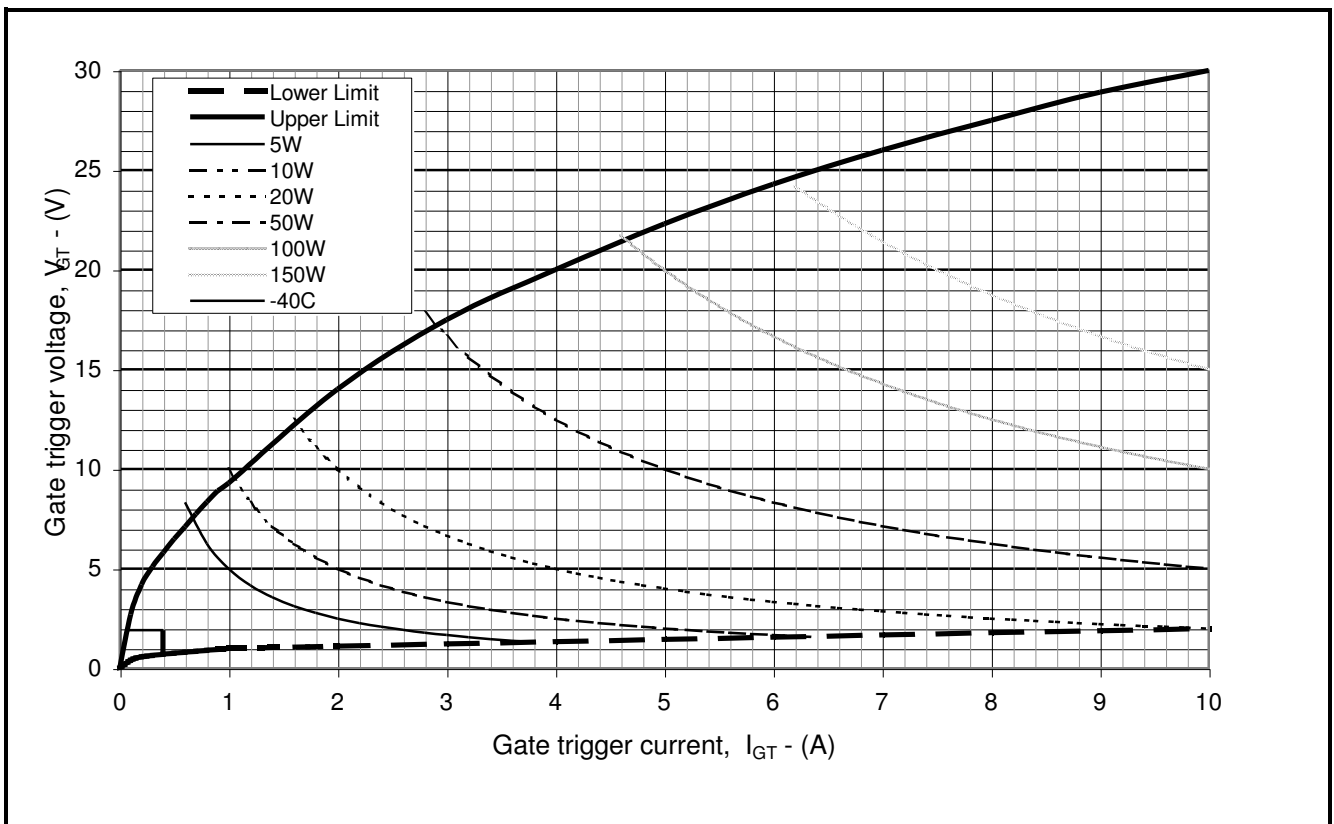


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

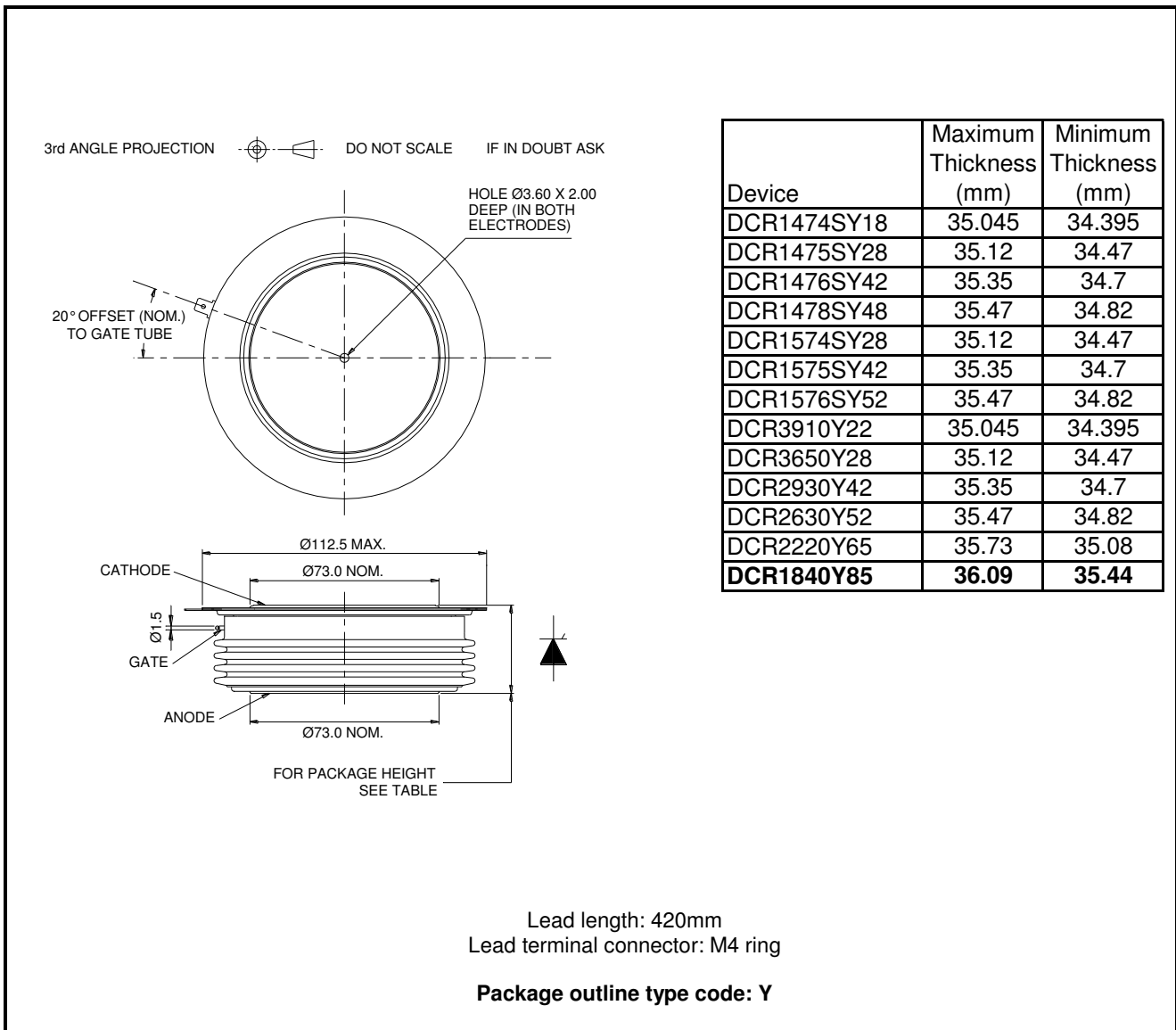


Fig.16 Package outline

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- | | |
|---------------------------------|---|
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| Provisional Information: | Some initial development work has been performed. The datasheet represents a view of the end product based on very limited information. Certain details will change. |
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