



### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- Medium Voltage Soft Starts
- High Voltage Power Supplies
- Static Switches

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR680N85*	8500	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM}$ & $V_{RSM} =$ $V_{DRM}$ & $V_{RRM} + 100\text{V}$ respectively
DCR680N80	8000	
DCR680N75	7500	
DCR680N70	7000	

Lower voltage grades available.  
 8200V @  $-40^{\circ}\text{C}$ , 8500V @  $0^{\circ}\text{C}$

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR680N85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### KEY PARAMETERS

$V_{DRM}$	<b>8500V</b>
$I_{T(AV)}$	<b>677A</b>
$I_{TSM}$	<b>9800A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$di/dt$	<b>200A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available

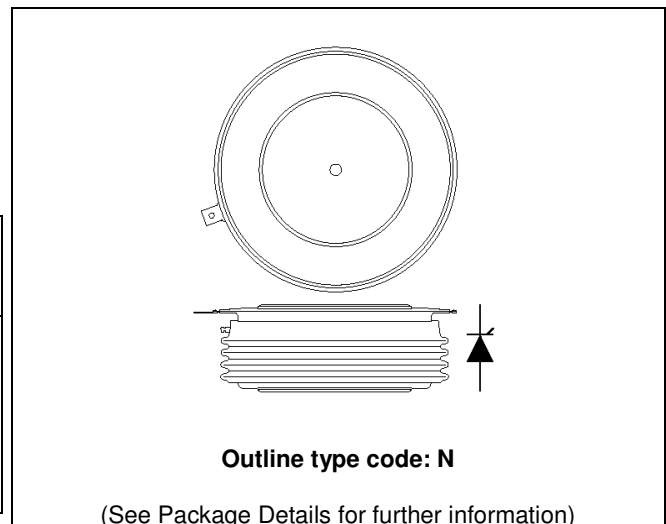


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	677	A
$I_{T(RMS)}$	RMS value	-	1063	A
$I_T$	Continuous (direct) on-state current	-	1013	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	9.8	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	0.48	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0221	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.041	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0516	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23 kN (with mounting compound)	Double side	-	0.004	$^{\circ}\text{C/W}$
			Single side	-	0.008	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		20.0	25.0	kN	

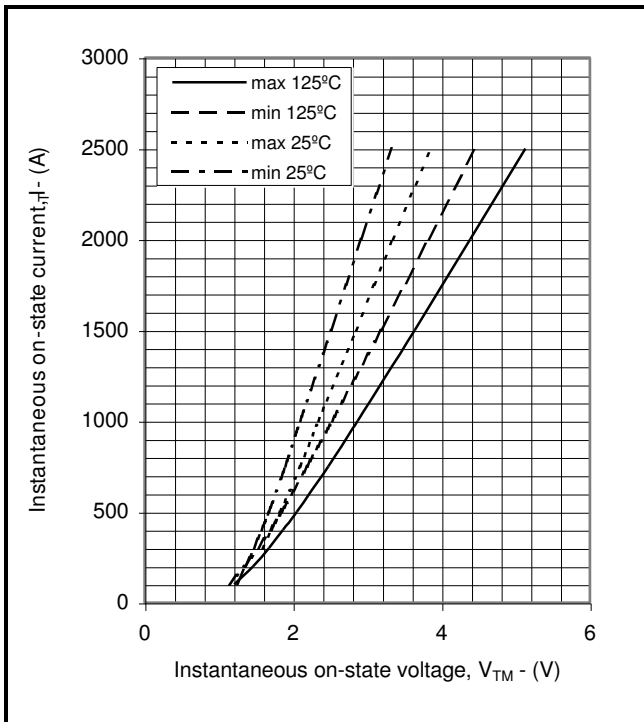
**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	200	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$di/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	100	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	200	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	100A to 500A at $T_{case} = 125^{\circ}C$	-	1.03	V	
	Threshold voltage – High level	500A to 2500A at $T_{case} = 125^{\circ}C$	-	1.3	V	
$r_T$	On-state slope resistance – Low level	100A to 500A at $T_{case} = 125^{\circ}C$	-	2.06	m $\Omega$	
	On-state slope resistance – High level	500A to 2500A at $T_{case} = 125^{\circ}C$	-	1.542	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $I_{peak} = 1000A$ , $t_p = 1000\mu s$ , $V_{RM} = 100V$ , $di/dt = -5A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear to 2500V	-	1200	$\mu s$	
$I_{RR}$	Reverse recovery current	$I_T = 1000A$ , $t_p = 1000\mu s$ , $T_j = 125^{\circ}C$ , $di/dt = -5A/\mu s$ , $V_R = 100V$	95	118	A	
$Q_S$	Stored charge		3000	4000	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	350	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	15	mA

**CURVES**



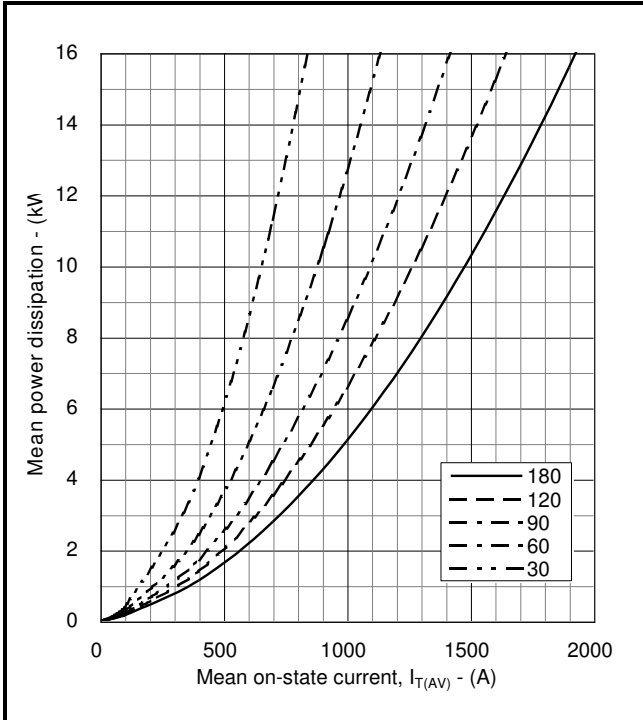
**Fig.2 Maximum & minimum on-state characteristics**

**V<sub>TM</sub> EQUATION**

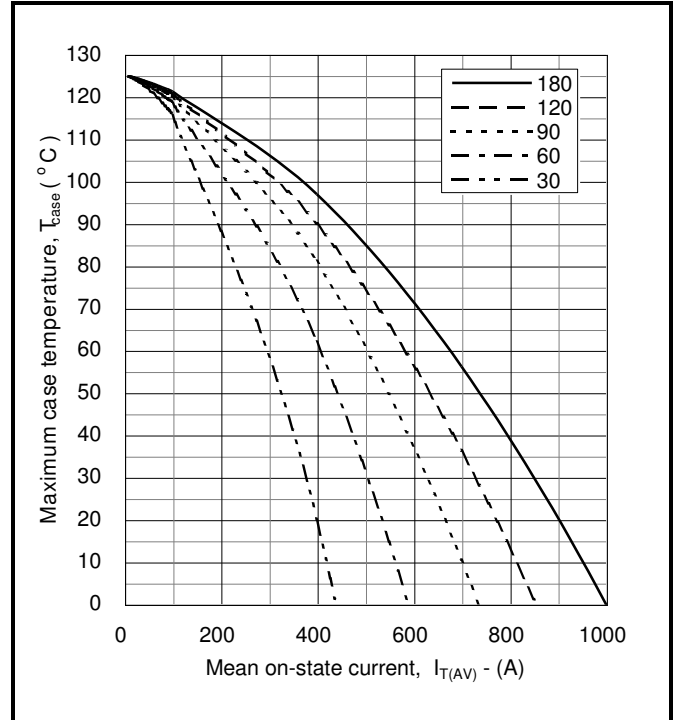
$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.454245  
 B = 0.106933  
 C = 0.001271  
 D = 0.013218

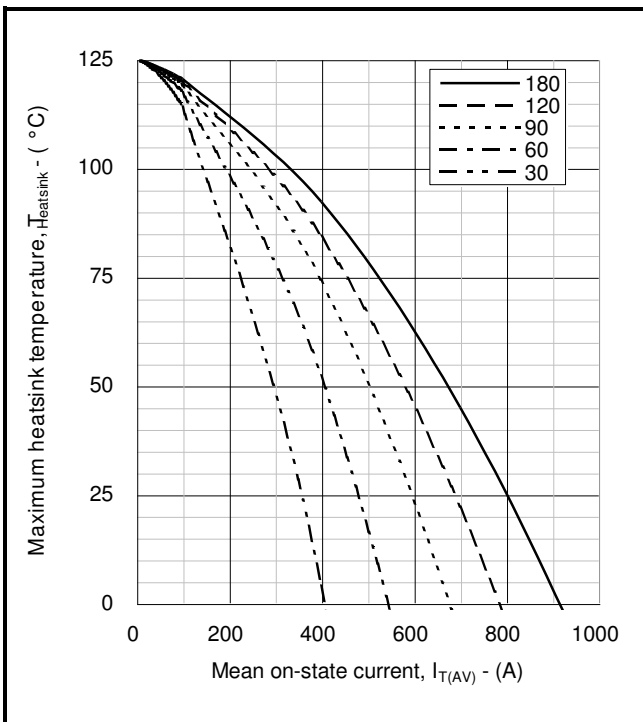
these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 100A to 3000A



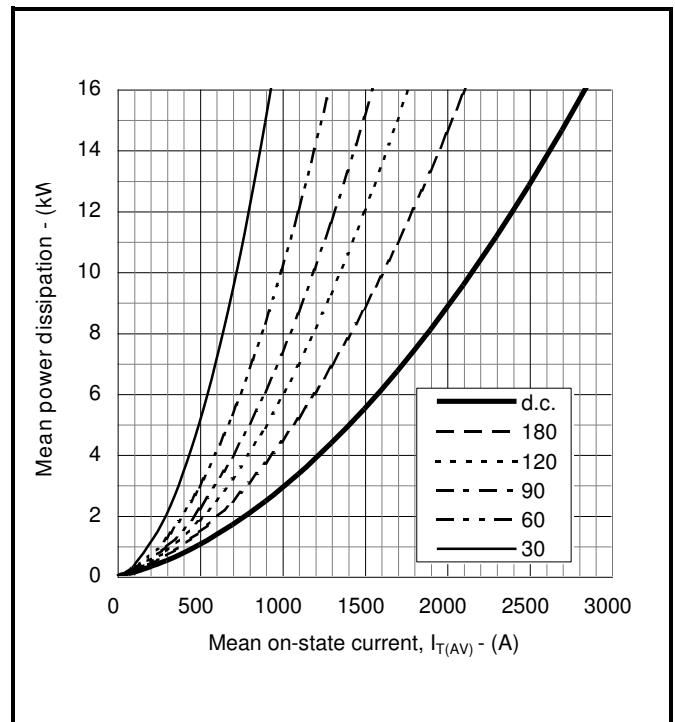
**Fig.3 On-state power dissipation – sine wave**



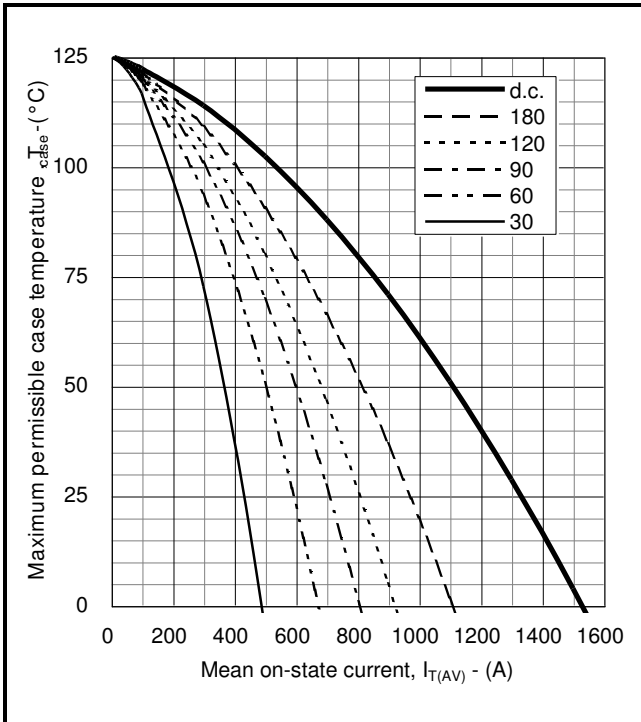
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



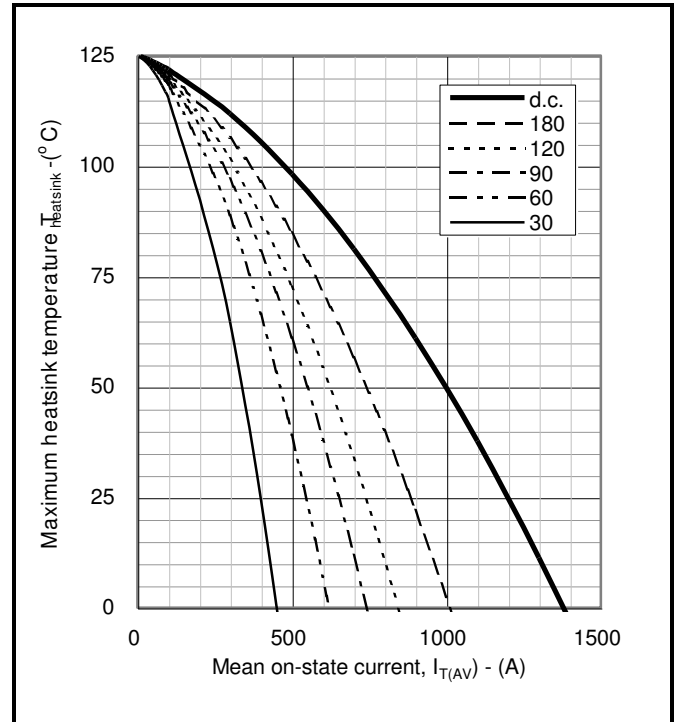
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



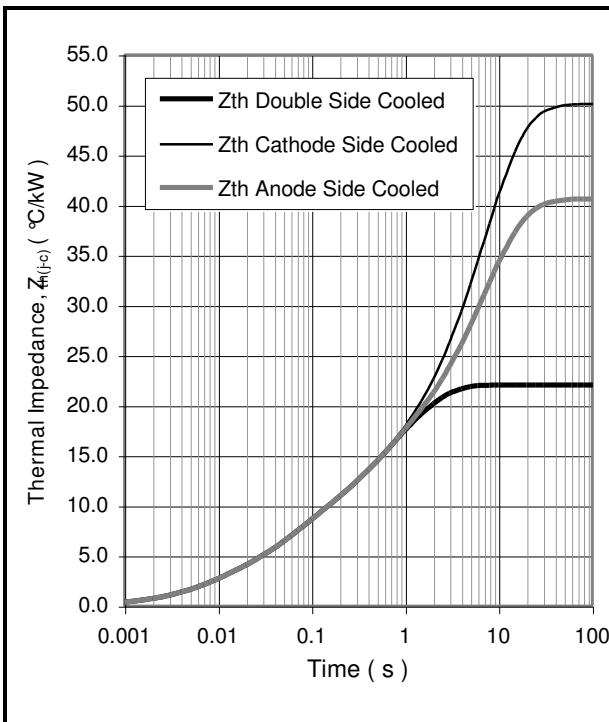
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	3.4733	4.9047	9.1463	4.5220
	T <sub>i</sub> (s)	0.1457	0.0166	1.2832	0.3767
Anode side cooled	R <sub>i</sub> (°C/kW)	7.6674	5.0530	9.7355	27.5992
	T <sub>i</sub> (s)	0.2241	0.0169	4.0566	8.2780
Cathode side cooled	R <sub>i</sub> (°C/kW)	6.0393	4.2782	5.1301	25.0874
	T <sub>i</sub> (s)	0.1356	0.0143	0.6594	7.2358

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(-T/T_i))]$$

**ΔR<sub>th(j-c)</sub> Conduction**

Tables show the increments of thermal resistance R<sub>th(j-c)</sub> when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)		θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.		sine.	rect.		sine.	rect.
180	3.03	2.07	180	3.03	2.07	180	3.12	2.12
120	3.49	2.95	120	3.49	2.95	120	3.61	3.04
90	3.99	3.43	90	3.99	3.43	90	4.13	3.54
60	4.43	3.94	60	4.43	3.94	60	4.60	4.08
30	4.77	4.49	30	4.76	4.48	30	4.96	4.66
15	4.92	4.77	15	4.92	4.77	15	5.13	4.97

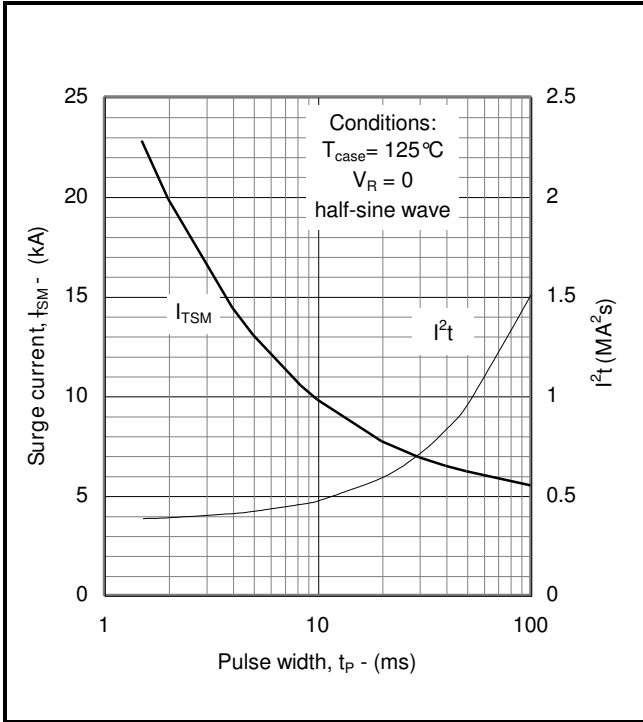


Fig.10 Single-cycle surge current

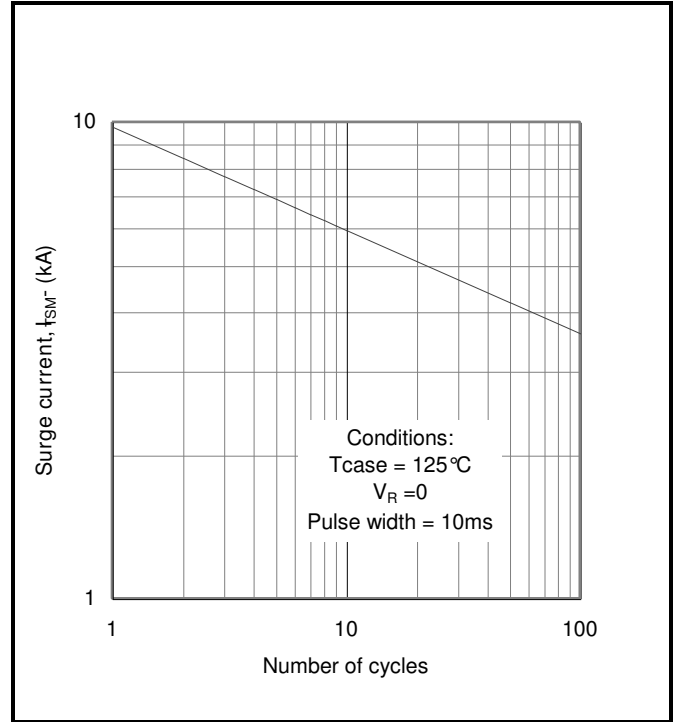


Fig.11 Multi-cycle surge current

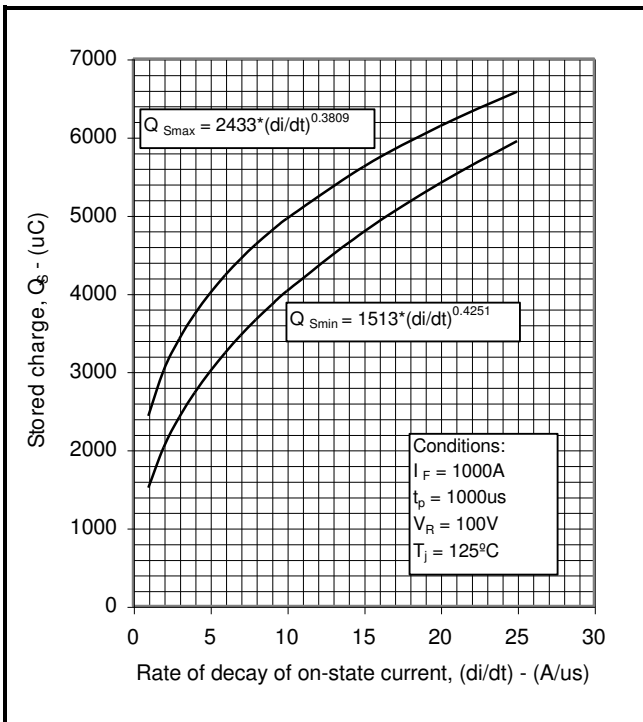


Fig.12 Stored charge

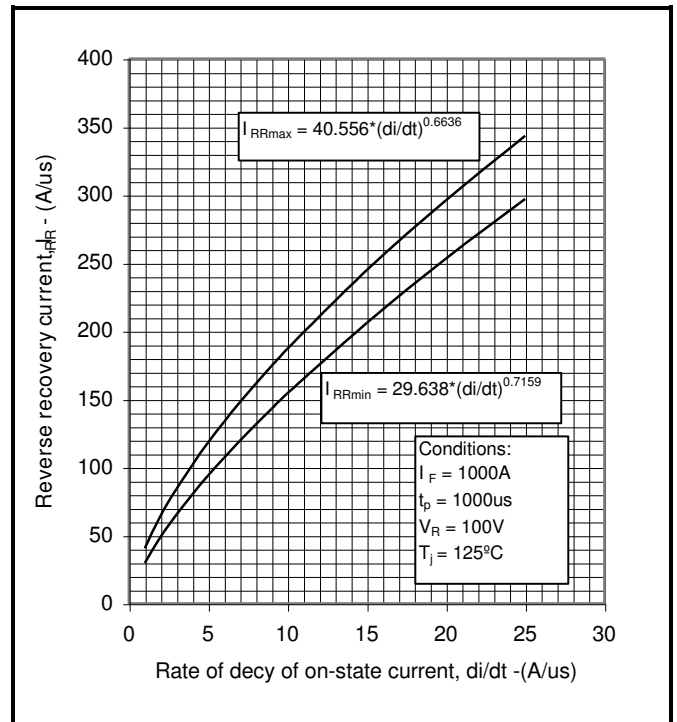


Fig.13 Reverse recovery current

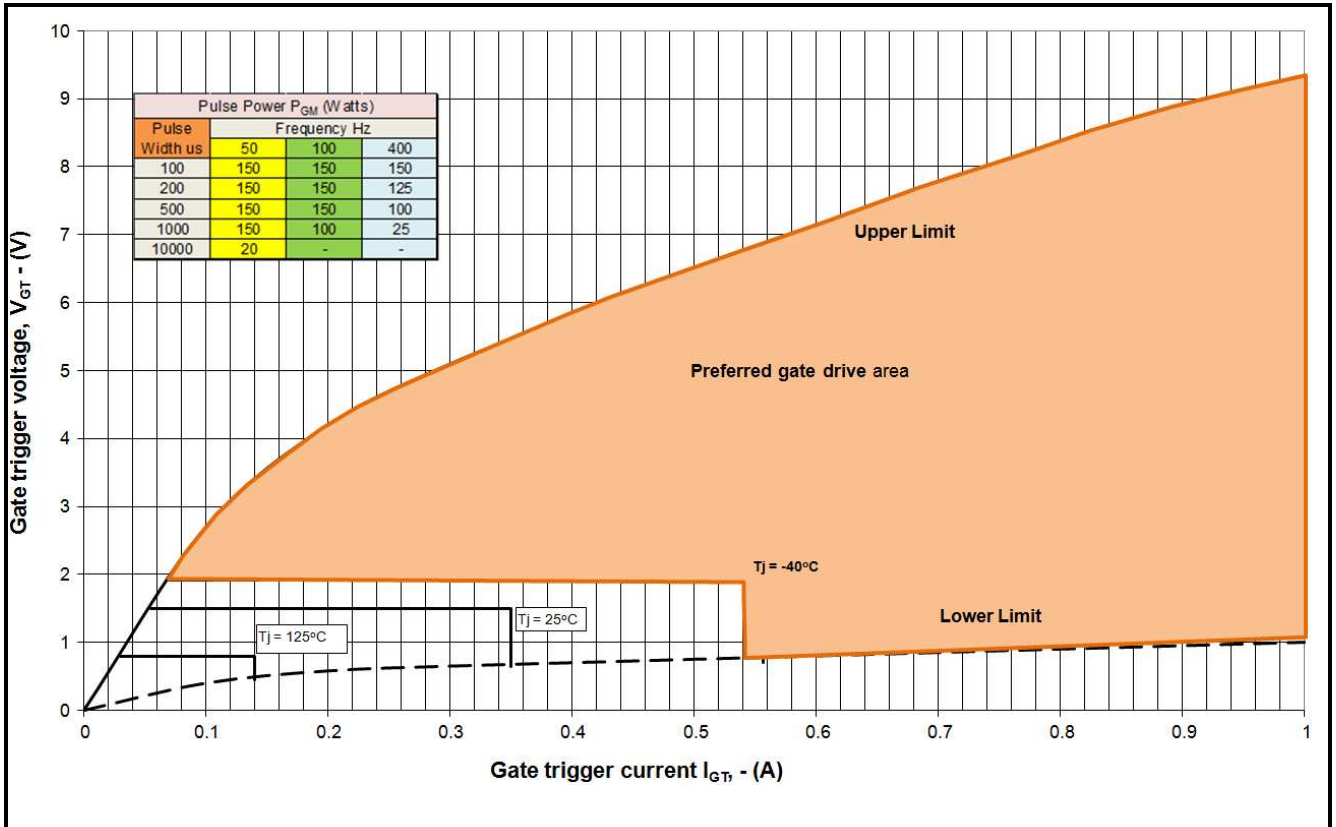


Fig14 Gate Characteristics

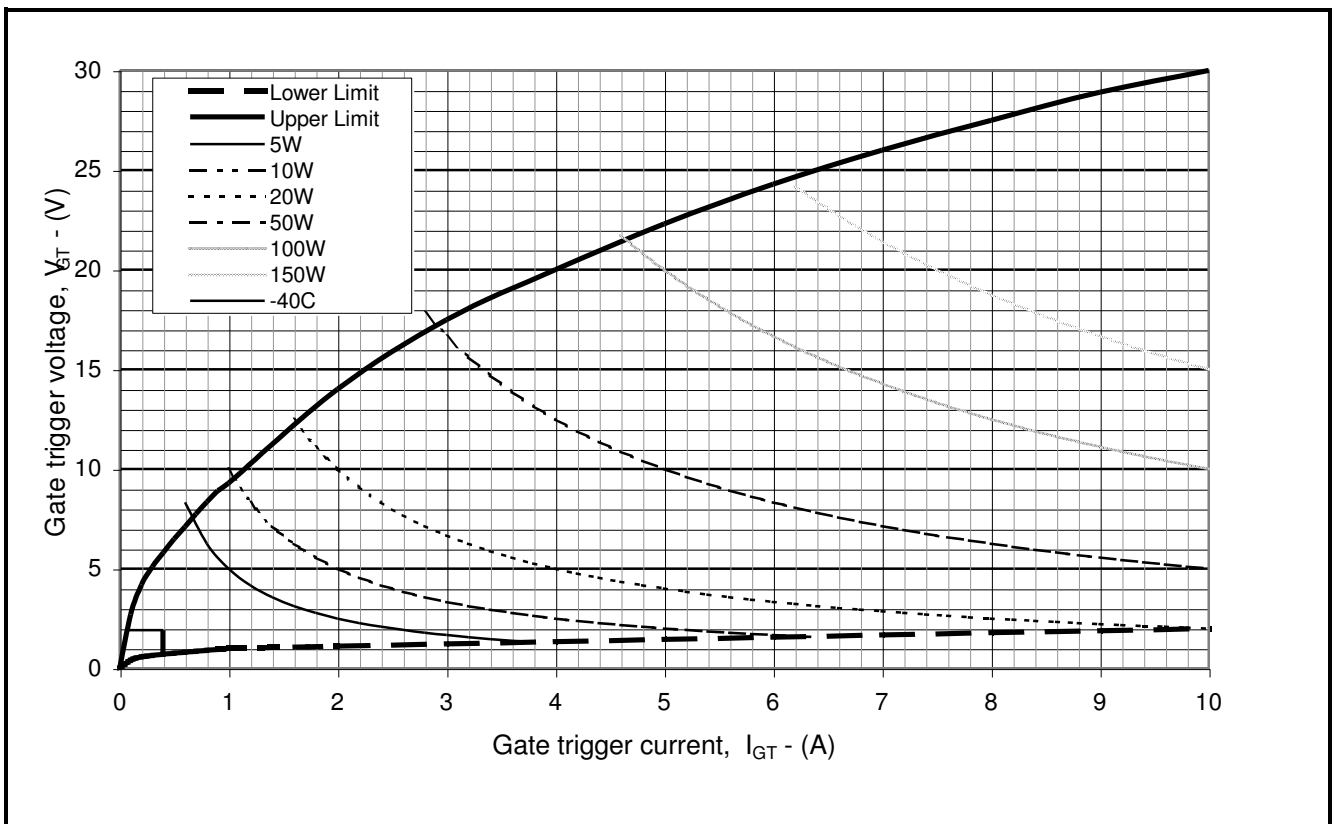
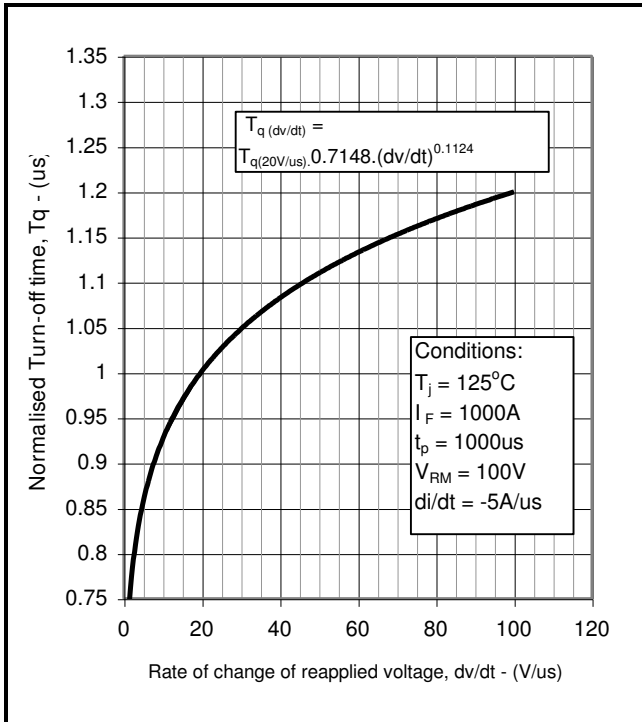


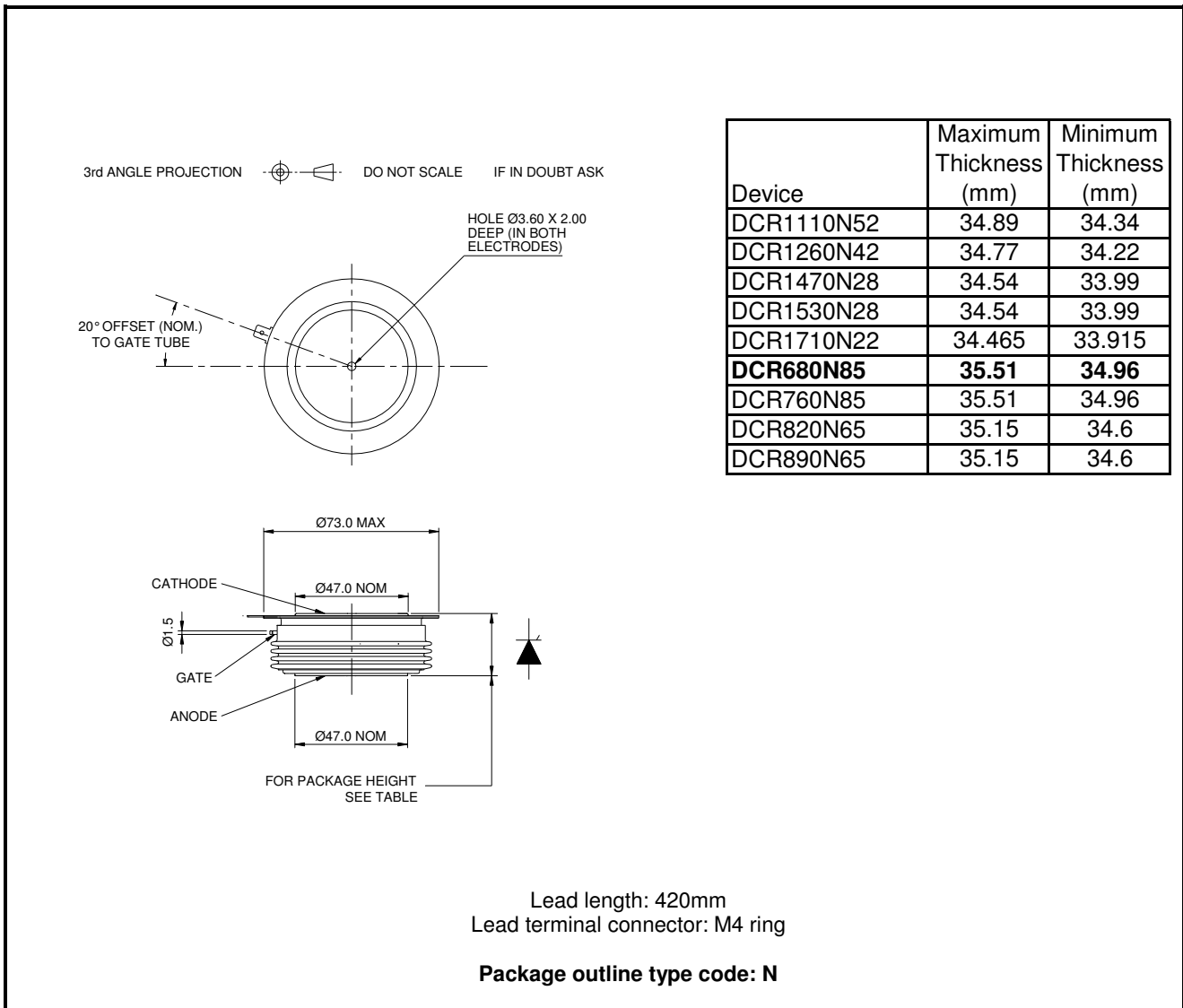
Fig. 15 Gate characteristics



**Fig.16 Turn-off time**

**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**



**Fig.17 Package outline**

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