

### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR2720V52*	5200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR2720V50	5000	
DCR2720V48	4800	

Lower voltage grades available.  
 \* 5000V @  $-40^{\circ}\text{C}$ , 5200V @  $0^{\circ}\text{C}$

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

### DCR2720V52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### KEY PARAMETERS

$V_{DRM}$	<b>5200V</b>
$I_{T(AV)}$	<b>2720A</b>
$I_{TSM}$	<b>36700A</b>
$dV/dt^*$	<b>1500V/<math>\mu\text{s}</math></b>
$dI/dt$	<b>300A/<math>\mu\text{s}</math></b>

\* Higher  $dV/dt$  selections available

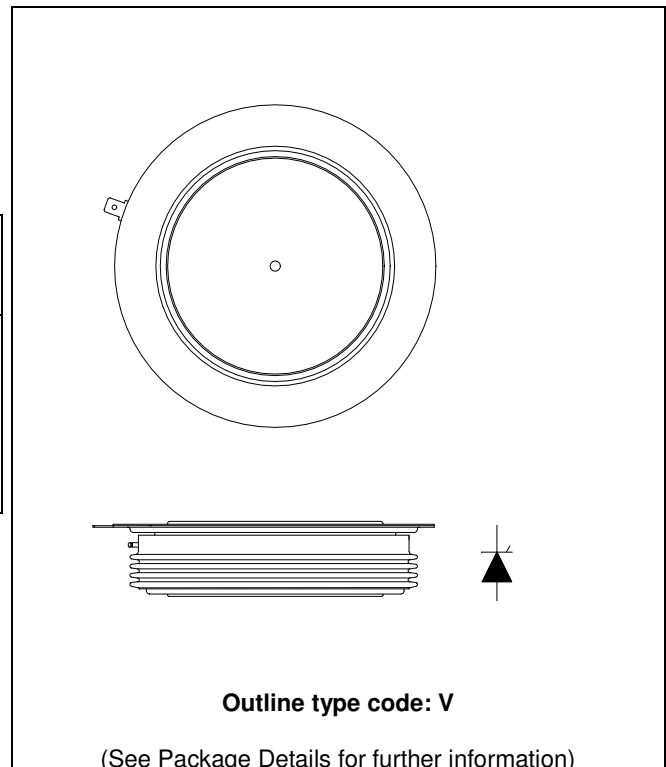


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	2720	A
$I_{T(RMS)}$	RMS value	-	4270	A
$I_T$	Continuous (direct) on-state current	-	4120	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	36.7	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	6.73	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0130	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0178	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	0.002	$^{\circ}\text{C/W}$
			Single side	-	0.004	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		48.0	59.0	kN	

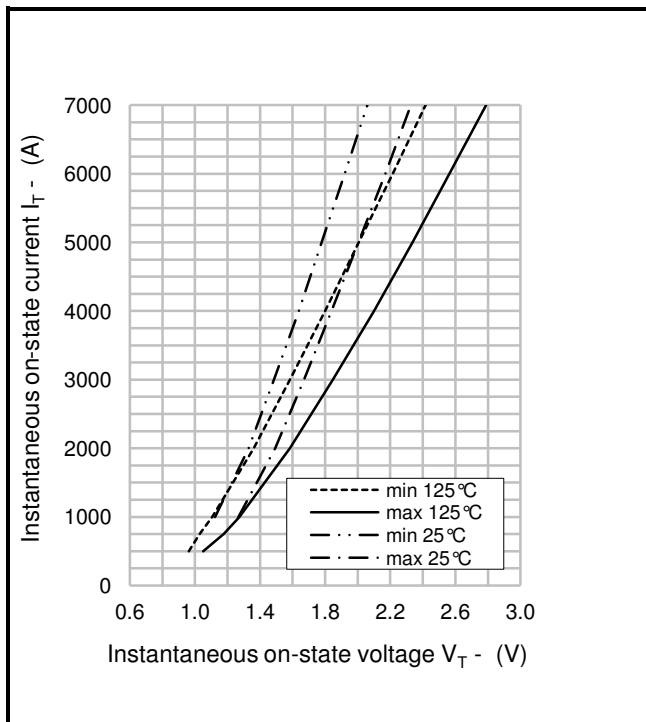
**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	200	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$dI/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	150	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	300	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	500A to 2000A at $T_{case} = 125^{\circ}C$	-	0.90	V	
	Threshold voltage – High level	2000A to 7200A at $T_{case} = 125^{\circ}C$	-	1.1	V	
$r_T$	On-state slope resistance – Low level	500A to 2000A at $T_{case} = 125^{\circ}C$	-	0.3428	m $\Omega$	
	On-state slope resistance – High level	2000A to 7200A at $T_{case} = 125^{\circ}C$	-	0.2414	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	-	3	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 200V$ , $dI/dt = 1A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear	-	600	$\mu s$	
$Q_S$	Stored charge	$I_T = 2000A$ , $T_j = 125^{\circ}C$ , $dI/dt = 1A/\mu s$ ,	2000	4750	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	350	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	15	mA

**CURVES**



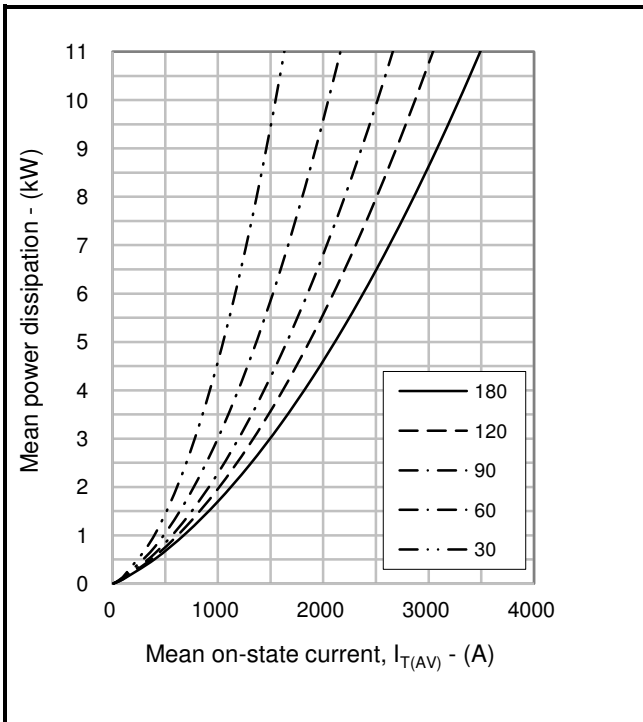
**Fig.2 Maximum & minimum on-state characteristics**

**V<sub>TM</sub> EQUATION**

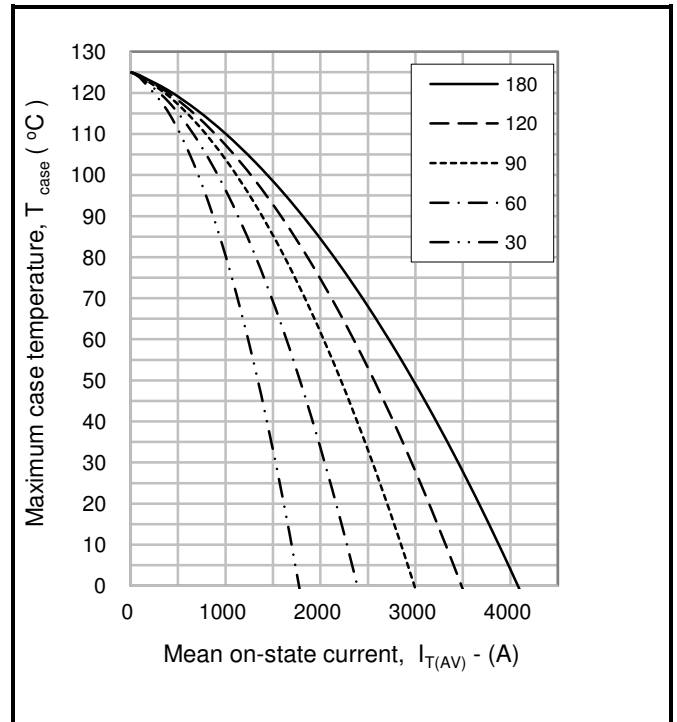
$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = - 0.450546  
 B = 0.251217  
 C = 0.000242  
 D = - 0.008134

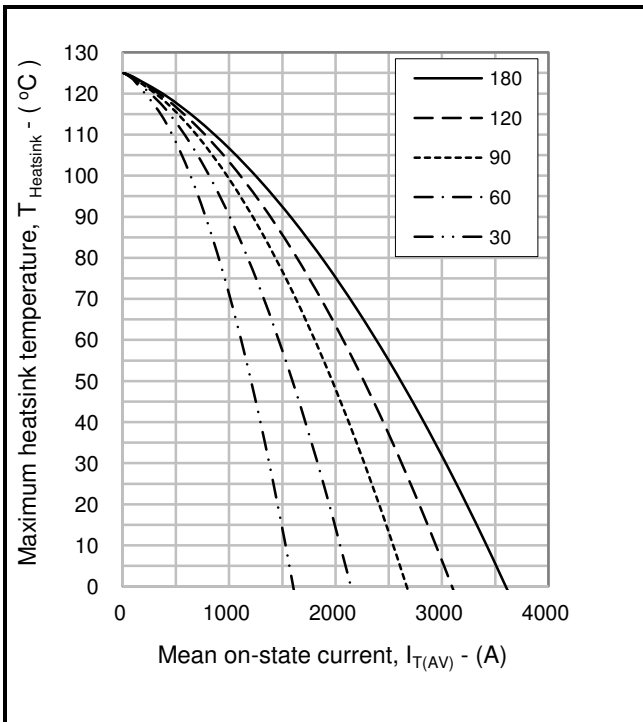
these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 500A to 7200A



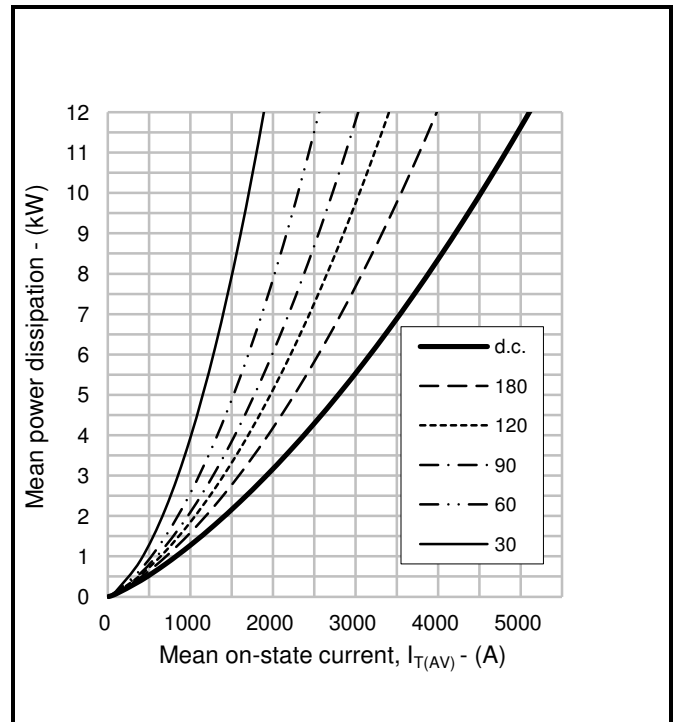
**Fig.3 On-state power dissipation – sine wave**



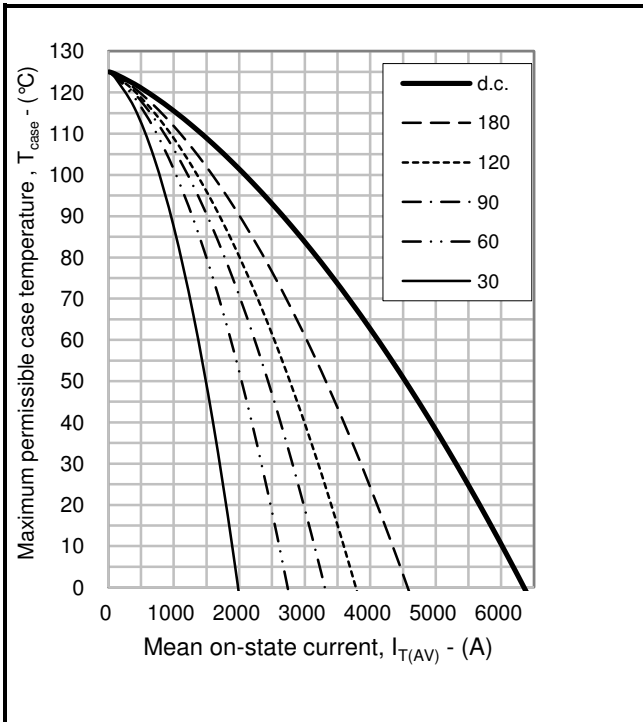
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



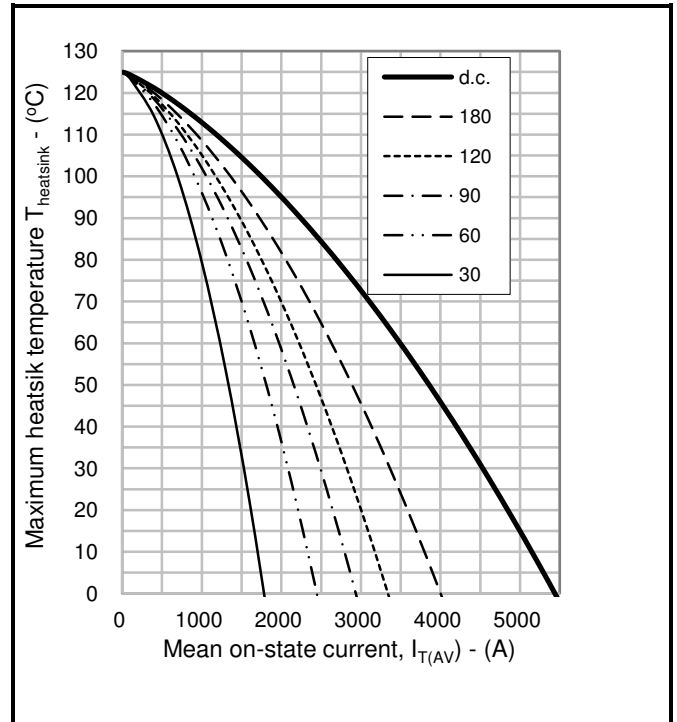
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



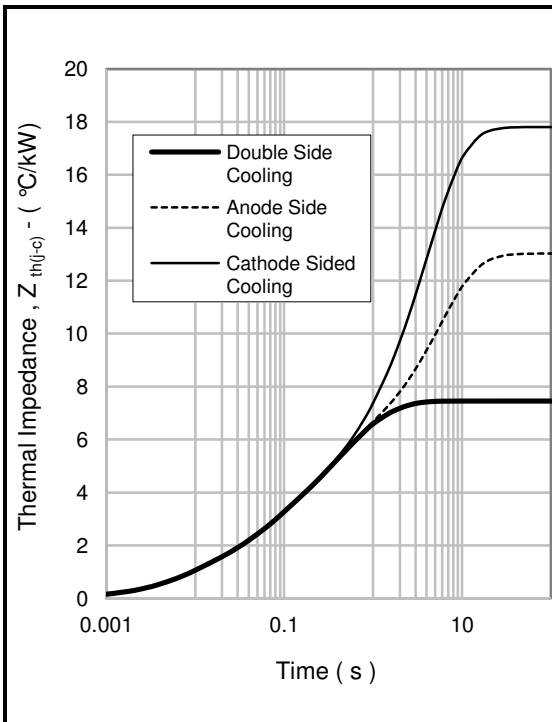
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	$R_{\theta}$ (°C/kW)	0.9206	1.8299	3.4022	1.3044
	$T_{\theta}$ (s)	0.0076807	0.0579454	0.4078613	1.2085
Anode side cooled	$R_{\theta}$ (°C/kW)	0.9032	1.6719	3.0101	7.4269
	$T_{\theta}$ (s)	0.0075871	0.0536531	0.3144537	5.624
Cathode side cooled	$R_{\theta}$ (°C/kW)	0.9478	2.0661	1.6884	13.0847
	$T_{\theta}$ (s)	0.0078442	0.0645541	0.3894389	4.1447

$\Delta R_{th(j-c)}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

$\eta^\circ$	Double side cooling		Anode Side Cooling		Cathode Sided Cooling	
	sine.	rect.	sine.	rect.	sine.	rect.
180	1.34	0.88	1.34	0.88	1.33	0.88
120	1.57	1.30	1.57	1.30	1.57	1.29
90	1.83	1.54	1.84	1.54	1.83	1.53
60	2.08	1.81	2.08	1.81	2.07	1.80
30	2.27	2.11	2.28	2.11	2.26	2.10
15	2.36	2.28	2.37	2.28	2.35	2.26

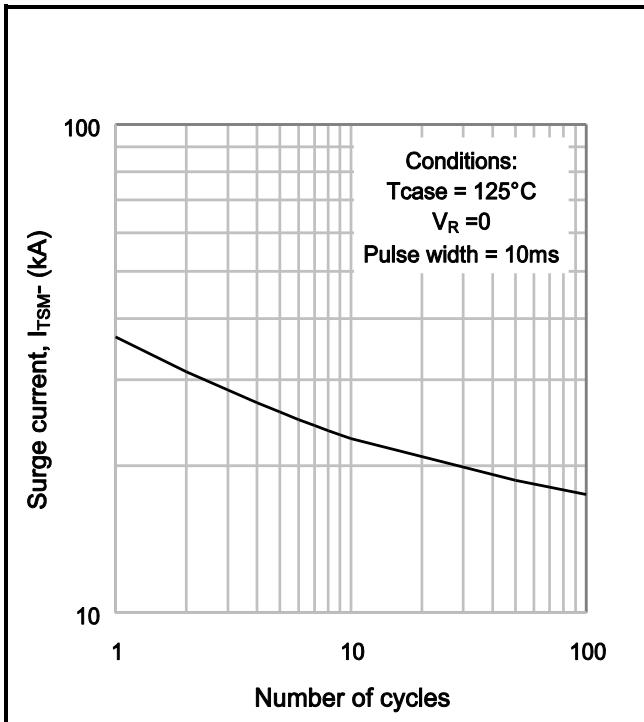


Fig.10 Multi-cycle surge current

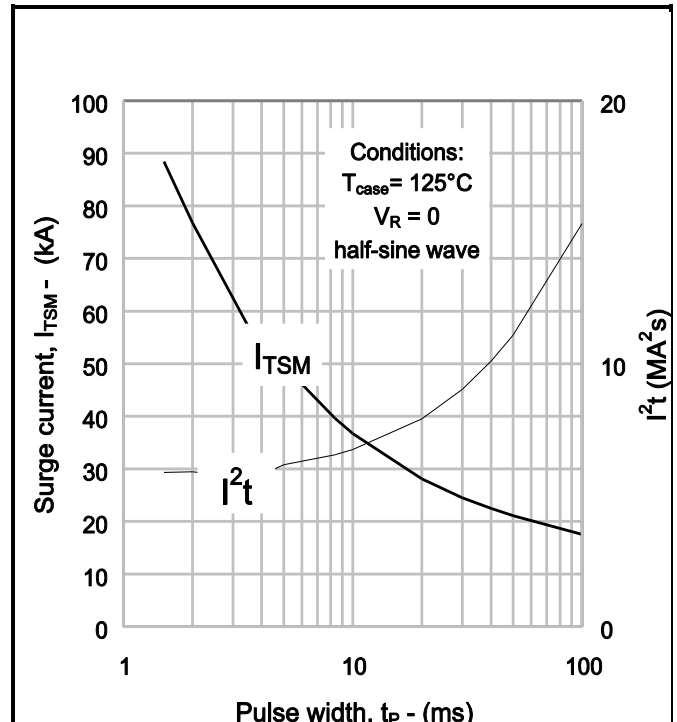


Fig.11 Single-cycle surge current

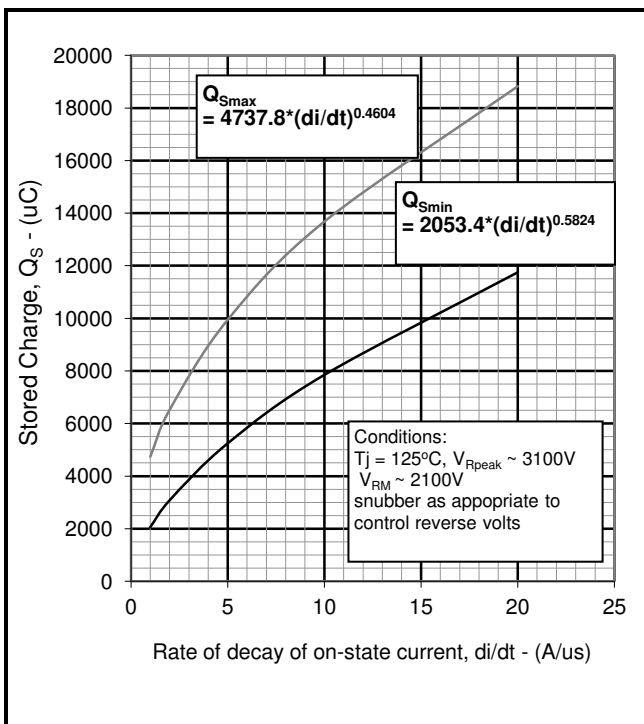


Fig.12 Stored charge

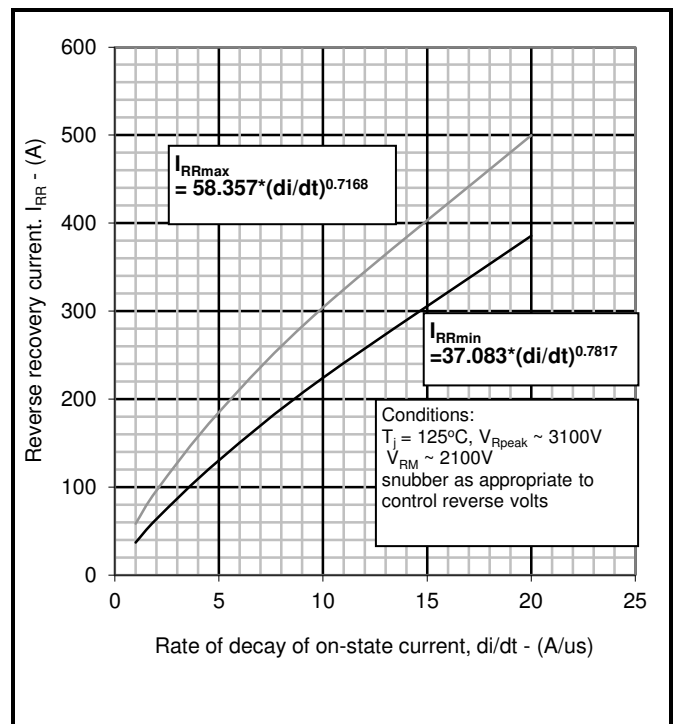


Fig.13 Reverse recovery current

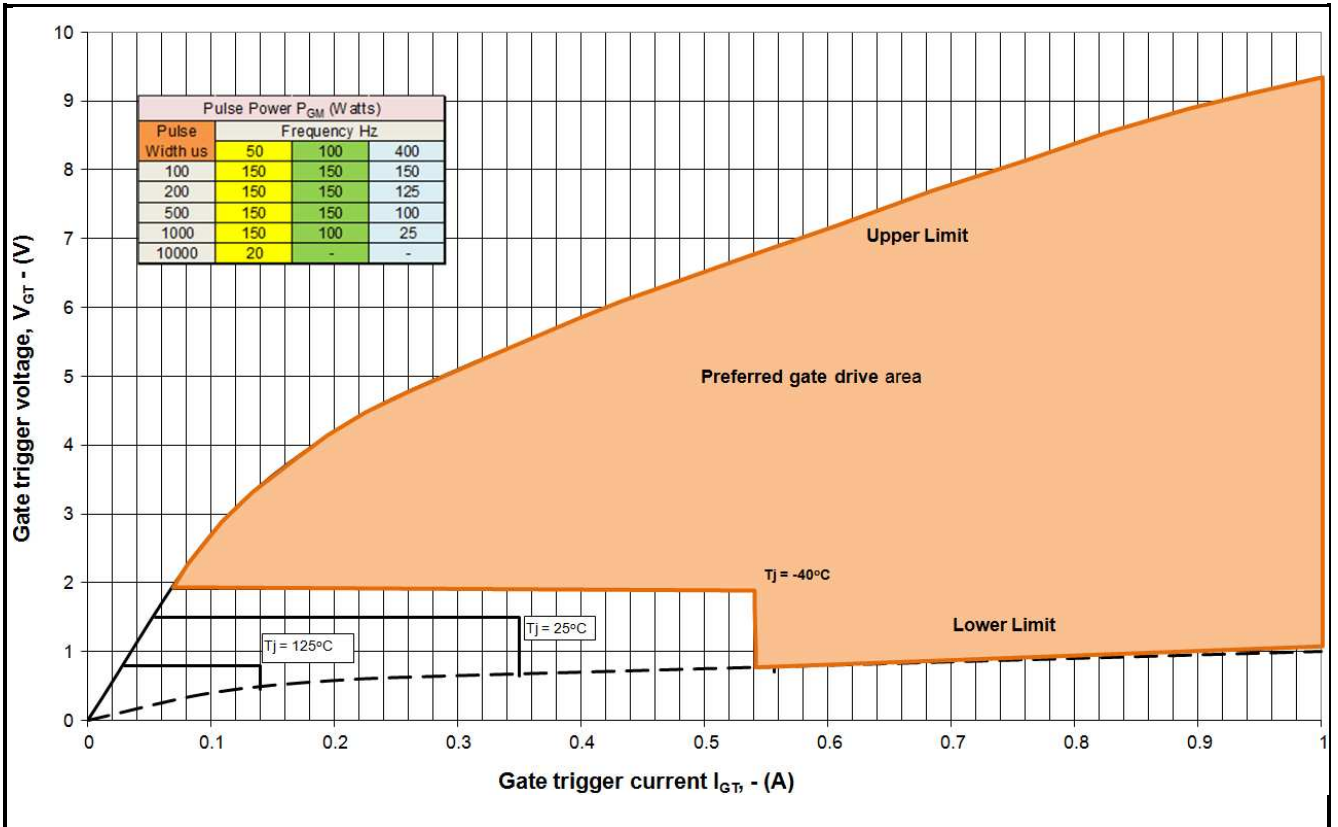


Fig14 Gate Characteristics

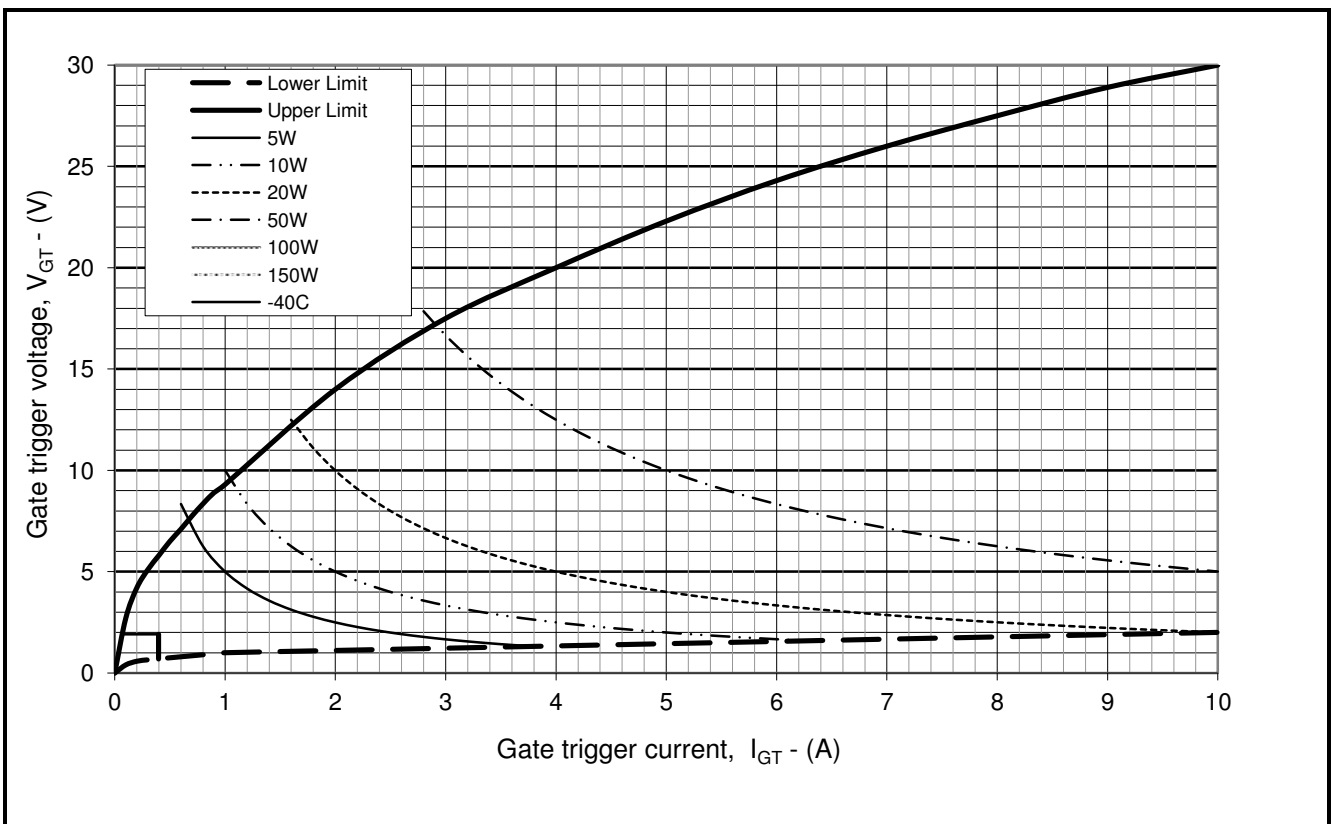
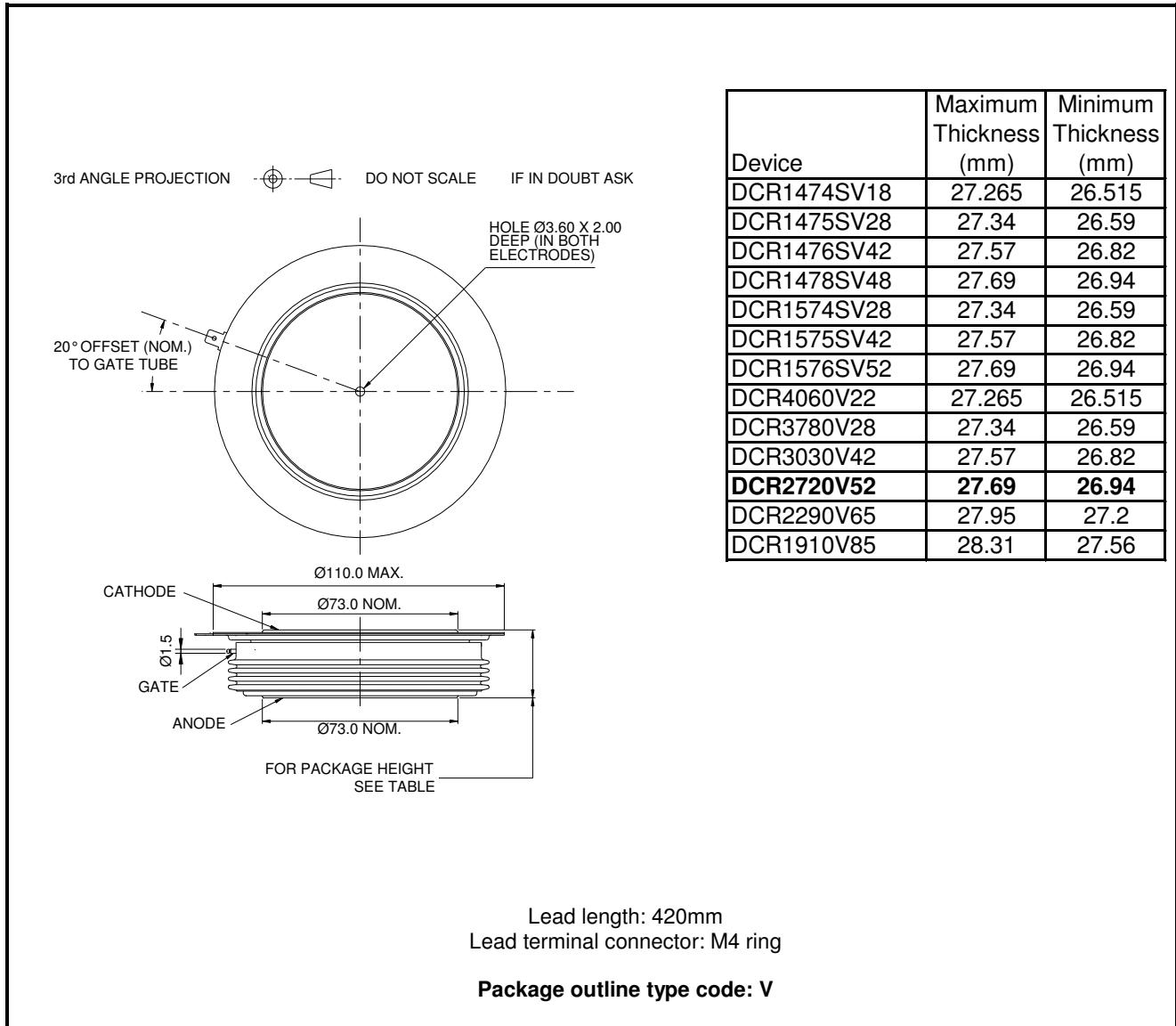


Fig. 15 Gate characteristics

**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**Fig.16 Package outline**

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