



FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- Medium Voltage Soft Starts
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR1020N52* DCR1020N50	5200 4000	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 100\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, V_{DSM} & $V_{RSM} =$ V_{DRM} & $V_{RRM} + 100\text{V}$ respectively

Lower voltage grades available.
*5000V @ -40°C , 5200V @ 0°C

KEY PARAMETERS

V_{DRM}	5200V
$I_{T(AV)}$	1018A
I_{TSM}	14800A
dV/dt^*	1500V/ μs
dI/dt	800A/ μs

* Higher dV/dt selections available

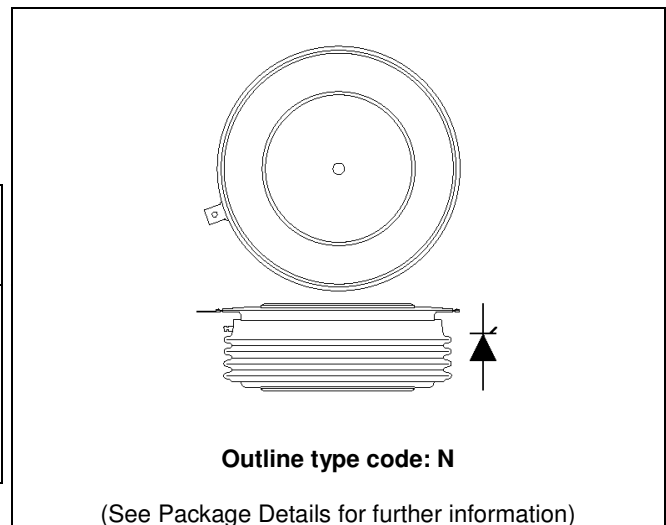


Fig. 1 Package outline

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR1020N52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1018	A
$I_{T(RMS)}$	RMS value	-	1599	A
I_T	Continuous (direct) on-state current	-	1487	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	14.8	kA
I^2t	I^2t for fusing	$V_R = 0$	1.097	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.0221	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.041	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0516	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 23 kN (with mounting compound)	Double side	-	0.004	$^{\circ}\text{C/W}$
			Single side	-	0.008	$^{\circ}\text{C/W}$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}	-	125	$^{\circ}\text{C}$	
T_{stg}	Storage temperature range		-55	125	$^{\circ}\text{C}$	
F_m	Clamping force		20.0	25.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	100	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μ s	
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$	Repetitive 50Hz	-	200	A/ μ s
		Gate source 30V, 10 Ω , $t_r < 0.5\mu$ s, $T_j = 125^{\circ}C$	Non-repetitive	-	800	A/ μ s
$V_{T(TO)}$	Threshold voltage – Low level	300A to 750A at $T_{case} = 125^{\circ}C$	-	0.948	V	
	Threshold voltage – High level	750A to 4000A at $T_{case} = 125^{\circ}C$	-	1.078	V	
r_T	On-state slope resistance – Low level	300A to 750A at $T_{case} = 125^{\circ}C$	-	0.783	m Ω	
	On-state slope resistance – High level	750A to 4000A at $T_{case} = 125^{\circ}C$	-	0.610	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu$ s, $T_j = 25^{\circ}C$	-	3	μ s	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $I_{peak} = 1000A$, $t_p = 1000\mu$ s, $V_{RM} = 100V$, $dI/dt = -5A/\mu$ s, $dV_{DR}/dt = 20V/\mu$ s linear to 2000V		1000	μ s	
I_{RR}	Reverse recovery current	$I_T = 1000A$, $t_p = 1000\mu$ s, $T_j = 125^{\circ}C$, $dI/dt = -5A/\mu$ s, $V_R = 100V$	90	115	A	
Q_S	Stored charge		2200	3800	μ C	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	-	3	A	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V _{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25°C	350	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	15	mA

CURVES

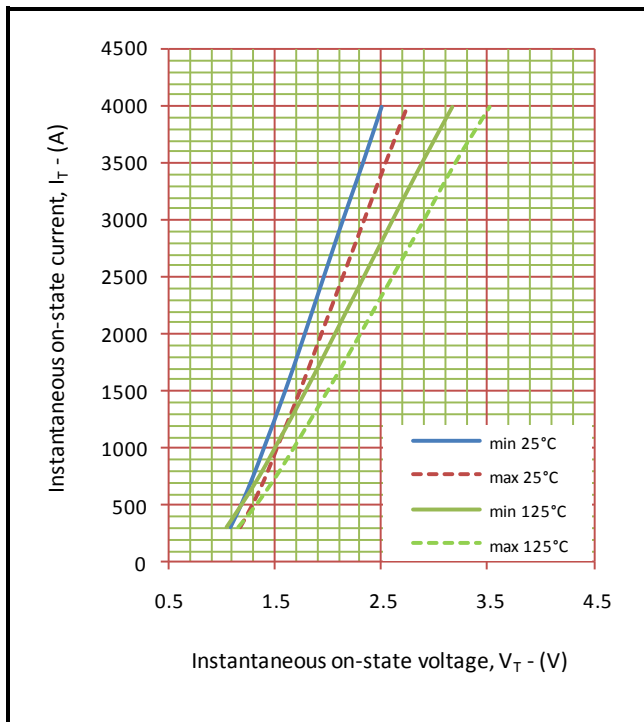


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = -0.069834
 B = 0.220863
 C = 0.000638
 D = -0.013352

these values are valid for T_j = 125°C for I_T 300A to 4000A

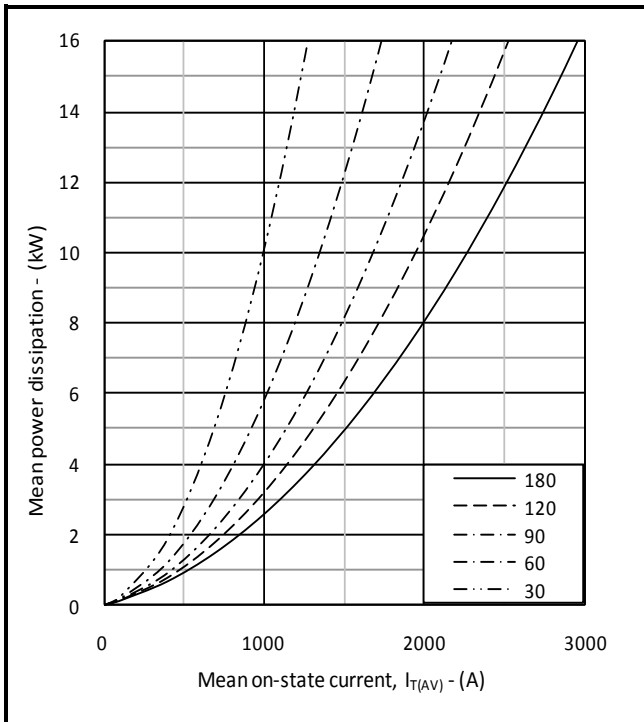


Fig.3 On-state power dissipation – sine wave

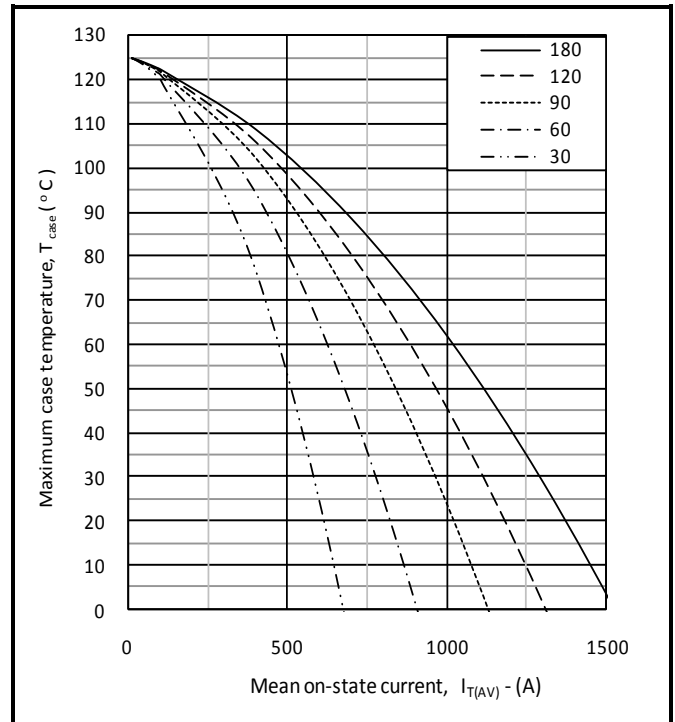


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

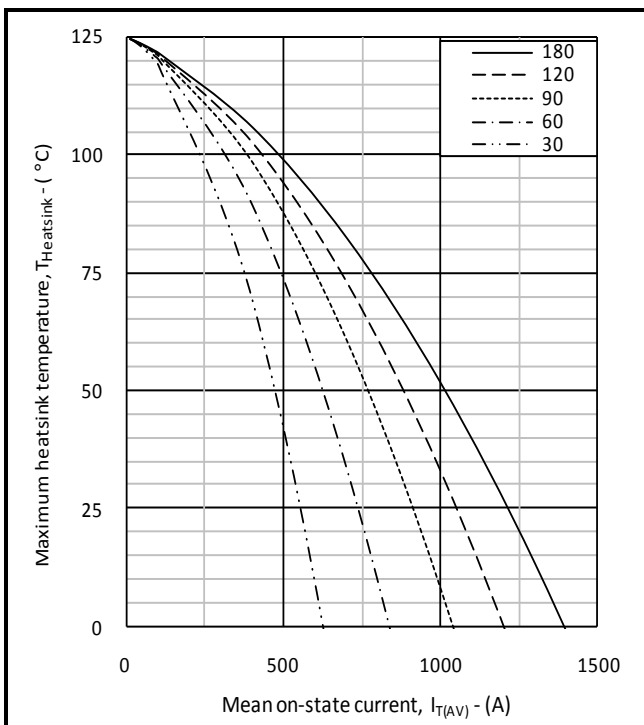


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

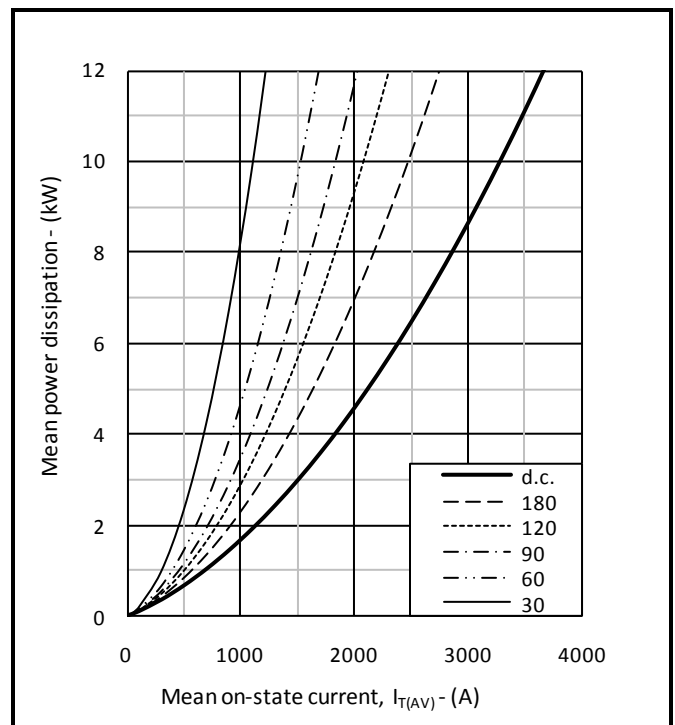


Fig.6 On-state power dissipation – rectangular wave

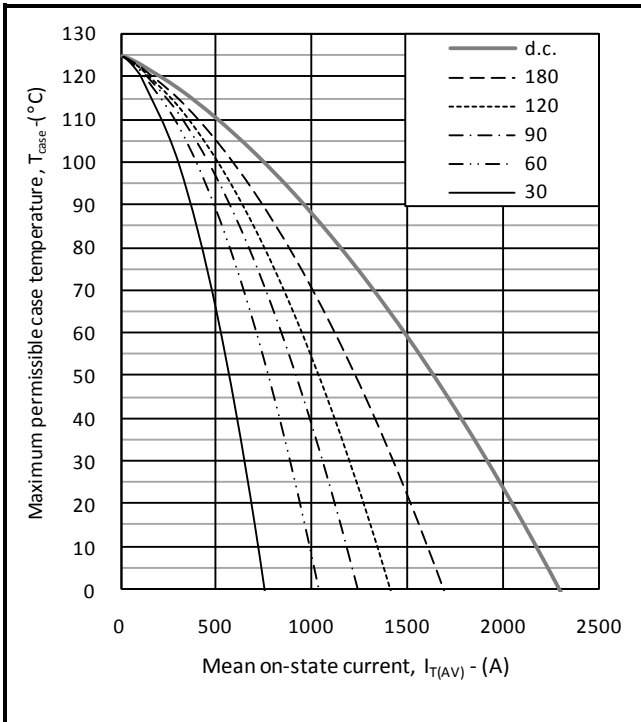


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

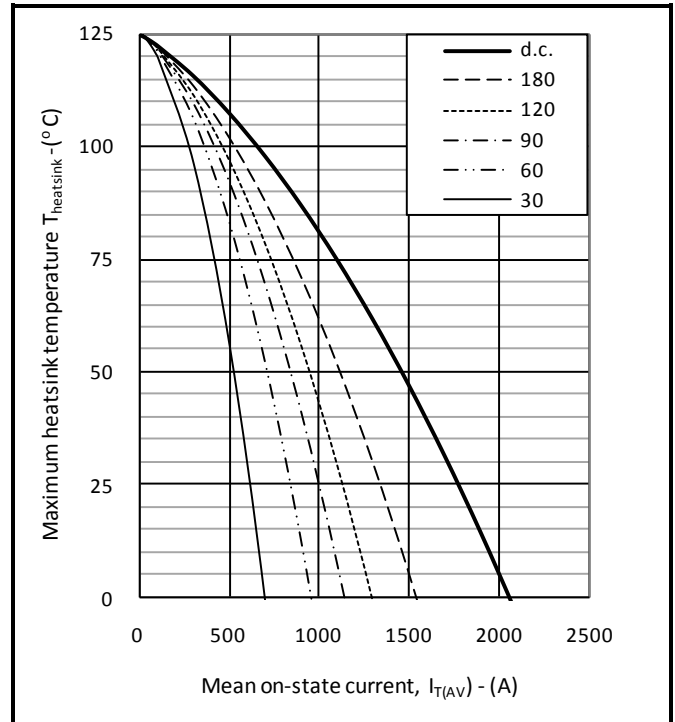


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

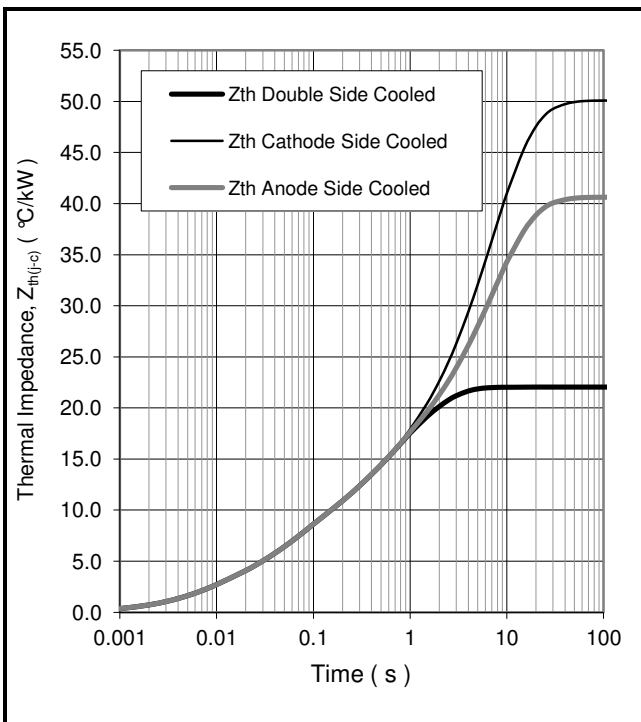


Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

		1	2	3	4
Double side cooled	R _i (°C/kW)	3.4733	4.9047	9.1463	4.5220
	T _i (s)	0.1457	0.0166	1.2832	0.3767
Anode side cooled	R _i (°C/kW)	7.6674	5.0530	9.7355	27.5992
	T _i (s)	0.2241	0.0169	4.0566	8.2780
Cathode side cooled	R _i (°C/kW)	6.0393	4.2782	5.1301	25.0874
	T _i (s)	0.1356	0.0143	0.6594	7.2358

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(-T/T_i))]$$

ΔR_{th(j-c)} Conduction

Tables show the increments of thermal resistance R_{th(j-c)} when the device operates at conduction angles other than d.c.

θ°	Double side cooling		Anode Side Cooling		Cathode Sided Cooling	
	sine.	rect.	sine.	rect.	sine.	rect.
180	3.03	2.07	3.03	2.07	3.12	2.12
120	3.49	2.95	3.49	2.95	3.61	3.04
90	3.99	3.43	3.99	3.43	4.13	3.54
60	4.43	3.94	4.43	3.94	4.60	4.08
30	4.77	4.49	4.76	4.48	4.96	4.66
15	4.92	4.77	4.92	4.77	5.13	4.97

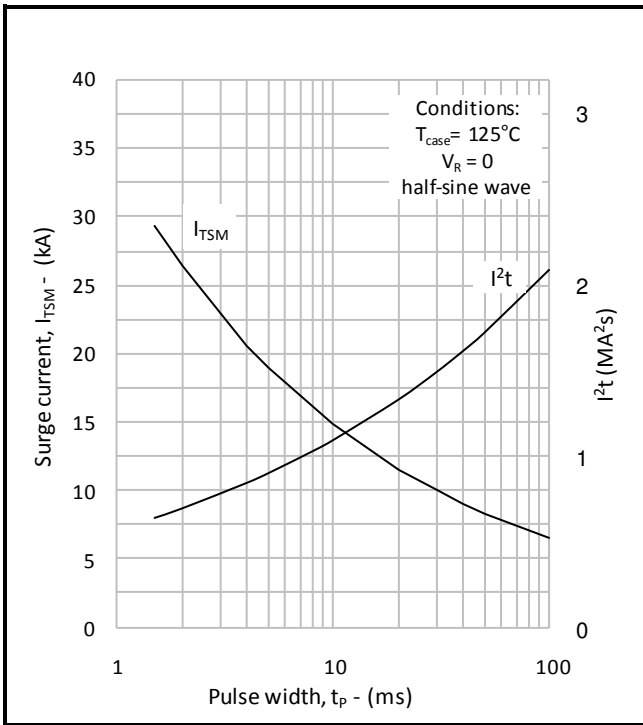


Fig.10 Single-cycle surge current

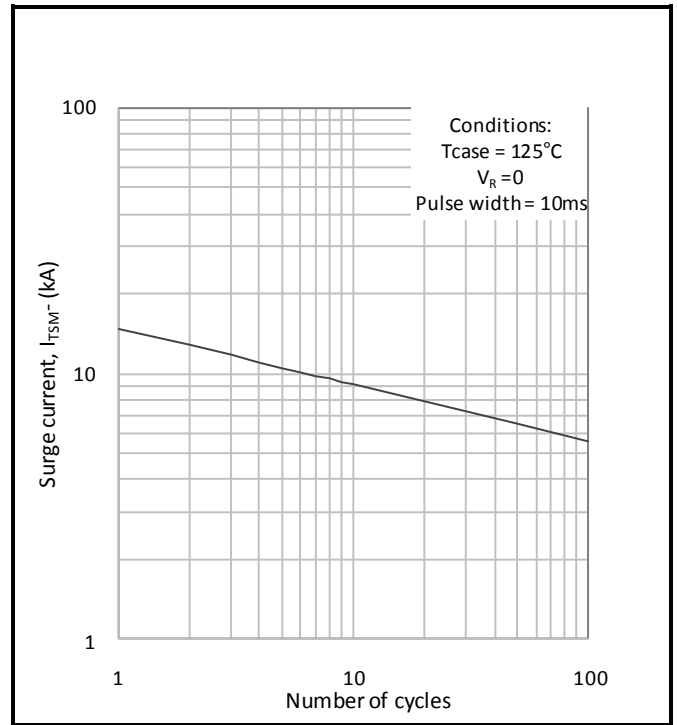


Fig.11 Multi-cycle surge current

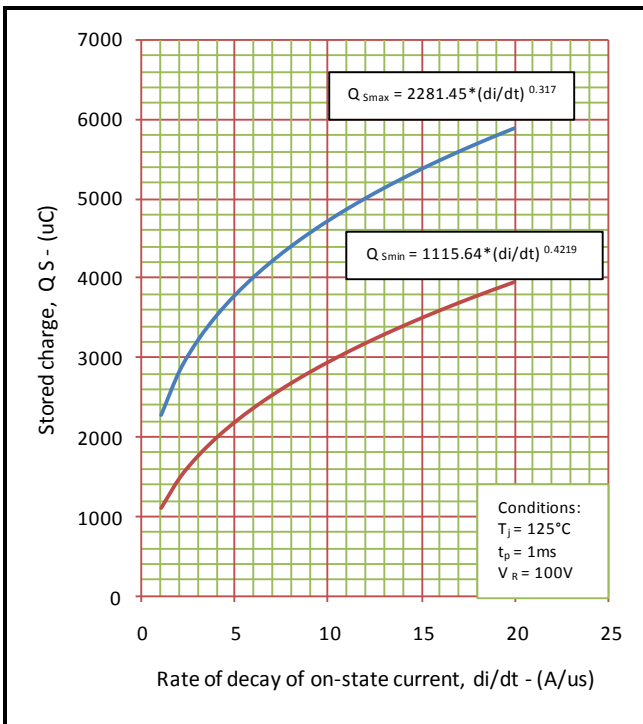


Fig.12 Stored charge

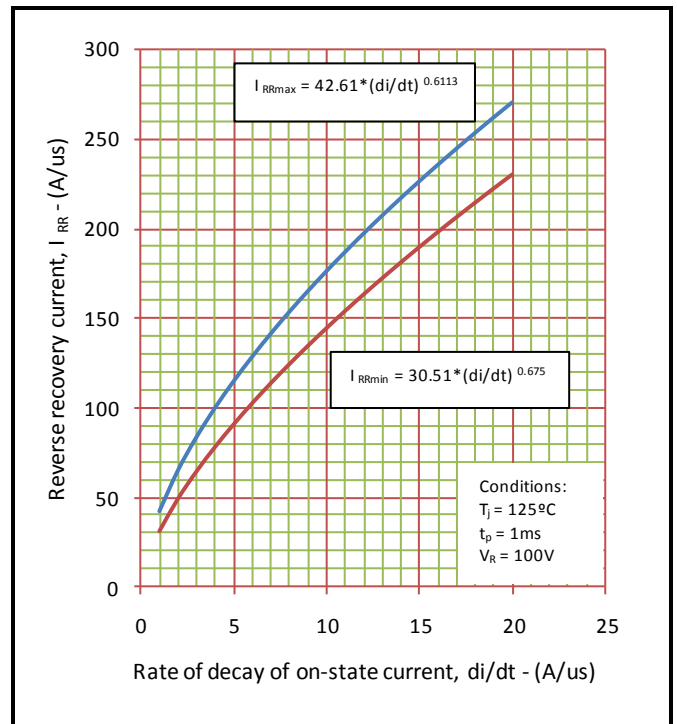


Fig.13 Reverse recovery current

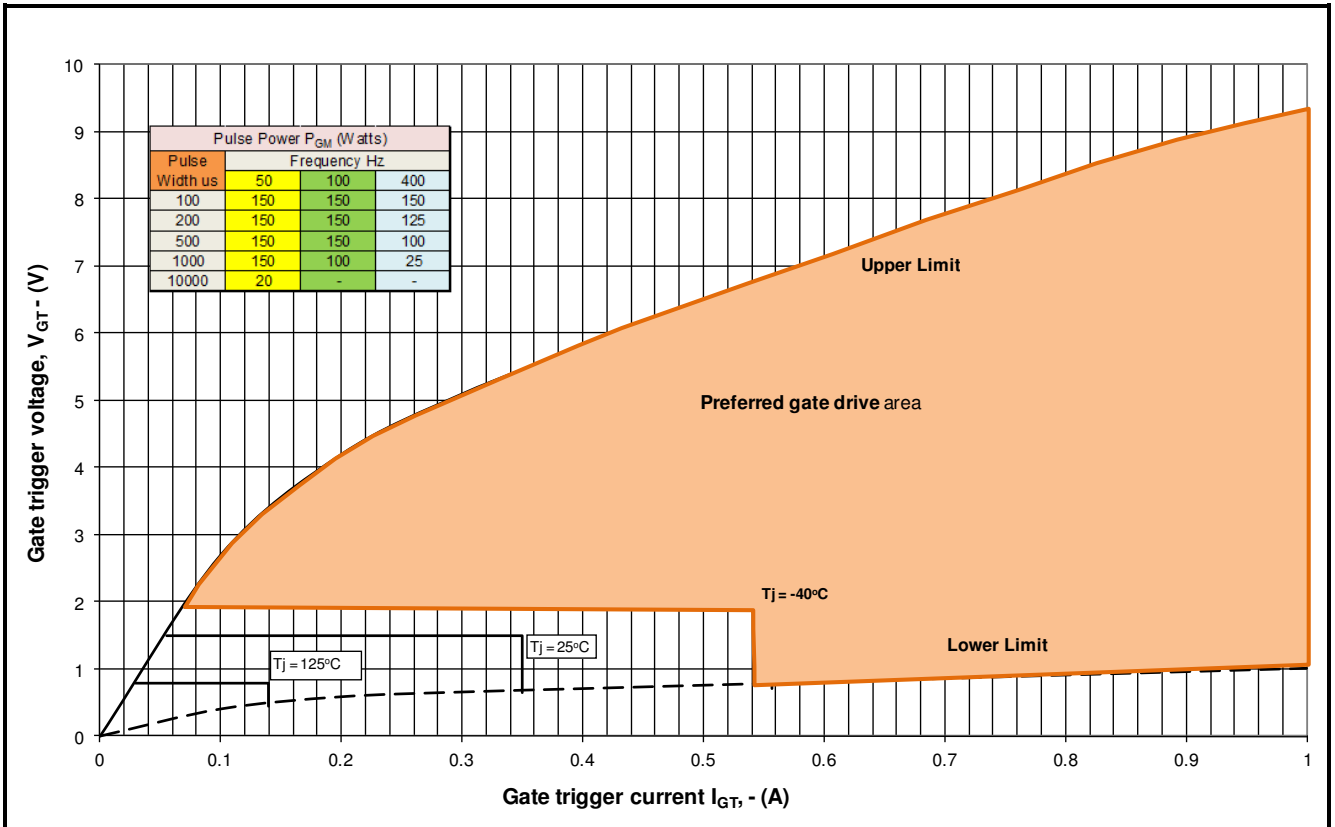


Fig14 Gate Characteristics

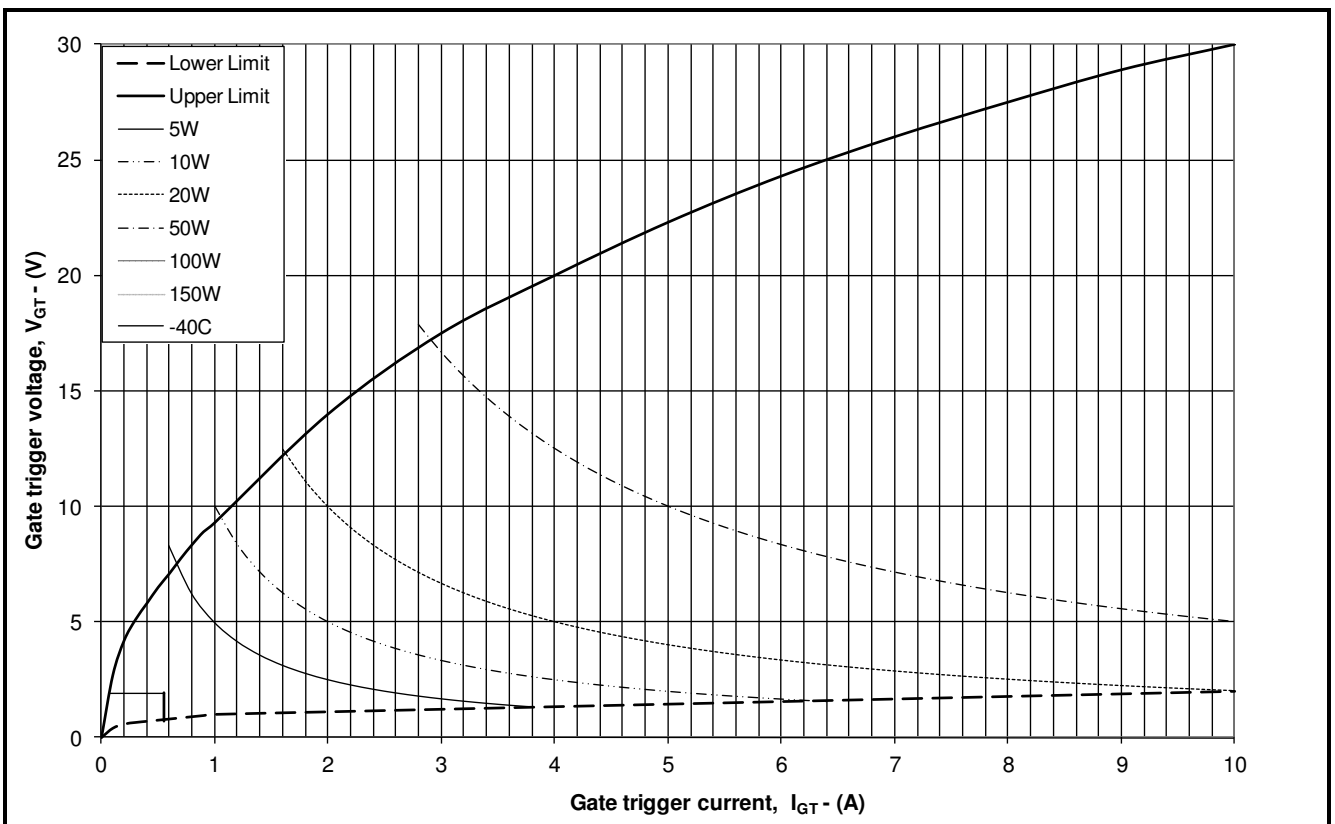


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

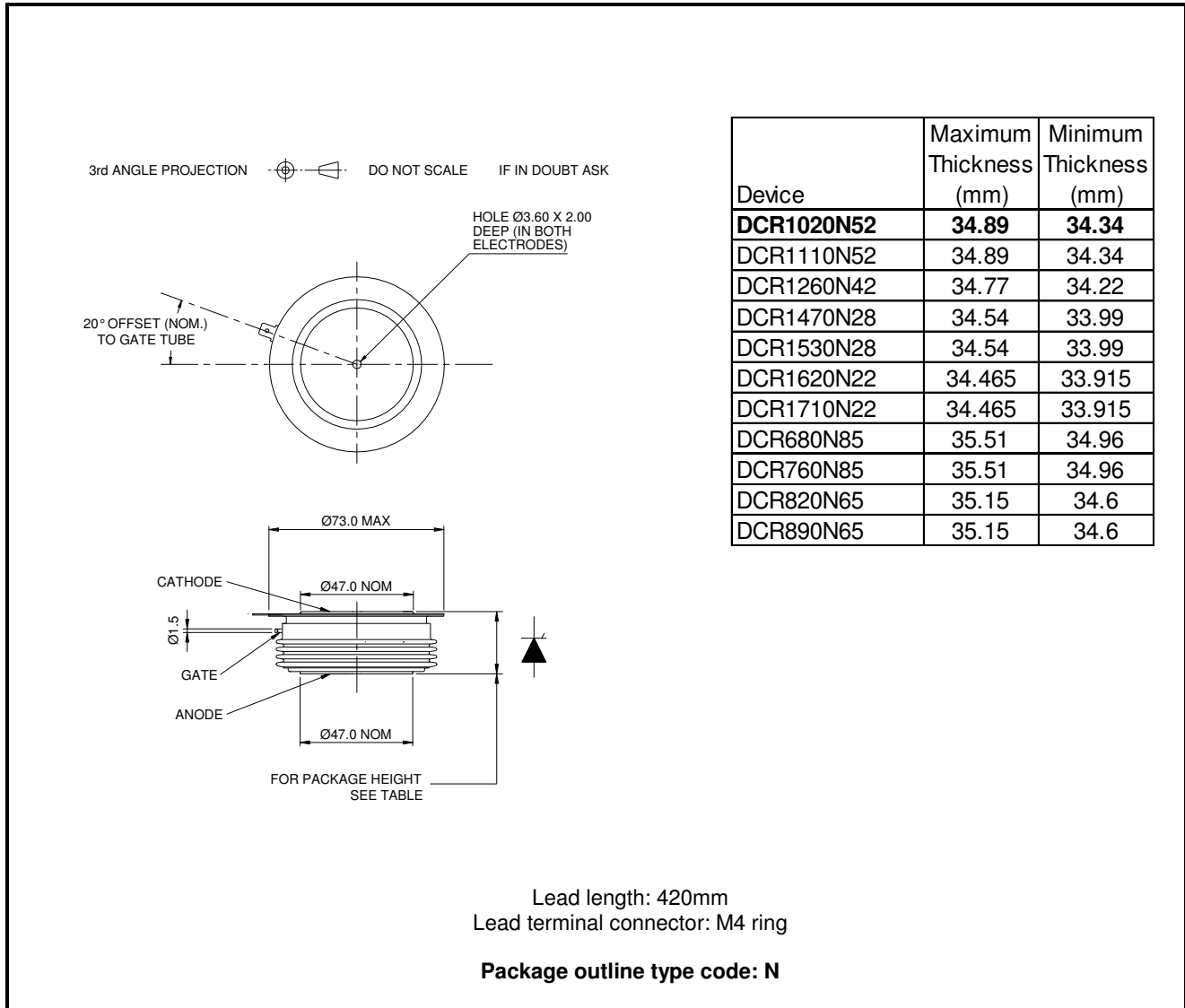


Fig.17 Package outline

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