

### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ V	Conditions
DCR3790B42	4200	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ , $V_{DSM}$ & $V_{RSM} =$ $V_{DRM}$ & $V_{RRM} + 100\text{V}$ respectively
DCR3790B40	4000	
DCR3790B35	3500	
DCR3790B30	3000	

Lower voltage grades available.

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR3790B42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### KEY PARAMETERS

$V_{DRM}$	4200V
$I_{T(AV)}$	3790A
$I_{TSM}$	53500A
$dV/dt^*$	1500V/ $\mu\text{s}$
$dI/dt$	400A/ $\mu\text{s}$

\* Higher  $dV/dt$  selections available

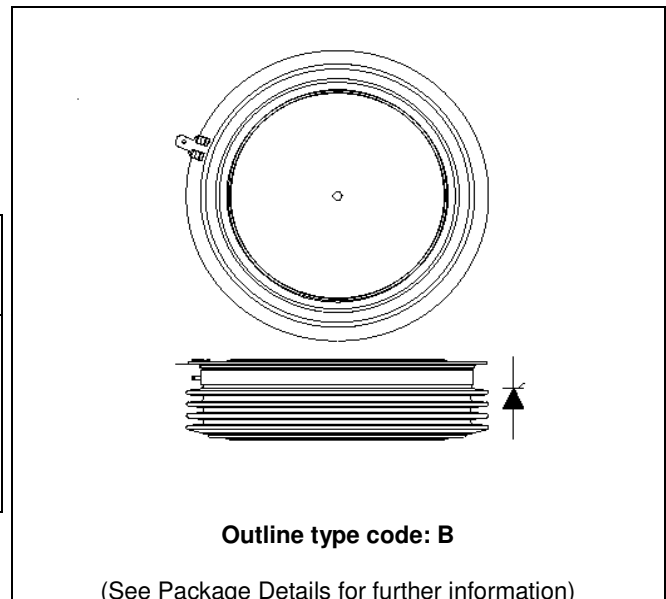


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3790	A
$I_{T(RMS)}$	RMS value	-	5953	A
$I_T$	Continuous (direct) on-state current	-	5330	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$	53.5	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$	14.31	$\text{MA}^2\text{s}$

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.007	$^{\circ}\text{C/W}$
		Single side cooled	Anode DC	-	0.0116	$^{\circ}\text{C/W}$
			Cathode DC	-	0.0181	$^{\circ}\text{C/W}$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 70.0kN (with mounting compound)	Double side	-	0.0014	$^{\circ}\text{C/W}$
			Single side	-	0.0028	$^{\circ}\text{C/W}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		63.0	77.0	kN	

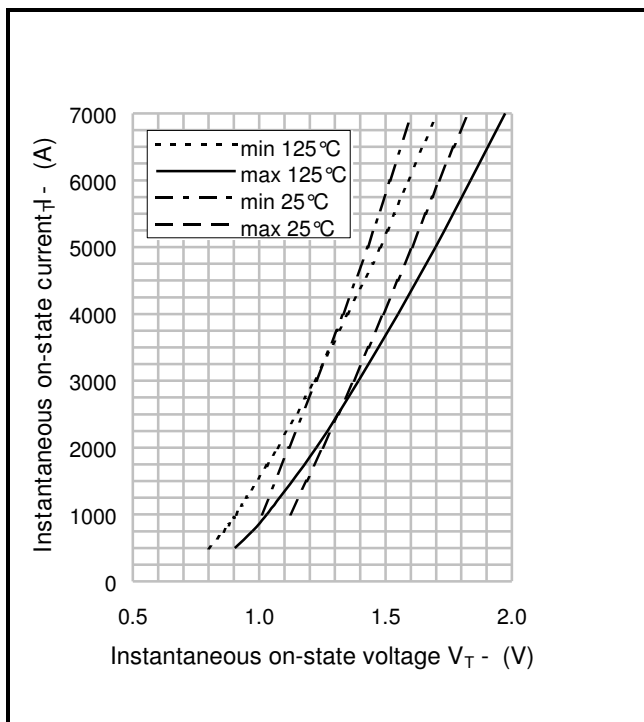
**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_{case} = 125^{\circ}C$	-	200	mA	
$dV/dt$	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^{\circ}C$ , gate open	-	1500	V/ $\mu s$	
$di/dt$	Rate of rise of on-state current	From 67% $V_{DRM}$ to $2x I_{T(AV)}$	Repetitive 50Hz	-	200	A/ $\mu s$
		Gate source 30V, 10 $\Omega$ , $t_r < 0.5\mu s$ , $T_j = 125^{\circ}C$	Non-repetitive	-	400	A/ $\mu s$
$V_{T(TO)}$	Threshold voltage – Low level	700A to 4100A at $T_{case} = 125^{\circ}C$	-	0.83	V	
	Threshold voltage – High level	4100A to 12000A at $T_{case} = 125^{\circ}C$	-	1.0	V	
$r_T$	On-state slope resistance – Low level	700A to 4100A at $T_{case} = 125^{\circ}C$	-	0.1688	m $\Omega$	
	On-state slope resistance – High level	4100A to 12000A at $T_{case} = 125^{\circ}C$	-	0.1263	m $\Omega$	
$t_{gd}$	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$ $t_r = 0.5\mu s$ , $T_j = 25^{\circ}C$	TBD	TBD	$\mu s$	
$t_q$	Turn-off time	$T_j = 125^{\circ}C$ , $V_R = 200V$ , $di/dt = 1A/\mu s$ , $dV_{DR}/dt = 20V/\mu s$ linear	250	500	$\mu s$	
$Q_S$	Stored charge	$I_T = 2000A$ , $T_j = 125^{\circ}C$ , $di/dt = 1A/\mu s$ ,	1500	4500	$\mu C$	
$I_L$	Latching current	$T_j = 25^{\circ}C$ , $V_D = 5V$	-	3	A	
$I_H$	Holding current	$T_j = 25^{\circ}C$ , $R_{G-K} = \infty$ , $I_{TM} = 500A$ , $I_T = 5A$	-	300	mA	

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
V <sub>GD</sub>	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	350	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

**CURVES**



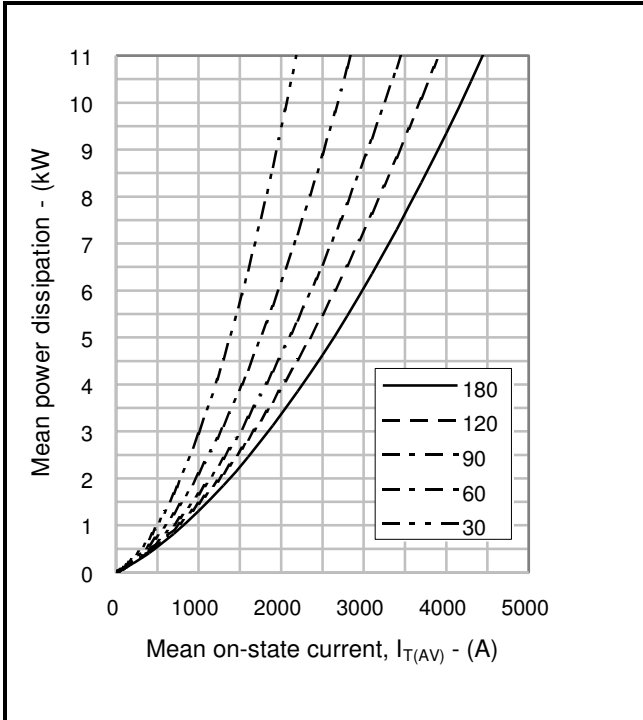
**Fig.2 Maximum & minimum on-state characteristics**

**V<sub>TM</sub> EQUATION**

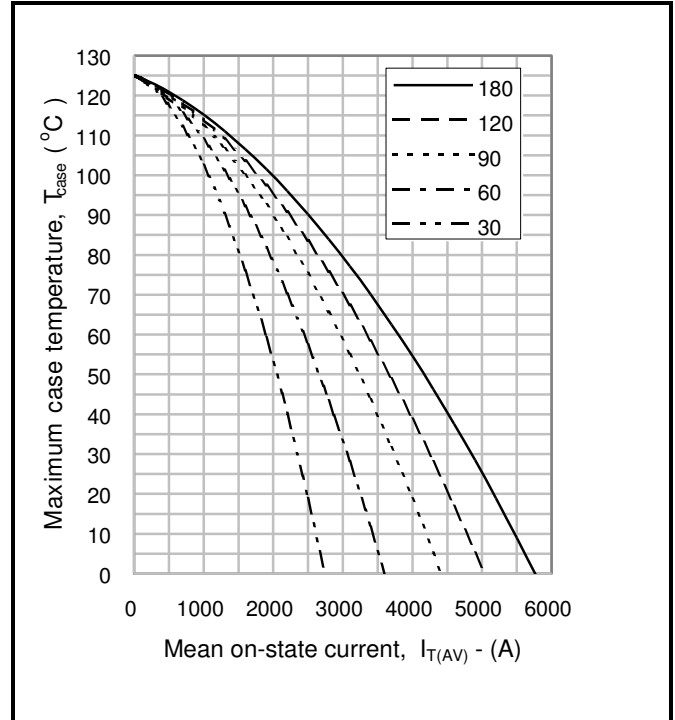
$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.348967  
 B = 0.066851  
 C = 0.000102  
 D = 0.003788

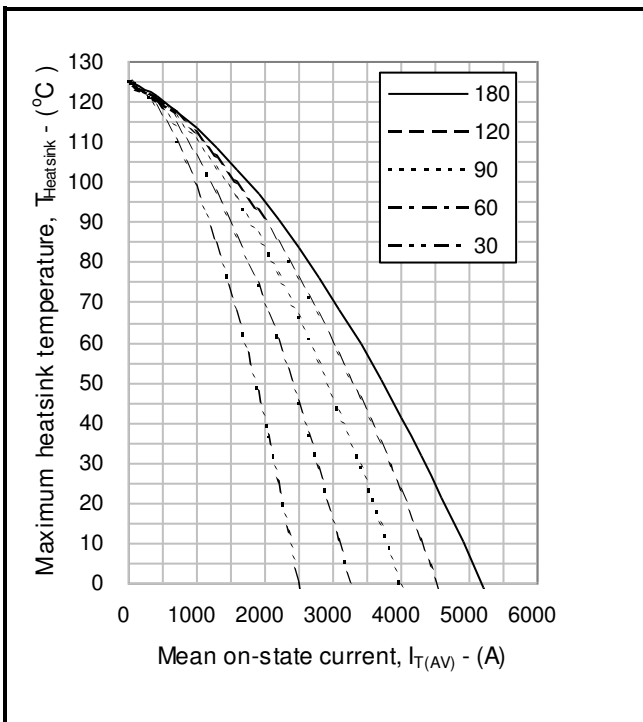
these values are valid for T<sub>j</sub> = 125°C for I<sub>T</sub> 500A to 10000A



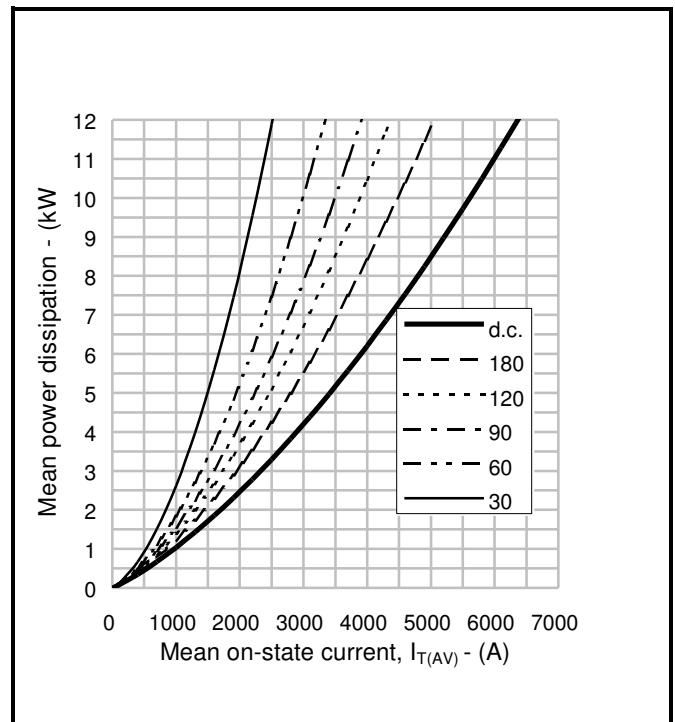
**Fig.3 On-state power dissipation – sine wave**



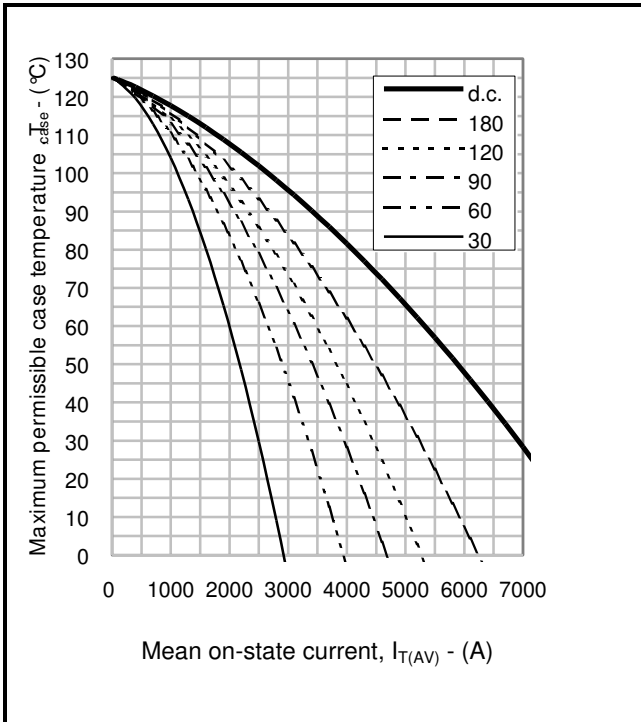
**Fig.4 Maximum permissible case temperature, double side cooled – sine wave**



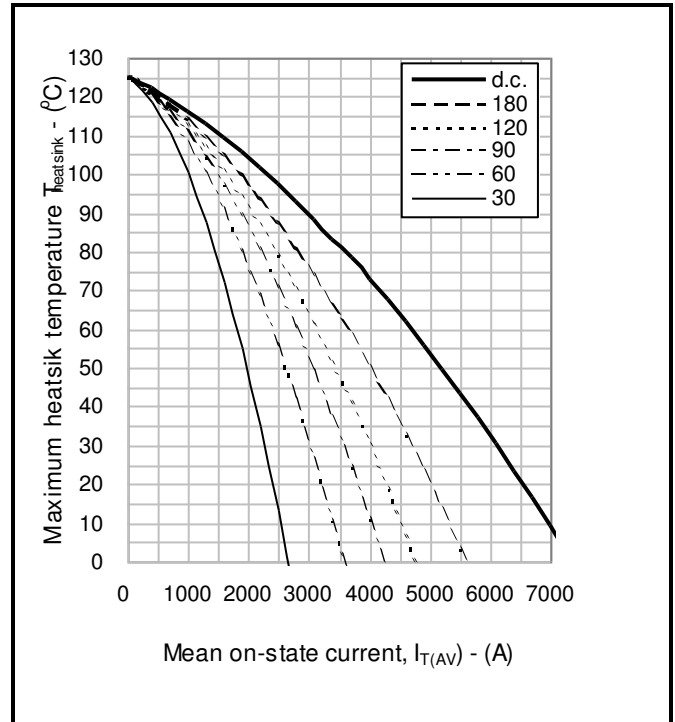
**Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave**



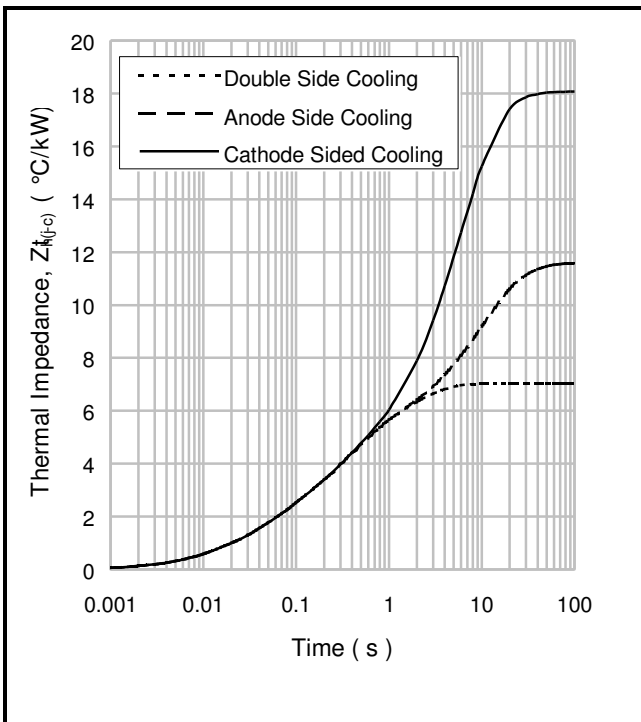
**Fig.6 On-state power dissipation – rectangular wave**



**Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave**



**Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave**



**Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)**

		1	2	3	4
Double side cooled	R <sub>l</sub> (°C/kW)	0.502	1.333	2.9559	2.2335
	T <sub>l</sub> (s)	0.0137081	0.0548877	0.3311925	1.6905
Anode side cooled	R <sub>l</sub> (°C/kW)	1.3035	3.138	1.1859	5.9136
	T <sub>l</sub> (s)	0.0251065	0.2410256	1.0806	11.002
Cathode side cooled	R <sub>l</sub> (°C/kW)	1.2616	2.6216	13.3603	0.8304
	T <sub>l</sub> (s)	0.0245837	0.2005035	5.7854	16.765

$$Z_{th} = \sum [R_l \times (1 - \exp.(-t/t_l))] \quad [1]$$

**ΔR<sub>th(j-c)</sub> Conduction**

Tables show the increments of thermal resistance R<sub>th(j-c)</sub> when the device operates at conduction angles other than d.c.

θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.
180	0.70	0.48
120	0.80	0.68
90	0.90	0.78
60	1.00	0.89
30	1.07	1.01
15	1.10	1.07

θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.
180	0.67	0.47
120	0.77	0.66
90	0.87	0.75
60	0.95	0.86
30	1.02	0.96
15	1.05	1.02

θ°	ΔZ <sub>th</sub> (z)	
	sine.	rect.
180	0.67	0.47
120	0.77	0.66
90	0.87	0.76
60	0.95	0.86
30	1.02	0.96
15	1.05	1.02

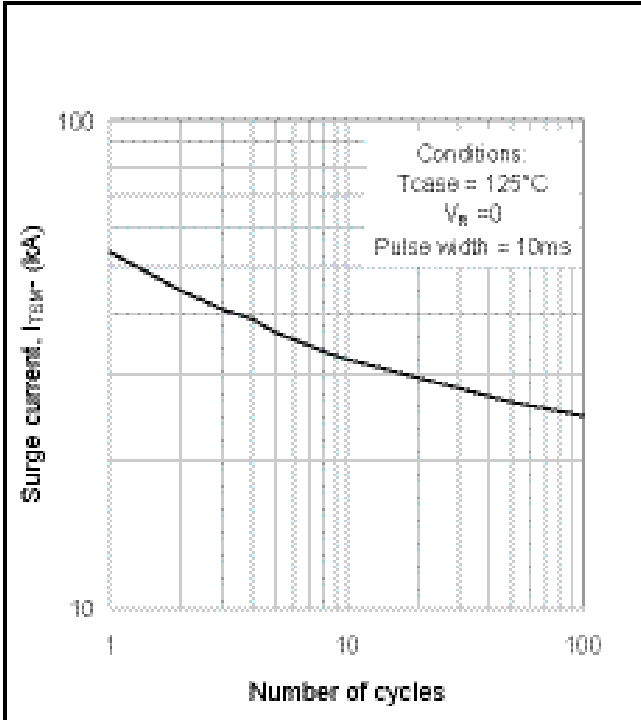


Fig.10 Multi-cycle surge current

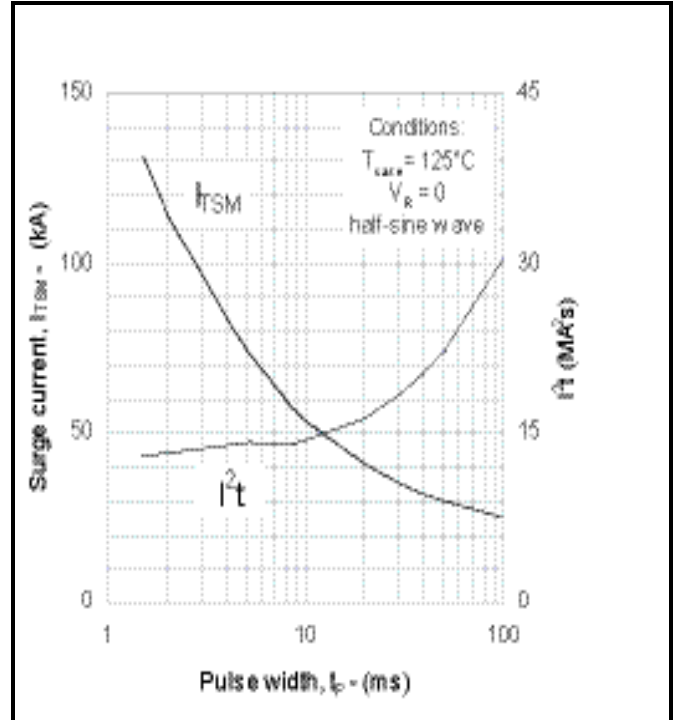


Fig.11 Single-cycle surge current

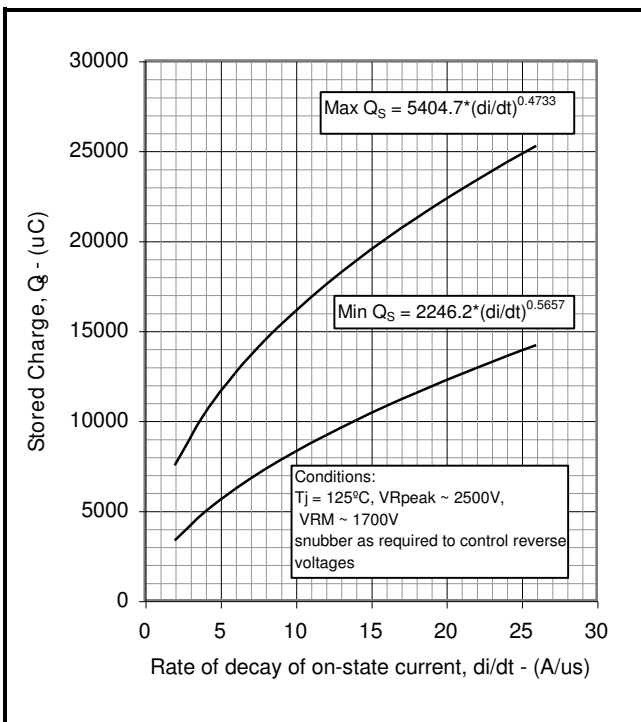


Fig.12 Stored charge

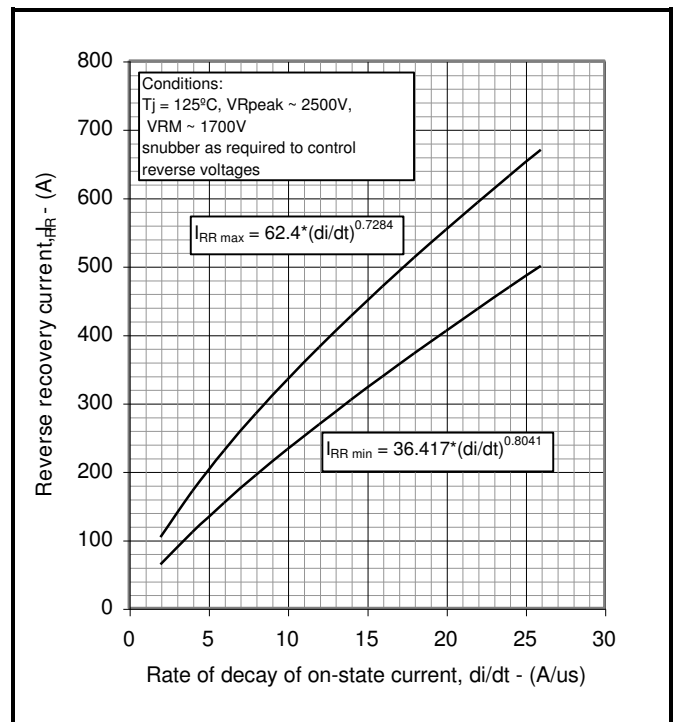


Fig.13 Reverse recovery current

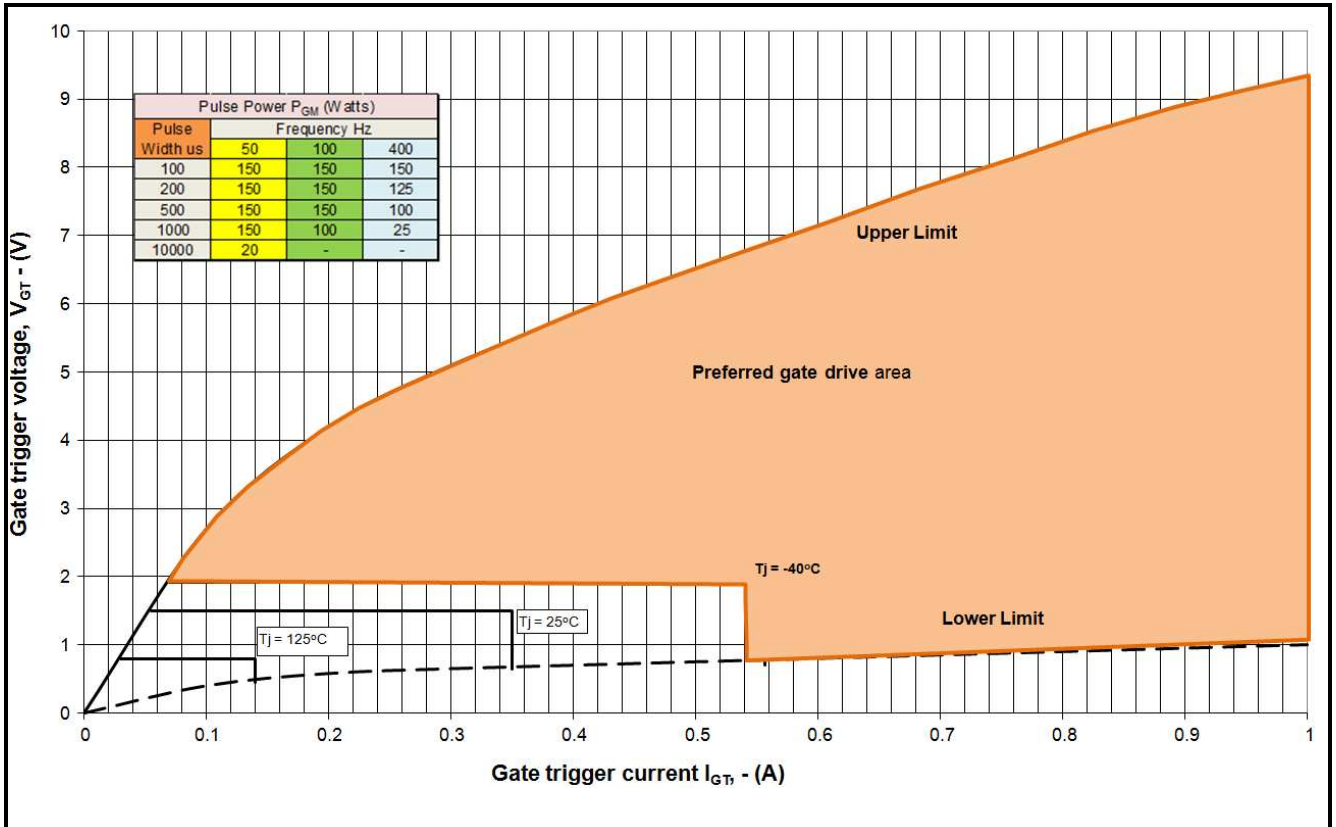


Fig14 Gate Characteristics

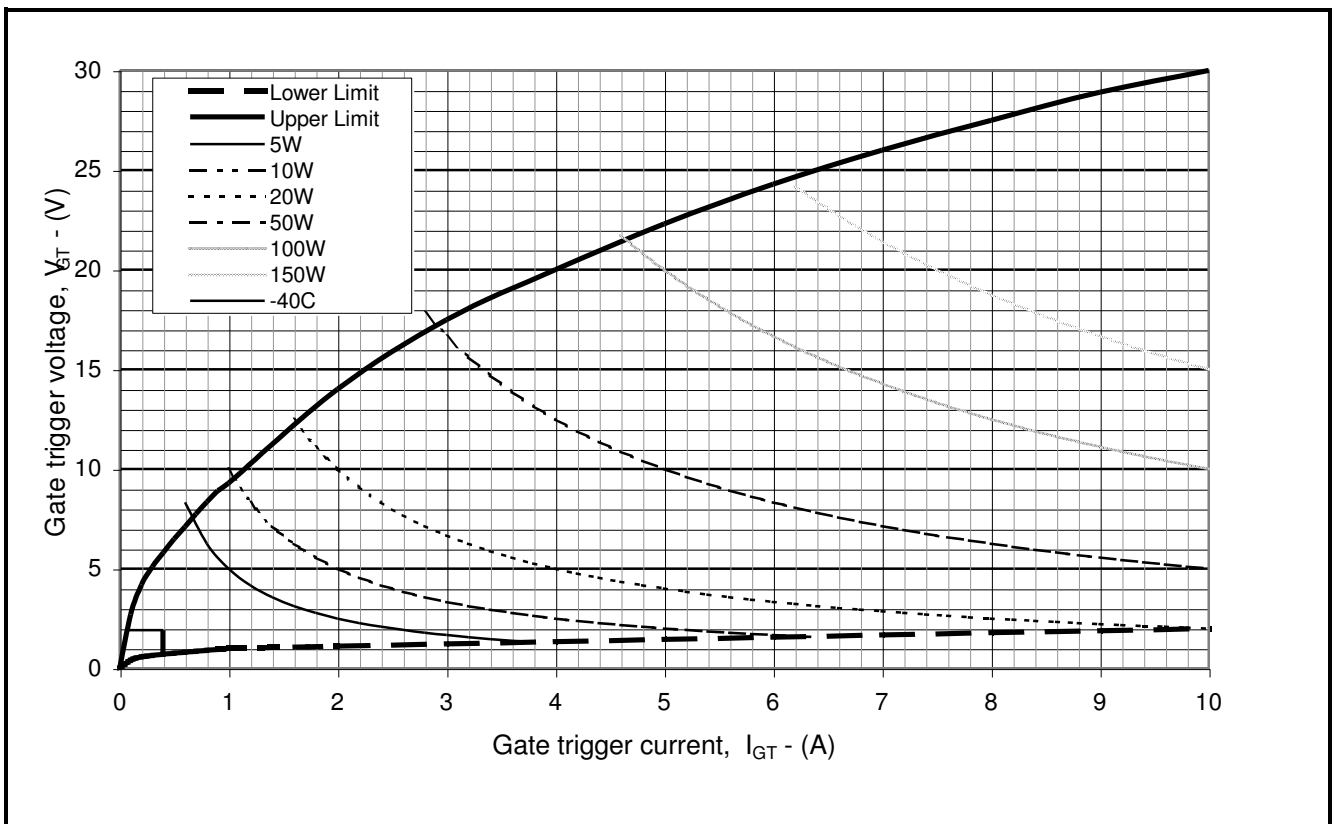
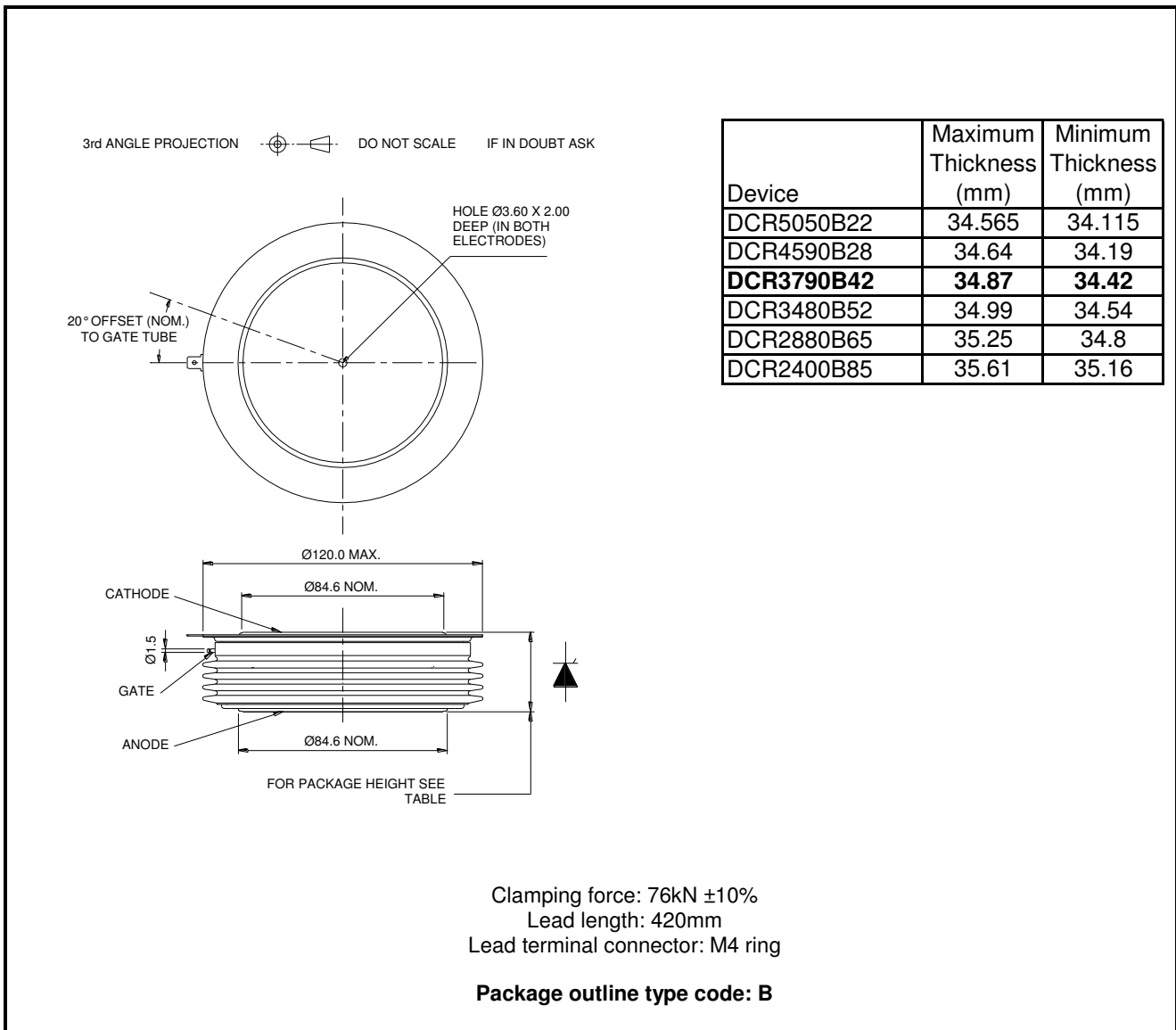


Fig. 15 Gate characteristics

**PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**Fig.16 Package outline**

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