

# AK632512AW - 64 Pin Version

## 524,288 x 32 Bit CMOS / BiCMOS

### Static Random Access Memory

#### DESCRIPTION

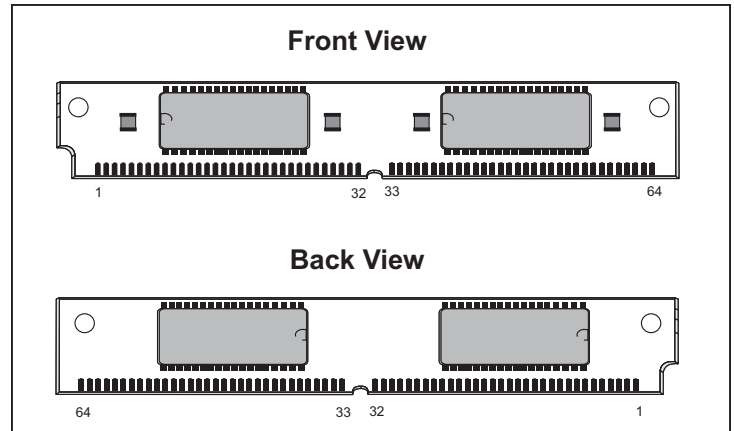
The Accutek AK632512AW SRAM Module consists of fast high performance SRAMs mounted on a low height, 64 pin SIM Board. The module utilizes four 36 pin 512K x 8 SRAMs in 400 mil SOJ packages and four decoupling capacitors mounted two on the front side and two on the back side of a printed circuit board.

The SRAMs used have common I/O functions and single output enable functions. Also, four separate chip select ( $\overline{CE}$ ) connections are used to independently enable the four bytes. The modules can be supplied in a variety of access time values from 15 nSEC to 35 nSEC in CMOS or BiCMOS technology.

The Accutek module is designed to have a maximum seated height of 0.640 inch SIM to provide for the lowest height off the board. The module conforms to JEDEC-standard size. The Presence Detect feature has been disabled on this 64 pin module. The customer must jumper his board to provide density identification. The available 72 pin module has the Presence Detect feature operational.

#### FEATURES

- 524,288 x 32 bit organization
- Similar to JEDEC standard 64 pin SIM format except that A18 replaces PD<sub>1</sub> on Pin #3
- Common I/O, single  $\overline{OE}$  and  $\overline{WE}$  functions with four separate chip selects ( $\overline{CE}$ )
- Fast access times from 15 nSEC
- Low height, 0.640 inch SIM maximum
- Power:
  - 720mA Max Active (20 nSEC)
  - 760mA Max Active (15 nSEC)
  - 800mA Max Active (12 nSEC)
  - 200mA Max Standby



- Presence Detect, PD<sub>0</sub> is open for identifying module density
- Downward compatible with 256K x 32 (AK632256), 128K x 32 (AK632128), 64K x 32 (AK63264) and 32K x 32 (AK63232), 64 pin SIM or ZIP designs
- Upward compatible with 1 Meg x 32 (AK6321024)
- TTL-compatible inputs and outputs
- Single 5 volt power supply - AK632512AW
- Single 3.3 volt power supply - AK632512AW/3.3
- Operating free air temperature 0° to 70°C

#### ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 512K x 8 SRAMs used to construct these modules. Accutek's module design allows the flexibility of selecting industry-compatible 512K x 8 SRAMs from several SRAM manufacturers.

#### PIN NOMENCLATURE

A <sub>0</sub> - A <sub>18</sub>	Address Inputs
$\overline{CE}_1$ - $\overline{CE}_4$	Chip Enable
DQ <sub>1</sub> - DQ <sub>32</sub>	Data In/Data Out
$\overline{OE}$	Output Enable
PD <sub>0</sub>	Presence Detect
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
$\overline{WE}$	Write Enable

#### MODULE OPTIONS

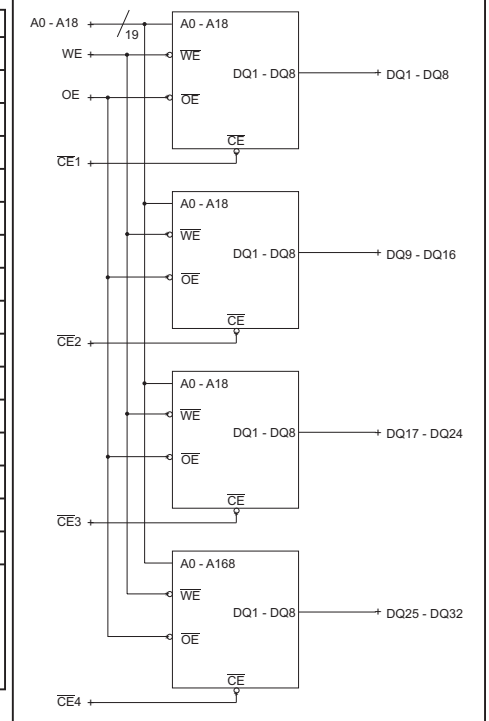
Leadless SIM: AK632512AW

#### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>ss</sub>	17	A <sub>2</sub>	33	$\overline{CE}_4$	49	A <sub>4</sub>
2	PD <sub>0</sub>	18	A <sub>9</sub>	34	$\overline{CE}_3$	50	A <sub>11</sub>
3	A <sub>18</sub>	19	DQ <sub>13</sub>	35	A <sub>17</sub>	51	A <sub>5</sub>
4	DQ <sub>1</sub>	20	DQ <sub>5</sub>	36	A <sub>16</sub>	52	A <sub>12</sub>
5	DQ <sub>9</sub>	21	DQ <sub>14</sub>	37	$\overline{OE}$	53	V <sub>cc</sub>
6	DQ <sub>2</sub>	22	DQ <sub>6</sub>	38	V <sub>ss</sub>	54	A <sub>13</sub>
7	DQ <sub>10</sub>	23	DQ <sub>15</sub>	39	DQ <sub>25</sub>	55	A <sub>6</sub>
8	DQ <sub>3</sub>	24	DQ <sub>7</sub>	40	DQ <sub>17</sub>	56	D <sub>21</sub>
9	DQ <sub>11</sub>	25	DQ <sub>16</sub>	41	DQ <sub>26</sub>	57	DQ <sub>29</sub>
10	DQ <sub>4</sub>	26	DQ <sub>8</sub>	42	DQ <sub>18</sub>	58	DQ <sub>22</sub>
11	DQ <sub>12</sub>	27	V <sub>ss</sub>	43	DQ <sub>27</sub>	59	DQ <sub>30</sub>
12	V <sub>cc</sub>	28	$\overline{WE}$	44	DQ <sub>19</sub>	60	DQ <sub>23</sub>
13	A <sub>0</sub>	29	A <sub>15</sub>	45	DQ <sub>28</sub>	61	DQ <sub>31</sub>
14	A <sub>7</sub>	30	A <sub>14</sub>	46	DQ <sub>20</sub>	62	DQ <sub>24</sub>
15	A <sub>1</sub>	31	$\overline{CE}_2$	47	A <sub>3</sub>	63	DQ <sub>32</sub>
16	A <sub>8</sub>	32	$\overline{CE}_1$	48	A <sub>10</sub>	64	V <sub>ss</sub>

PD<sub>0</sub> = Open

#### FUNCTIONAL DIAGRAM



## ORDERING INFORMATION

## PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8																				
<b>1 Product</b>	<b>AK = Accuthek Memory</b>																											
<b>2 Type</b>	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM																											
<b>3 Organization/Word Width</b>	1 = by 1    16 = by 16 4 = by 4    32 = by 32 8 = by 8    36 = by 36 9 = by 9																											
<b>4 Size/Bits Depth</b>	64 = 64K      4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG    16384 = 16 MEG																											
<b>5 Package Type</b>	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)																											
<b>6 Special Designation</b>	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram																											
<b>7 Separator</b>	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In																											
<b>8 Speed (first two significant digits)</b>	<table border="0"> <tr> <td>DRAMS</td> <td>SRAMS</td> <td></td> <td></td> </tr> <tr> <td>50 = 50 nS</td> <td>8 = 8 nS</td> <td></td> <td></td> </tr> <tr> <td>60 = 60 nS</td> <td>10 = 10 nS</td> <td></td> <td></td> </tr> <tr> <td>70 = 70 nS</td> <td>12 = 12 nS</td> <td></td> <td></td> </tr> <tr> <td>80 = 80 nS</td> <td>15 = 15 nS</td> <td></td> <td></td> </tr> </table>								DRAMS	SRAMS			50 = 50 nS	8 = 8 nS			60 = 60 nS	10 = 10 nS			70 = 70 nS	12 = 12 nS			80 = 80 nS	15 = 15 nS		
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The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

## EXAMPLES:

**AK632512AW-15**

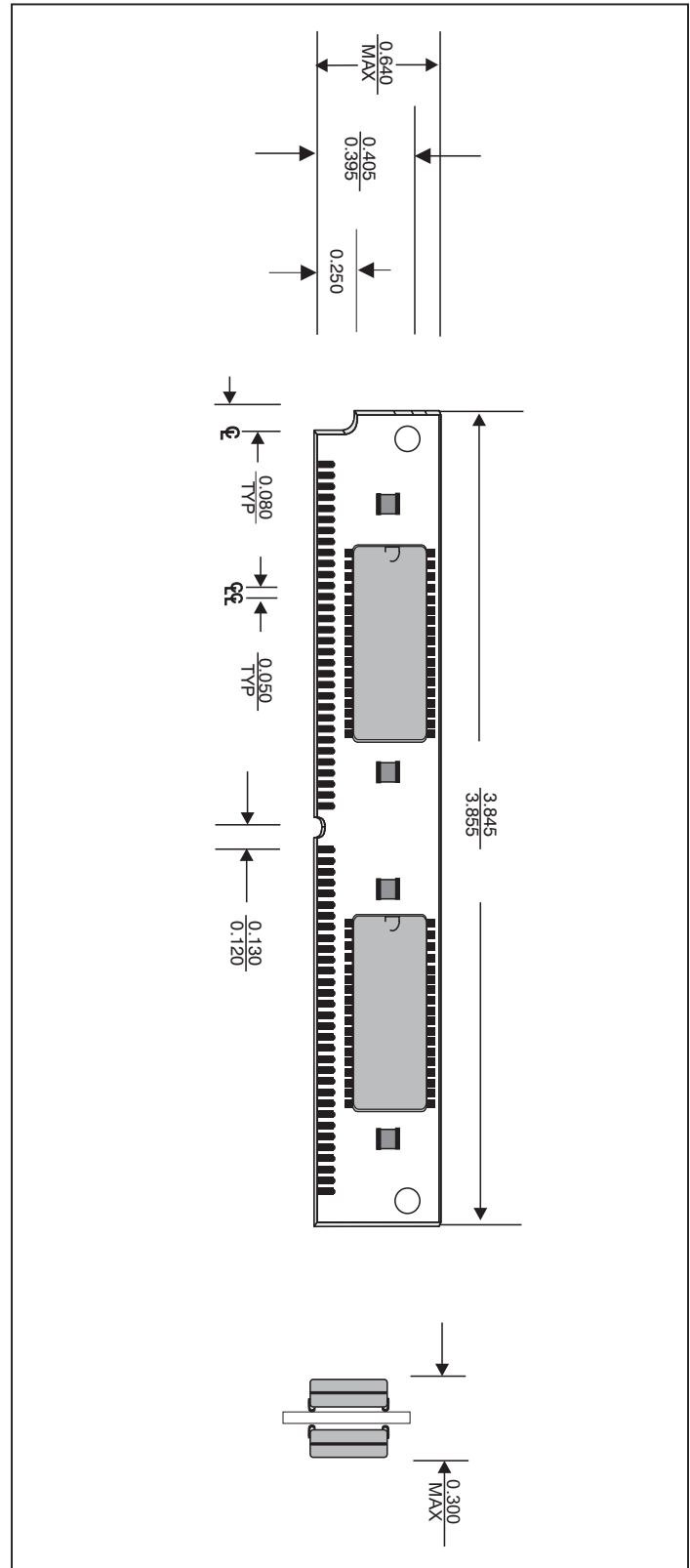
512K x 32, 15 nSEC SRAM Module, SIM Configuration, 64 Pin



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Internet: www.accutekmicro.com

## MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.