

AK68512D

524,288 x 8 Bit CMOS

Static Random Access Memory

DESCRIPTION

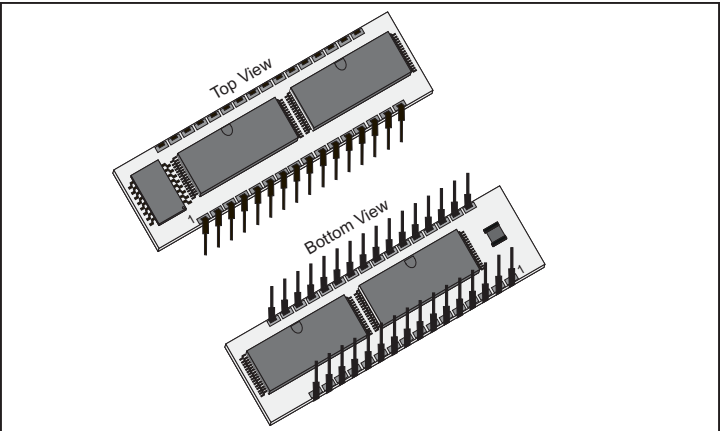
The Accuthek AK68512D high density memory module is a static random access memory organized in 512K x 8 bit words. The assembly consists of two medium speed 128K x 8 SRAMs in thin TSOP packages and a CMOS decoder logic IC mounted on the top side and two medium speed 128K x 8 SRAMs in thin TSOP packages mounted on the bottom surfaces of a printed circuit board. The module is supplied in a 600 mil wide, 32 pin DIP (Dual In-Line Package) configuration. This pinout is completely compatible with forthcoming industry standard monolithic designs. These modules are intended for use in applications where limited board space dictates compact module designs.

The operation of the AK68512D is identical to standard monolithic 8 bit word wide SRAMs.

The AK68512D offers the features of low power and medium speed by using CMOS devices and makes high density mounting possible with no surface mount technology.

FEATURES

- 524,288 x 8 bit organization
- Fast access time: 85 - 120 nSEC
- Completely static RAM, no clock or timing strobe required
- Inputs and outputs TTL compatible
- Conventional 600 mil wide SIP package with industry compatible pinout
- Single 5 volt power supply - AK68512D
- Single 3.3 volt power supply - AK68512D/3.3



- Operating free air temperature 0° to 70°C

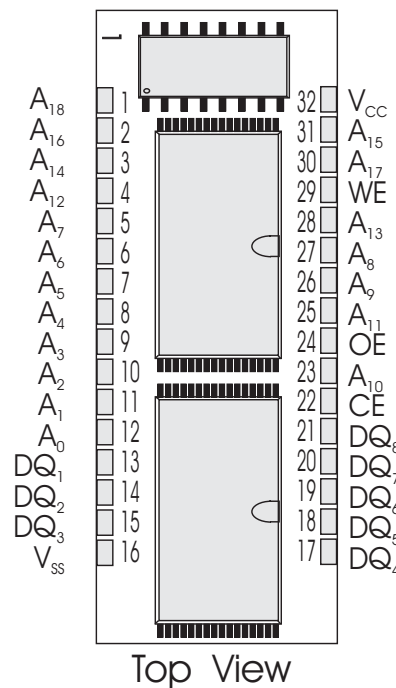
ELECTRICAL SPECIFICATIONS

Timing diagrams and basic electrical characteristics are those of the standard 128K x 8 SRAMs used to construct these modules. Accuthek's module design allows the flexibility of selecting industry-compatible 128K x 8 SRAMs from any of a number of semiconductor manufacturers.

PIN NOMENCLATURE

| | |
|-----------------------------------|------------------|
| DQ ₁ - DQ ₈ | Data In/Data Out |
| A ₀ - A ₁₈ | Address Inputs |
| \overline{CE} | Chip Enable |
| \overline{WE} | Write Enable |
| V _{cc} | 5v Supply |
| V _{ss} | Ground |
| \overline{OE} | Output Enable |

PIN ASSIGNMENT



TIMING OPTIONS

| |
|----------------------|
| 70 nSEC Access Time |
| 85 nSEC Access Time |
| 100 nSEC Access Time |
| 120 nSEC Access Time |

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

| Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|--|---|---|---|---|---|---|---|---|
| 1 Product | | | | | | | | |
| AK = Accuthek Memory | | | | | | | | |
| 2 Type | | | | | | | | |
| 4 = Dynamic RAM | | | | | | | | |
| 5 = CMOS Dynamic RAM | | | | | | | | |
| 6 = Static RAM | | | | | | | | |
| 3 Organization/Word Width | | | | | | | | |
| 1 = by 1 16 = by 16 | | | | | | | | |
| 4 = by 4 32 = by 32 | | | | | | | | |
| 8 = by 8 36 = by 36 | | | | | | | | |
| 9 = by 9 | | | | | | | | |
| 4 Size/Bits Depth | | | | | | | | |
| 64 = 64K 4096 = 4 MEG | | | | | | | | |
| 256 = 256K 8192 = 8 MEG | | | | | | | | |
| 1024 = 1 MEG 16384 = 16 MEG | | | | | | | | |
| 5 Package Type | | | | | | | | |
| G = Single In-Line Package (SIP) | | | | | | | | |
| S = Single In-Line Module (SIM) | | | | | | | | |
| D = Dual In-Line Package (DIP) | | | | | | | | |
| W = .050 inch Pitch Edge Connect | | | | | | | | |
| Z = Zig-Zag In-Line Package (ZIP) | | | | | | | | |
| 6 Special Designation | | | | | | | | |
| P = Page Mode | | | | | | | | |
| N = Nibble Mode | | | | | | | | |
| K = Static Column Mode | | | | | | | | |
| W = Write Per Bit Mode | | | | | | | | |
| V = Video Ram | | | | | | | | |
| 7 Separator | | | | | | | | |
| - = Commercial 0°C to +70°C | | | | | | | | |
| M = Military Equivalent Screened (-55°C to +125°C) | | | | | | | | |
| I = Industrial Temperature Tested (-45°C to +85°C) | | | | | | | | |
| X = Burned In | | | | | | | | |
| 8 Speed (first two significant digits) | | | | | | | | |
| DRAMS SRAMS | | | | | | | | |
| 50 = 50 nS 8 = 8 nS | | | | | | | | |
| 60 = 60 nS 10 = 10 nS | | | | | | | | |
| 70 = 70 nS 12 = 12 nS | | | | | | | | |
| 80 = 80 nS 15 = 15 nS | | | | | | | | |

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

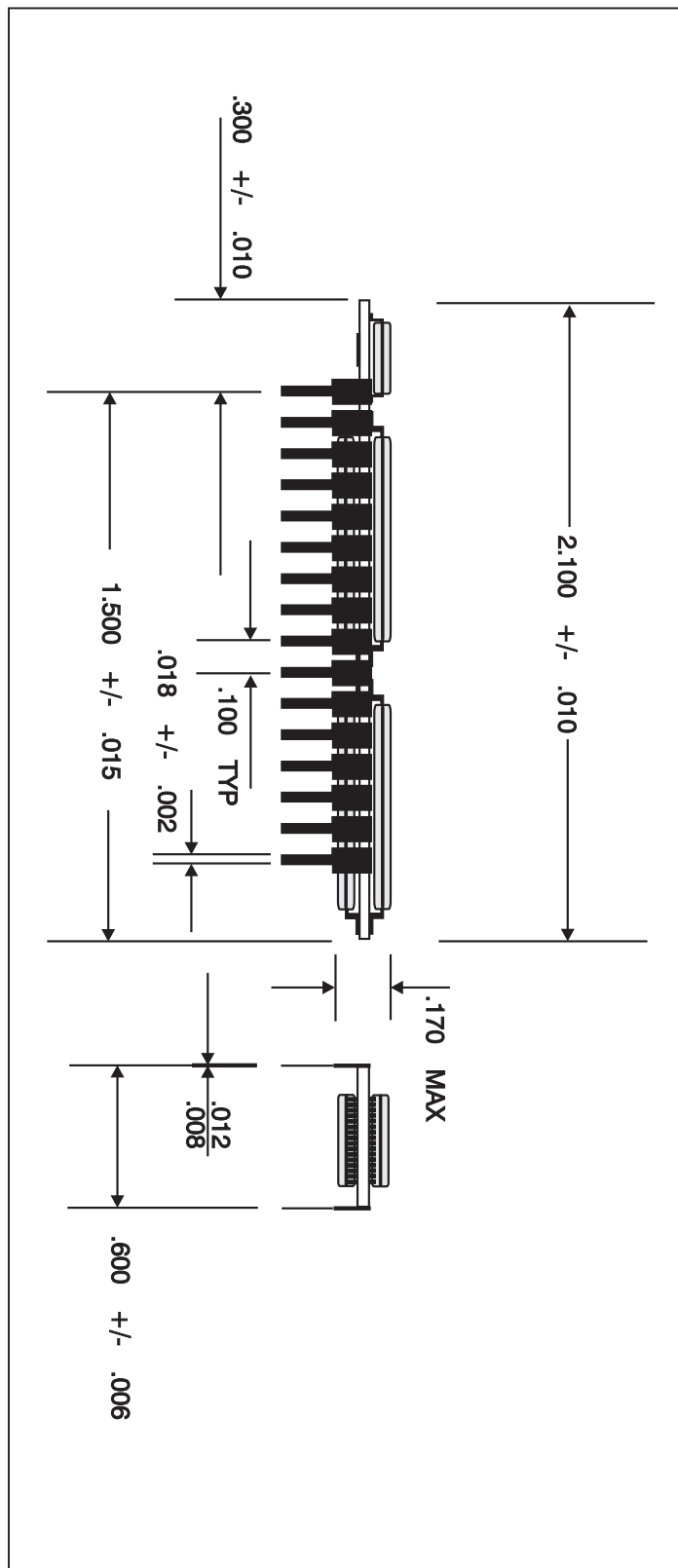
EXAMPLES:

AK68512D-70

512K x 8, 70 nSEC SRAM Module, DIP Configuration

MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.



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