

## DESCRIPTION

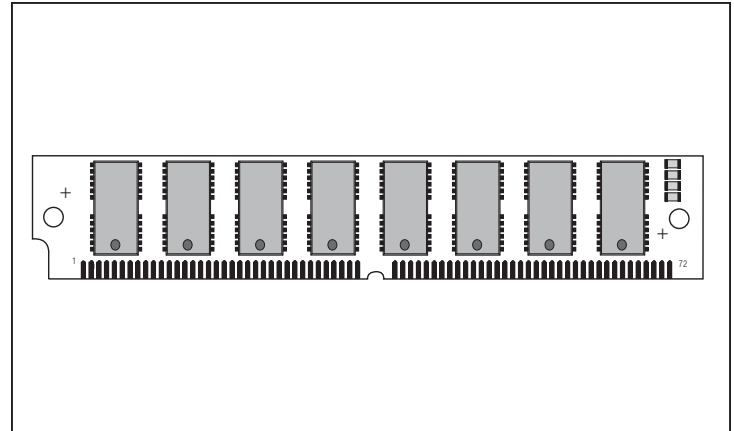
The Accutek AK5328192W high density memory module is a CMOS dynamic RAM organized in 8192K x 32 bit words. The module consists of sixteen standard 4 Meg x 4 DRAMs in plastic SOJ packages. The assembly has eight drams mounted on each side of a printed circuit board in a 72 pad leadless SIM configuration.

This configuration allows socket-mounting of large quantities of memory in applications where high density and ease of inserting additional memory are important.

The operation of the AK5328192W is identical to sixteen 4M x 4 Drams. There are four CAS lines and four RAS lines. On each bank of 4M x 32, independent byte control is accomplished by four  $\overline{\text{CAS}}$  lines. Each separate CAS line controls two 4M x 4 Drams to form an 8 bit byte. Two banks of 32 bits are controlled by the two pairs of RAS lines. A sixteen bit data path can be produced by connecting DQ<sub>0</sub> to DQ<sub>16</sub>, DQ<sub>1</sub> to DQ<sub>17</sub>, etc. and alternately strobing  $\overline{\text{RAS}}_0$  with  $\overline{\text{RAS}}_1$  and  $\overline{\text{RAS}}_2$  with  $\overline{\text{RAS}}_3$ .

## FEATURES

- 8,388,608 x 32 bit organization
- 72 pad Single In-Line Module
- Multiple  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  lines allow x16 or x32 bit widths
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ ,  $\overline{\text{RAS}}$ -only or hidden refresh
- Power
  - 5.32 Watt Max Active (60nS)
  - 4.48 Watt Max Active (70 nS)
  - 88 mW Max Standby
- Operating free air temperature 0°C to 70°C



- Single 5 Volt Power Supply
- 2048 Refresh Cycles, 32 mSEC
- 4096 Refresh Cycles, 64 mSEC available for all module sizes
- Available in Fast Page Mode and EDO
- Available in leadless (W) or leaded Zip (Z) versions
- Downward compatible with AK5324096, AK5322048, AK5321024, AK532512 and AK532256

## EXAMPLES

### AK5328192WP-60

8 Meg x 32 CMOS Dynamic RAM, SIM, Page Mode, Commercial 60 nSEC Access Time

## PIN NOMENCLATURE

A <sub>0</sub> - A <sub>10</sub>	Address Inputs
DQ <sub>0</sub> - DQ <sub>31</sub>	Data In/Data Out
$\overline{\text{CAS}}_0$ - $\overline{\text{CAS}}_3$	Column Address Strobe
$\overline{\text{RAS}}_0$ - $\overline{\text{RAS}}_3$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
PD <sub>1</sub> - PD <sub>4</sub>	Presence Detect
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
NC	No Connect

## MODULE OPTIONS

Leadless SIM: AK5328192W

Leaded ZIP: AK5328192Z

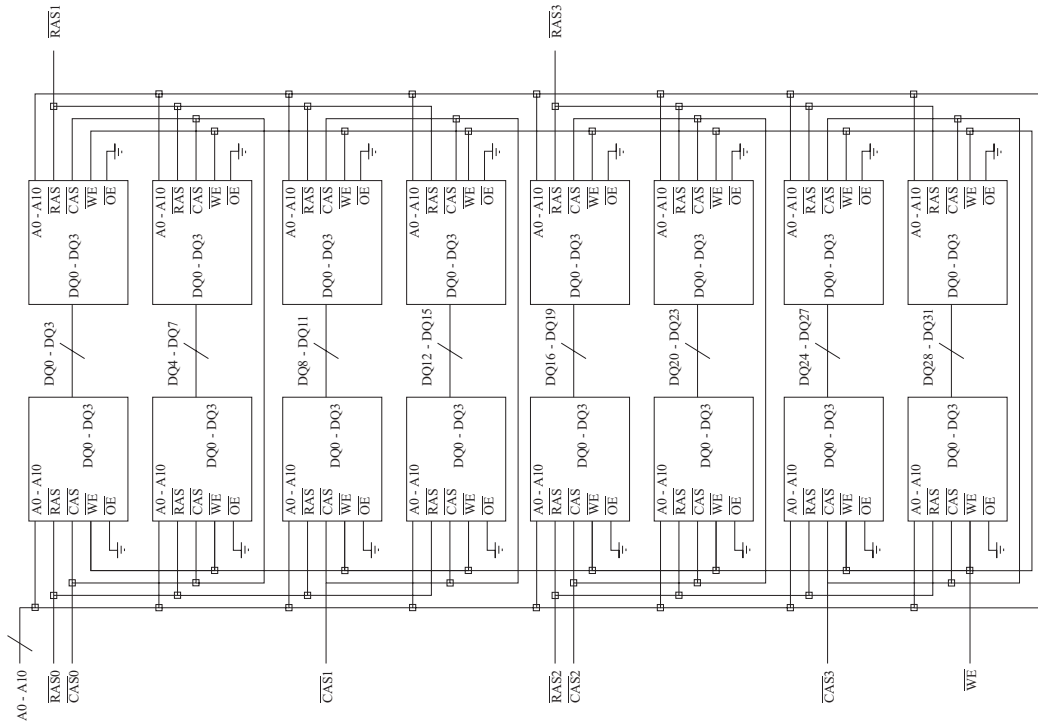
## PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>ss</sub>	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V <sub>ss</sub>	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS}}_0$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS}}_2$	59	V <sub>cc</sub>
6	DQ2	24	DQ6	42	$\overline{\text{CAS}}_3$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS}}_1$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS}}_0$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{\text{RAS}}_1$	63	DQ14
10	V <sub>cc</sub>	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V <sub>cc</sub>	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{\text{RAS}}_3$	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS}}_2$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V <sub>ss</sub>

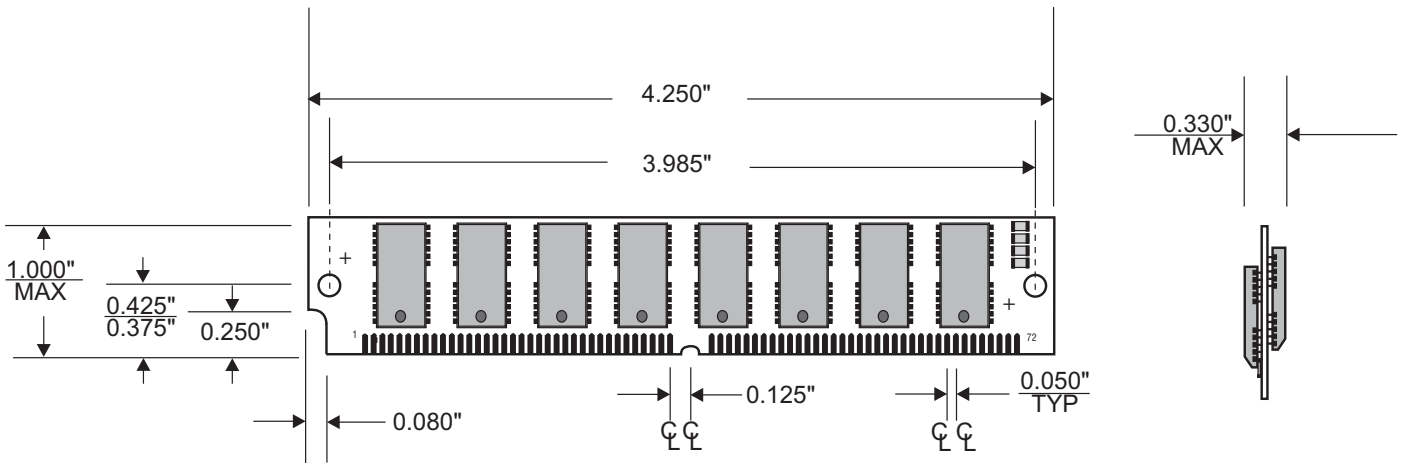
### Presence Detect -

	-60	-70
PD1	NC	NC
PD2	V <sub>ss</sub>	V <sub>ss</sub>
PD3	NC	V <sub>ss</sub>
PD4	NC	NC

# FUNCTIONAL DIAGRAM



# MECHANICAL DIMENSIONS



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