

AK594096BS / AK594096BG 4,194,304 Word by 9 Bit CMOS Dynamic Random Access Memory

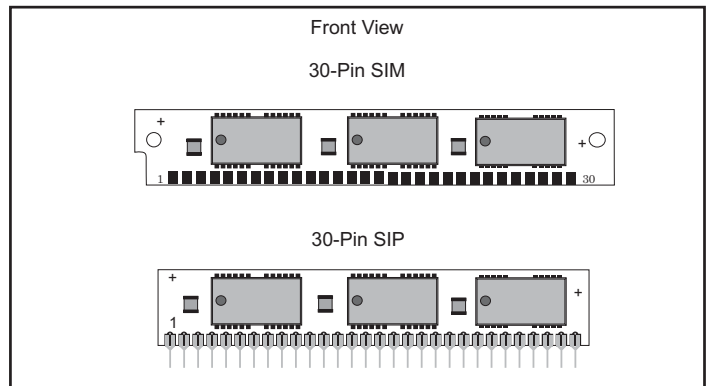
DESCRIPTION

The Accutek AK594096 high density memory module is a CMOS random access memory organized in 4 Meg x 9 bit words. The assembly consists of two 4 Meg x 4 and one 4 Meg x 1 DRAMs, mounted on the front side of a printed circuit board in 30 pad SIM (leadless) or 30 pin SIP (leadless) configuration with JEDEC-standard pinouts. Designed especially for low-height applications such as VMEbus boards, this low profile module is 0.550 inch high.

The operation is identical to nine 4 Meg x 1 DRAMs. For the lower eight bits, data input is tied to data output and brought out separately for each bit, with common \overline{RAS} and \overline{CAS} control. This common I/O feature dictates the use of early-write cycles to prevent contention of data In and data out. Since the Write-Enable (\overline{WE}) signal must always go low before \overline{CAS} in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, data in (D_9) and data out (Q_9) pins are brought out separately and controlled by a separate \overline{PCAS} for that bit.

FEATURES

- 4,194,304 x 9 bit organization
- Low Profile 30 pad (SIM) Single In-Line Memory
- Low Profile 30 pin (SIP) Single In-Line package
- JEDEC standard pinout
- Common \overline{CAS} , \overline{RAS} and \overline{WE} for the lower eight bits
- \overline{CAS} -before- \overline{RAS} refresh



- Refresh cycle 2048 cycles in 32 mSEC
- Power
1.450 Watt Max Active, 70 nSEC
1.610 Watt Max Active, 60 nSEC
16.5 mWatt Max Standby
- Operating free air temperature 0°C to 70°C
- Downward compatible with AK591024 and AK59256
- Upward compatible with AK5916384
- Fast Page Mode and Static Column Mode versions available, nibble mode is not possible

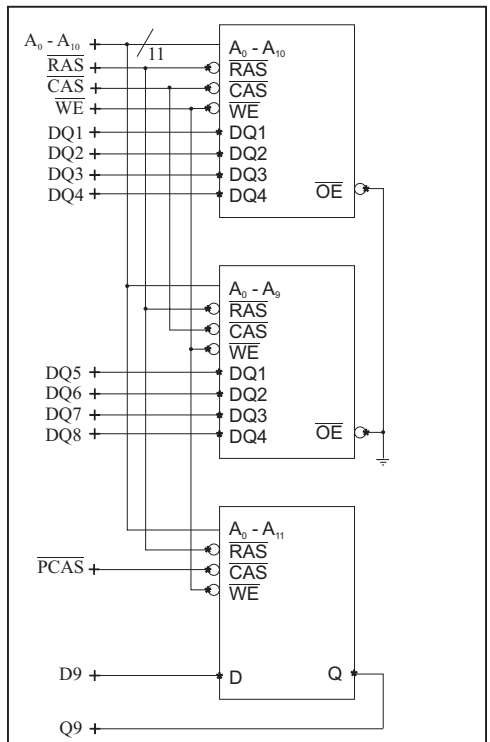
PIN NOMENCLATURE

$A_0 - A_{10}$	Address Inputs
\overline{RAS}_0	Row Address Strobe
\overline{CAS}	Column Address Strobe
\overline{WE}	Write Enable
\overline{OE}	Output Enable
$DQ_1 - DQ_8$	Data In/Data Out
D_9	Data In
Q_9	Data Out
Vcc	5v Supply
Vss	Ground
NC	No Connect

PIN ASSIGNMENT

Pin #	Symbol	Pin #	Symbol
1	Vcc	16	DQ5
2	\overline{CAS}	17	A8
3	DQ1	18	A9
4	A0	19	A10
5	A1	20	DQ6
6	DQ2	21	\overline{WE}
7	A2	22	Vss
8	A3	23	DQ7
9	Vss	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	\overline{RAS}_0
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	Vcc

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leadless SIM: AK594096BS
Leaded SIP: AK594096BG

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position 1 2 3 4 5 6 7 8

- 1 Product**
AK = Accuthek Memory
- 2 Type**
4 = Dynamic RAM
5 = CMOS Dynamic RAM
6 = Static RAM
- 3 Organization/Word Width**
1 = by 1 16 = by 16
4 = by 4 32 = by 32
8 = by 8 36 = by 36
9 = by 9
- 4 Size/Bits Depth**
64 = 64K 4096 = 4 MEG
256 = 256K 8192 = 8 MEG
1024 = 1 MEG 16384 = 16 MEG
- 5 Package Type**
G = Single In-Line Package (SIP)
S = Single In-Line Module (SIM)
D = Dual In-Line Package (DIP)
W = .050 inch Pitch Edge Connect
Z = Zig-Zag In-Line Package (ZIP)
- 6 Special Designation**
P = Page Mode
N = Nibble Mode
K = Static Column Mode
W = Write Per Bit Mode
V = Video Ram
- 7 Separator**
- = Commercial 0°C to +70°C
M = Military Equivalent Screened (-55°C to +125°C)
I = Industrial Temperature Tested (-45°C to +85°C)
X = Burned In
- 8 Speed (first two significant digits)**
DRAMS SRAMS
50 = 50 nS 8 = 8 nS
60 = 60 nS 10 = 10 nS
70 = 70 nS 12 = 12 nS
80 = 80 nS 15 = 15 nS

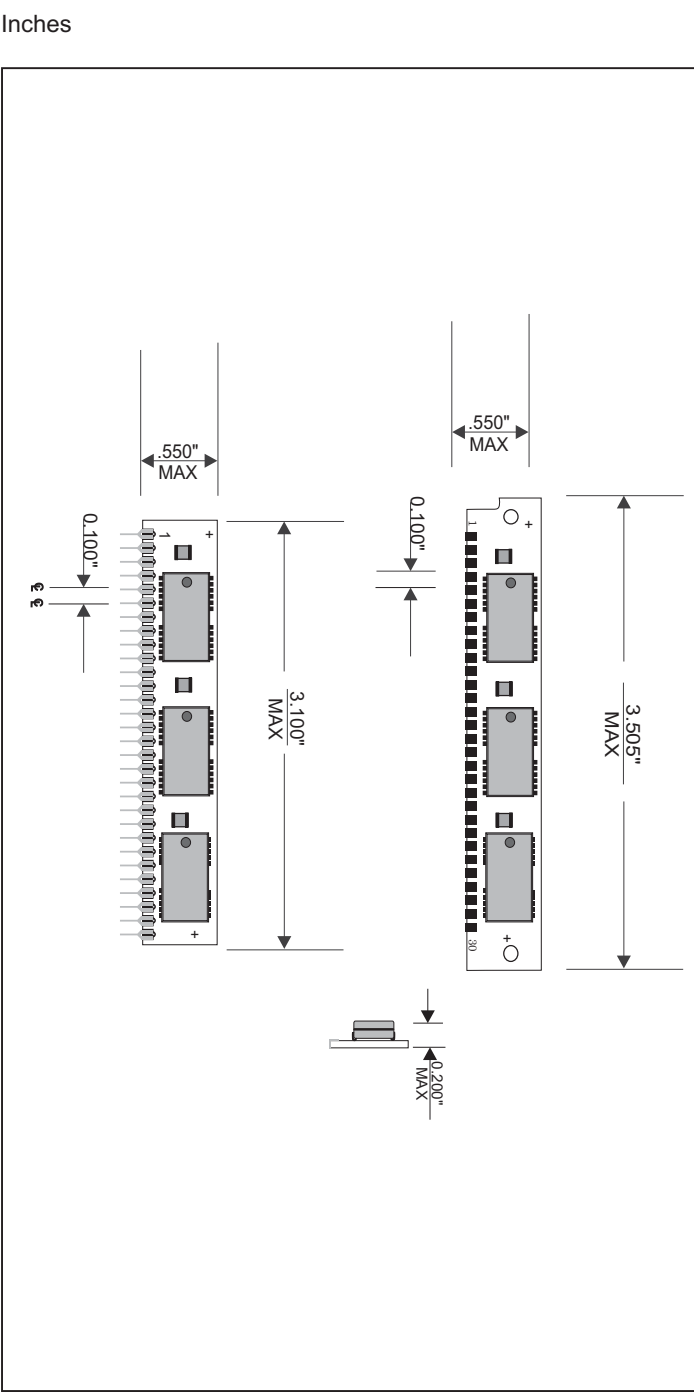
The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accuthek if other information is required.

EXAMPLES:

AK594096BGP-70
4 Meg x 9, CMOS Dynamic RAM, Leaded SIP, Page Mode, Commercial, 70 nSEC Access Time

AK594096BSP-60
4 Meg x 9, CMOS Dynamic RAM, Leadless SIM, Page Mode, Commercial, 60 nSEC Access Time

MECHANICAL DIMENSIONS



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.