

# AK594096AS / AK594096AG

## 4,194,304 Word x 9 Bit CMOS

### Dynamic Random Access Memory

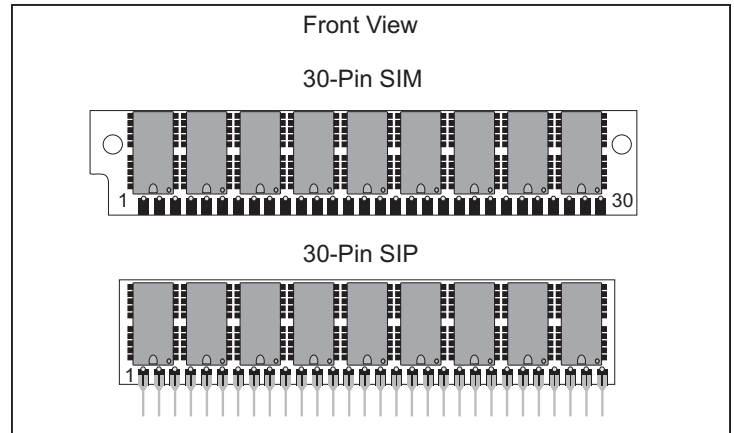
#### DESCRIPTION

The Accutek AK594096A high density memory module is a CMOS random access memory organized in 4 Meg x 9 bit words. The assembly consists of nine standard 4 Meg x 1 DRAMs in plastic leaded chip carriers (SOJ) mounted on the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. The module is only 0.800 inches high (same height as a standard 1 Meg module), making it ideally suited for applications with low height restrictions.

The operation of the AK594096A is identical to nine 4 Meg x 1 DRAMs. For the lower eight bits data input is tied to the data output and brought out separately for each device, with common  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable ( $\overline{\text{WE}}$ ) signal must always go low before  $\overline{\text{CAS}}$  in a write cycle, Read-Write and Read-Modify-Write operation is not possible. For the ninth bit, the data input ( $\text{D}_9$ ) and the data output ( $\text{Q}_9$ ) pins are brought out separately and controlled by a separate  $\overline{\text{PCAS}}$  for that bit. Bit nine is generally used for parity.

#### FEATURES

- 4,194,304 x 9 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Common  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  control for the lower eight bits
- Separate  $\overline{\text{PCAS}}$  for control for  $\text{D}_9$  and  $\text{Q}_9$
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
- Power
  - 4.45 Watt Max Active (80 nSEC)
  - 3.96 Watt Max Active (100 nSEC)
  - 49.5 mW Max Standby
- Operating free air temperature  $0^\circ\text{C}$  to  $70^\circ\text{C}$
- Upward compatible with AK5916384
- Downward compatible with AK591024, AK59256



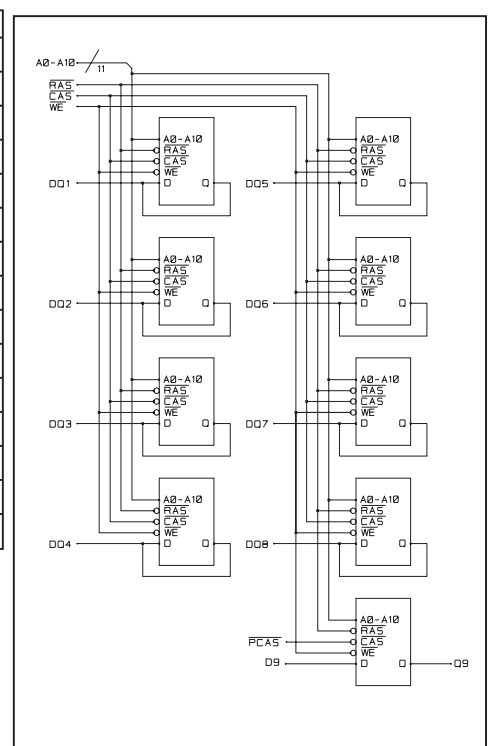
#### PIN NOMENCLATURE

DQ <sub>1</sub> - DQ <sub>8</sub>	Data In / Data Out
D <sub>9</sub>	Data In 9
Q <sub>9</sub>	Data Out 9
A <sub>0</sub> - A <sub>10</sub>	Address Inputs
$\overline{\text{CAS}}$ , $\overline{\text{PCAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
V <sub>cc</sub>	5v Supply
V <sub>ss</sub>	Ground
NC	No Connect

#### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	V <sub>cc</sub>	16	DQ <sub>5</sub>
2	$\overline{\text{CAS}}$	17	A <sub>8</sub>
3	DQ <sub>1</sub>	18	A <sub>9</sub>
4	A <sub>0</sub>	19	A <sub>10</sub>
5	A <sub>1</sub>	20	DQ <sub>6</sub>
6	DQ <sub>2</sub>	21	$\overline{\text{WE}}$
7	A <sub>2</sub>	22	V <sub>ss</sub>
8	A <sub>3</sub>	23	DQ <sub>7</sub>
9	V <sub>ss</sub>	24	NC
10	DQ <sub>3</sub>	25	DQ <sub>8</sub>
11	A <sub>4</sub>	26	Q <sub>9</sub>
12	A <sub>5</sub>	27	$\overline{\text{RAS}}$
13	DQ <sub>4</sub>	28	$\overline{\text{PCAS}}$
14	A <sub>6</sub>	29	D <sub>9</sub>
15	A <sub>7</sub>	30	V <sub>cc</sub>

#### FUNCTIONAL DIAGRAM



#### MODULE OPTIONS

Leadless SIM: AK594096AS
Leaded SIP: AK594096AG

