



AK584096BS / AK584096BG

4,194,304 Word by 8 Bit CMOS

Dynamic Random Access Memory

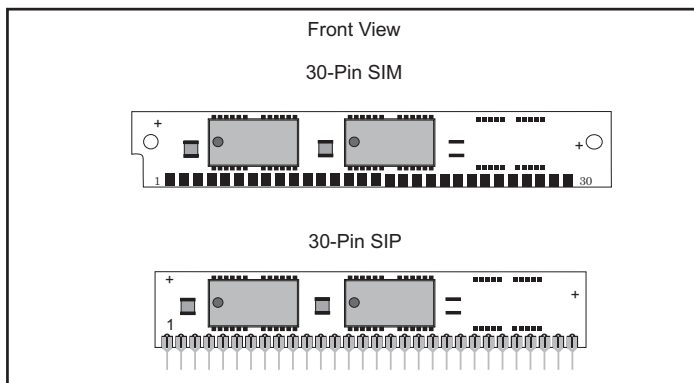
DESCRIPTION

The Accutek AK584096 high density memory module is a CMOS dynamic RAM organized in 4 Meg x 8 bit words. The assembly consists of two 4 Meg x 4 DRAMS, mounted on the front side of a printed circuit board in 30 pad SIM (leadless) or 30 pin SIP (leaded) configuration with JEDEC-standard pinouts. Designed especially for low-height applications such as VMEbus boards, this low profile module is 0.550 inch high.

The operation is identical to eight 4 Meg x 1 DRAMs. The data input/output is brought out separately for each bit, with common RAS, CAS and WE control. This common I/O feature dictates the use of early-write cycles to prevent contention of Data In and Data Out. Since the Write-Enable (WE) signal must always go low before CAS in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

FEATURES

- 4,194,304 x 8 bit organization
- Low Profile 30 pad (SIM) Single In-Line Memory
- Low Profile 30 pin (SIP) Single In-Line package
- JEDEC standard pinout
- Common CAS and RAS control for eight common DQ Lines
- CAS-before-RAS refresh
- Refresh cycle 2048 cycles in 32 mSEC
- Power
 - 0.095 Watt Max Active, 70 nSEC
 - 1.060 Watt Max Active, 60 nSEC
 - 11.0 mWatt Max Standby
- Operating free air temperature 0°C to 70°C
- Downward compatible with AK581024 and AK58256
- Upward compatible with AK5816384
- Fast Page Mode and Static Column Mode versions available, nibble mode is not possible



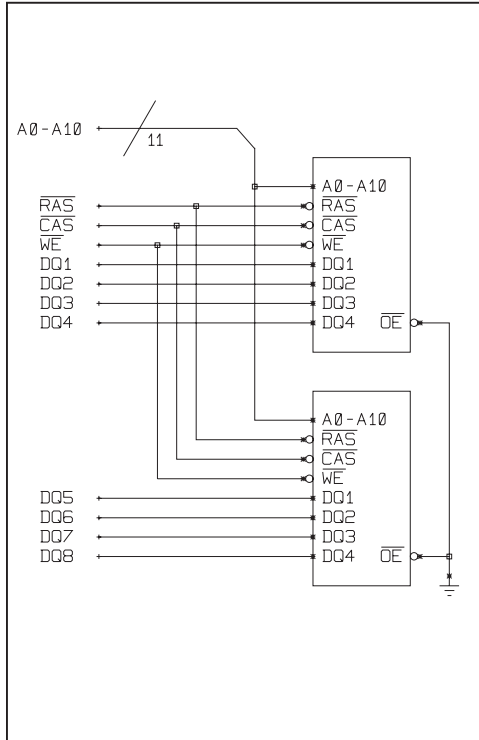
PIN NOMENCLATURE

A ₀ - A ₁₀	Address Inputs
RAS ₀	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
DQ ₁ - DQ ₈	Data In/Data Out
Vcc	5v Supply
Vss	Ground
NC	No Connect

PIN ASSIGNMENT

Pi n #	Symbol	Pi n #	Symbol
1	Vcc	16	DQ5
2	CAS	17	A8
3	DQ1	18	A9
4	A0	19	A10
5	A1	20	DQ6
6	DQ2	21	WE
7	A2	22	Vss
8	A3	23	DQ7
9	Vss	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	RAS ₀
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	Vcc

FUNCTIONAL DIAGRAM



MODULE OPTIONS

Leadless SIM: AK584096BS

Leaded SIP: AK584096BG

ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8
1	Product							
	AK = Accuthek Memory							
2	Type							
	4 = Dynamic RAM							
	5 = CMOS Dynamic RAM							
	6 = Static RAM							
3	Organization/Word Width							
	1 = by 1 16 = by 16							
	4 = by 4 32 = by 32							
	8 = by 8 36 = by 36							
	9 = by 9							
4	Size/Bits Depth							
	64 = 64K 4096 = 4 MEG							
	256 = 256K 8192 = 8 MEG							
	1024 = 1 MEG 16384 = 16 MEG							
5	Package Type							
	G = Single In-Line Package (SIP)							
	S = Single In-Line Module (SIM)							
	D = Dual In-Line Package (DIP)							
	W = .050 inch Pitch Edge Connect							
	Z = Zig-Zag In-Line Package (ZIP)							
6	Special Designation							
	P = Page Mode							
	N = Nibble Mode							
	K = Static Column Mode							
	W = Write Per Bit Mode							
	V = Video Ram							
7	Separator							
	- = Commercial 0°C to +70°C							
	M = Military Equivalent Screened (-55°C to +125°C)							
	I = Industrial Temperature Tested (-45°C to +85°C)							
	X = Burned In							
8	Speed (first two significant digits)							
	DRAMS SRAMS							
	50 = 50 nS 8 = 8 nS							
	60 = 60 nS 10 = 10 nS							
	70 = 70 nS 12 = 12 nS							
	80 = 80 nS 15 = 15 nS							

The numbers and coding on this page do not include all variations available but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.

EXAMPLES:

AK584096BGP-70

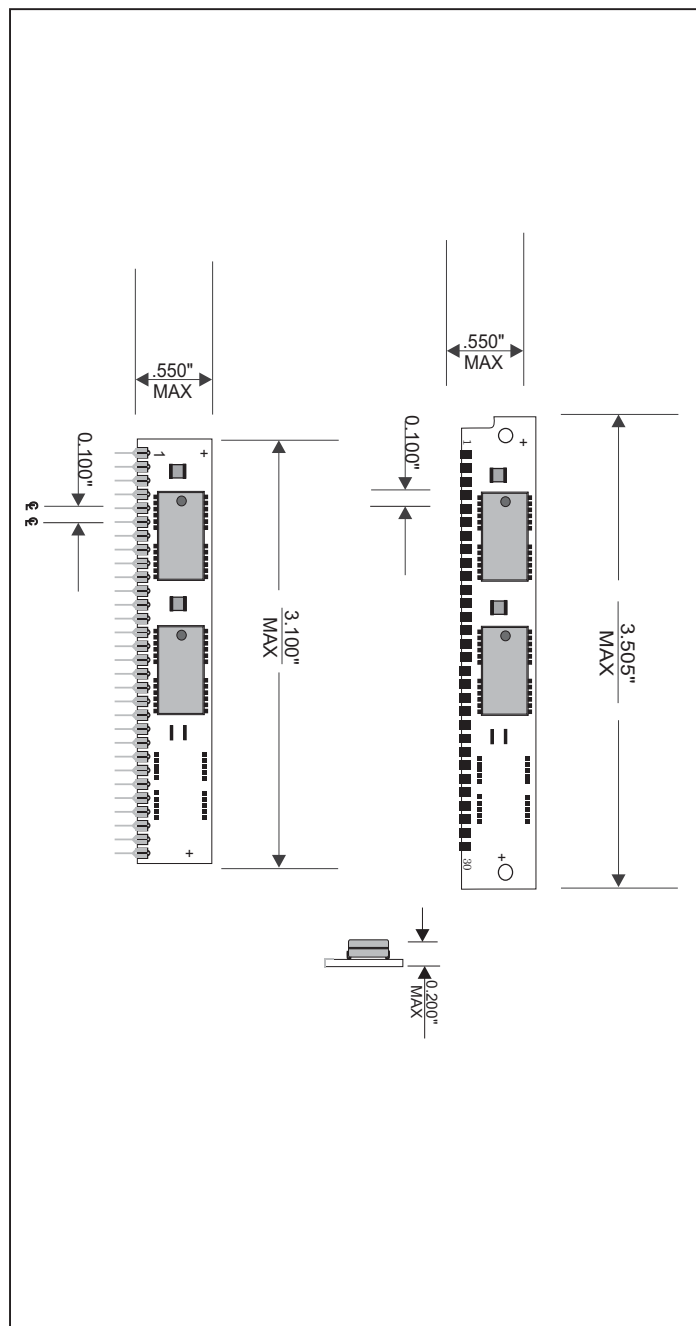
4 Meg x 8, CMOS Dynamic RAM, Leaded SIP, Page Mode, Commercial, 70 nSEC Access Time

AK584096BSP-60

4 Meg x 8, CMOS Dynamic RAM, Leadless SIM, Page Mode, Commercial, 60 nSEC Access Time

MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.