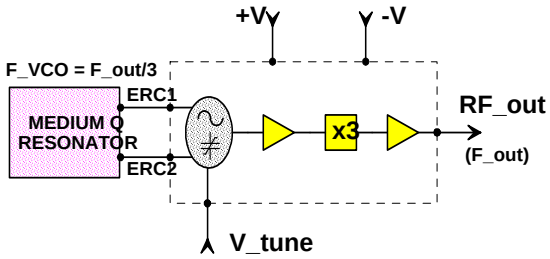
Q-band VCO based on Ku-band Oscillator and Q-band Multiplier

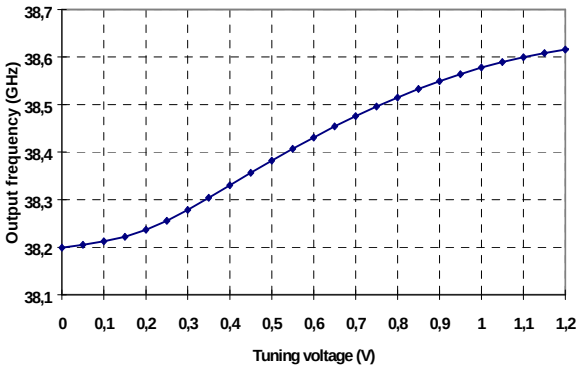
GaAs Monolithic Microwave IC

Description

The CHV2242c is a monolithic multifunction for frequency generation. It integrates a Ku-band oscillator with frequency control (VCO), a Q-band frequency multiplier and buffer amplifiers. For performance optimisation, two external ports (ERC1 and ERC2) allow a passive resonator coupling to the oscillator (at one third of output frequency). On chip Schottky diode, based on a pHEMT, is used as varactor. All the active devices are internally self-biased.
The circuit is manufactured with the pHEMT process 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Multifunction block diagram



Typical tuning characteristic
(Coupled to a micro-strip filter

Main Features

- Ku-band VCO + Q-band multiplier
- On chip varactor
- External resonator for centre frequency control and phase noise optimisation
- Low phase noise
- Auxiliary output at VCO frequency
- High temperature range
- On-chip self biasing
- Automatic assembly oriented
- Chip size 2.41 x 1.18 x 0.1mm
- BCB Layer protection

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output centre frequency	38	38.25	38.5	GHz
F_vco	Oscillator frequency	F_out/3			
F_tune	Output frequency tuning range	150	200		MHz
Pout	Output power	5	7		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Full temperature range, used according to section “Typical assembly and bias configuration”

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output centre frequency	38	38.25	38.5	GHz
F_vco	VCO frequency (1)		F_out/3		
F_tune	Frequency tuning range (at F_out) (2)	150	200		MHz
P_out	Output power	5	7		dBm
F_slope	Frequency tuning slope (2)		500		MHz/V
V_tune	Control voltage range		0.2 – 0.8	0 – 1.5	V
Pushing	Frequency pushing vs positive supply voltage		60		MHz/v
PN	Phase noise (given at F_out) (2) @ 10kHz @ 100kHz @ 1MHz		 -48 -75 -100	 -43 -70 -95	dBc/Hz
+V	Positive supply voltage	4.4	4.5	4.6	V
+I	Positive supply current		110	160	mA
-V	Negative supply voltage	-4.6	-4.5	-4.4	V
-I	Negative supply current		5	8	mA
Top	Operating temperature range	-40		100	℃

(1) The centre frequency is given by the external passive resonator

(2) This characteristic depends on the resonator Q, the given performance has been obtained by using a micro-strip filter used as resonator (see section “Proposed External Medium Q Resonator”)

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
V_tune	Tuning voltage	2.5	V
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	250	mA
-I	Negative supply current	15	mA
Tstg	Storage temperature range	-55 to +155	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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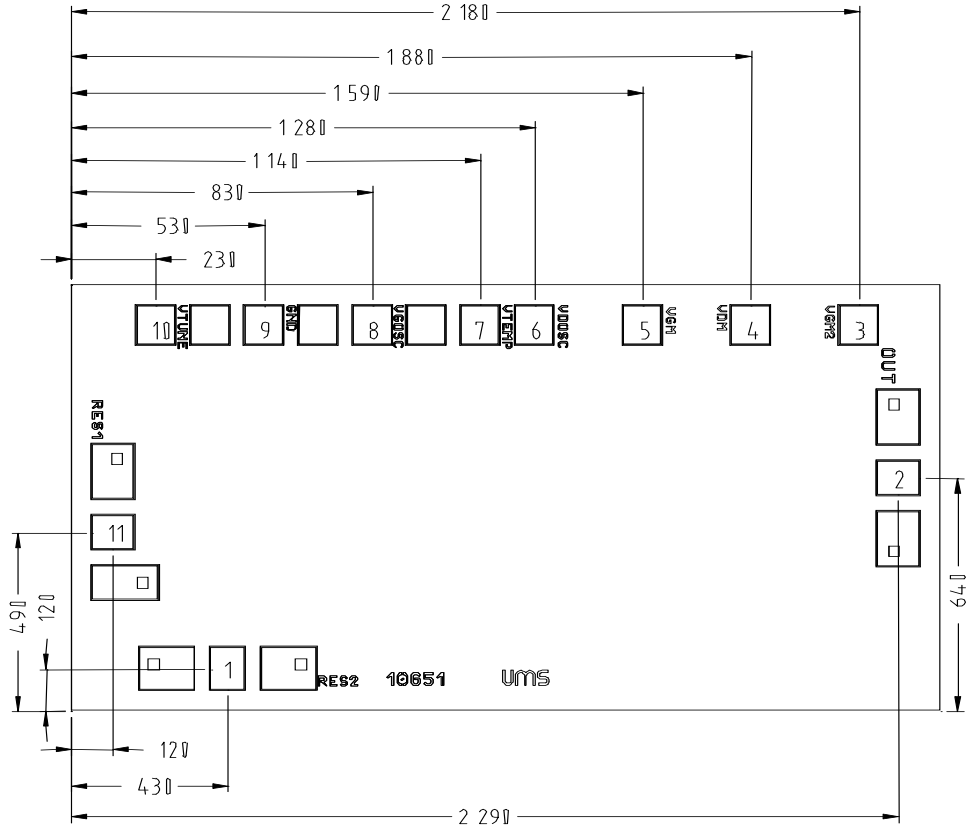
Chip Mechanical Data and Pin References



Unit = µm
External chip size = 2410 x 1180 +/- 35
Chip thickness = 100 +/- 10
RF Pads (1, 2,11) = 83 x 86
DC/IF Pads = 98 x 95

Pin number	Pin name	Description
1	**ERC2**	External Resonator Coupling Port 2
2	**RF_out**	RF output at 38GHz
3, 7		NC
4, 6	**+V**	Positive supply voltage
5, 8	**-V**	Negative supply voltage
9		GND (optional)
10	**V-tune**	Tuning voltage input port
11	**ERC1**	External Resonator Coupling Port 1
No Number		Ground : should not be bonded. If required, please ask for more information.

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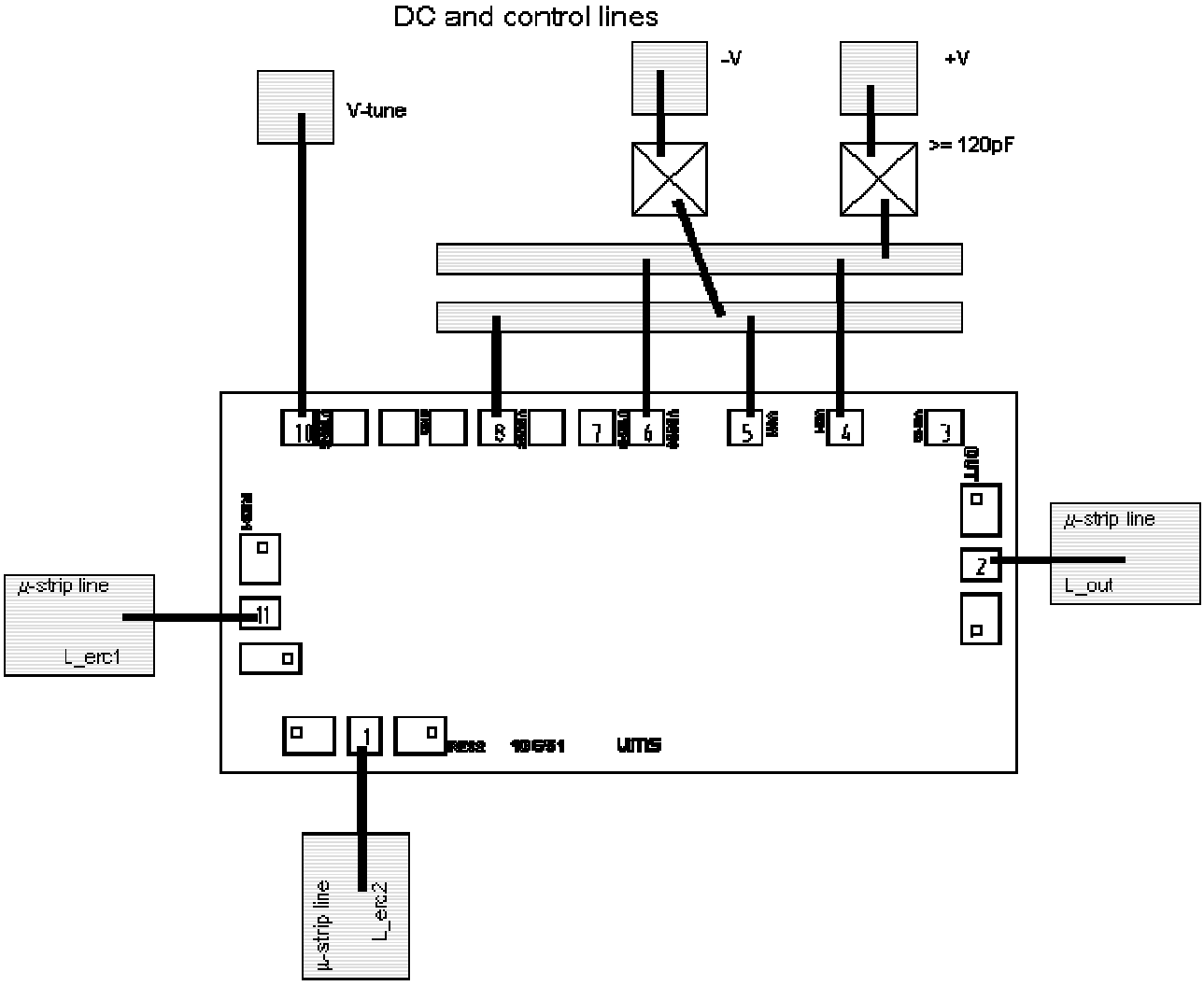
Typical Assembly and Bias Configuration



This drawing shows an example of assembly and bias configuration. All the transistors are internally self-biased. The positive and negative voltages can be respectively connected together (see drawing) according to the recommended values given in the electrical characteristics table. **Due to the high value of frequency sensitivity versus tuning voltage (around 500MHz/V), the signal applied to V_tune port must have very low level of noise.**

For the RF pads the equivalent wire bonding inductance (diameter=25µm) has to be according to the following recommendation.

Port	Equivalent inductance (nH)	Approximated wire length (mm)
ERC1 (11)	L_erc1 = 0.4	0.5
ERC2 (1)	L_erc2 = 0.4	0.5
RF_out (2)	L_out = 0.28	0.35

For a micro-strip configuration a hole in the substrate is recommended for chip assembly.

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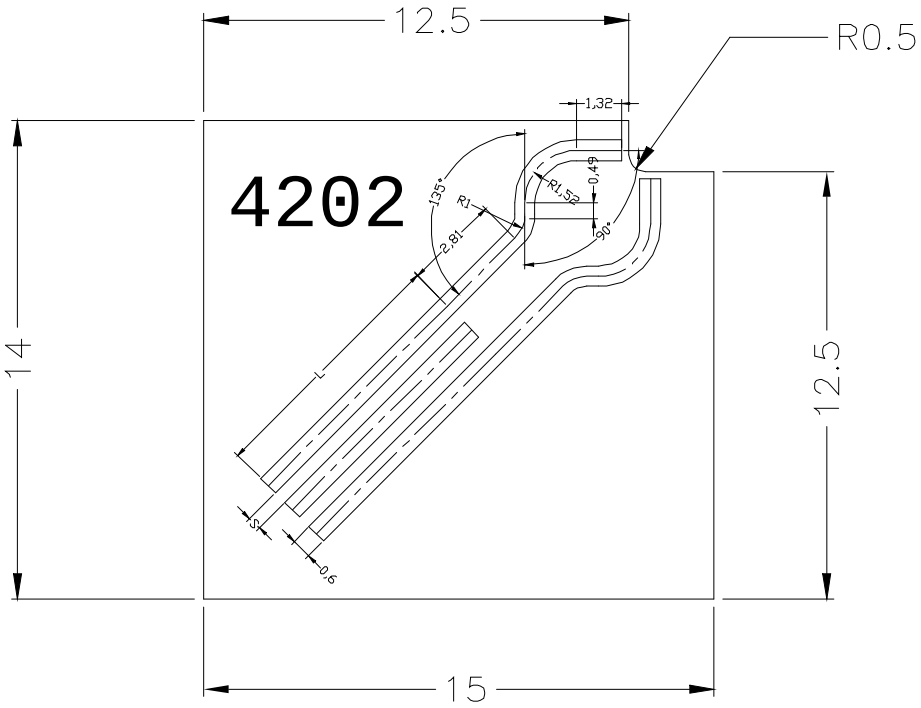
Proposed External Medium Q Resonator

This resonator can be used for 77GHz FMCW-based radar applications.

The chip has been especially designed to be coupled to a medium Q resonator printed on temperature compensated soft substrate. The resonance is given by three half wave coupled lines. The length of the coupler (L) gives the centre frequency and the space between the coupled lines (s) gives the bandwidth. For easy connection and phase considerations half wave lines are at the input and output of the filter. All the recommended dimensions are given in the following drawing.



The main substrate characteristics are the following (ROGERS R03003)

Dielectric constant	Thickness	Dissipation factor (10GHz)	Thermal coefficient
3	250µm	0.0013	13 ppm/℃

The typical resonator length (L) is 7.35mm for a coupling value (s) of 0.4mm and for a frequency of 38.25GHz. However this L value should have to be adjusted depending on the final chip environment.

Other possibility is ARLON/CLTE substrate. (L is 7.27mm for s=0.4mm)

Recommendation for Frequency stability

In order to ensure a good frequency stability (versus temperature, external resonator aging,…), it is recommended to use an external frequency locked loop with a low frequency loop filter (below modulation frequency), or a PLL for both frequency modulation and stability.

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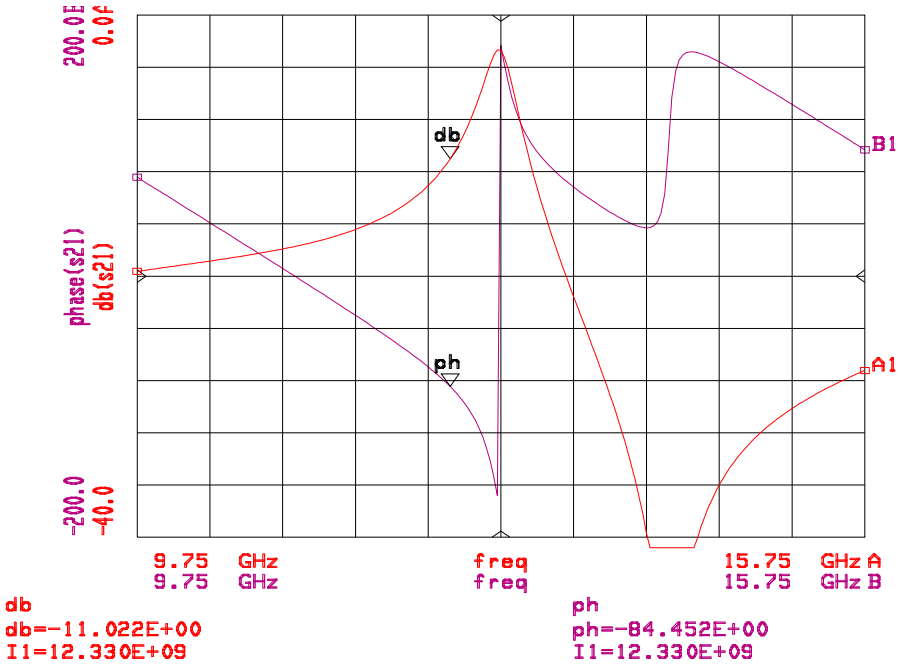
Proposed External Medium Q Resonator

The following information is about the S parameter of the resonator (plot for S21 and table for the four parameters). These values don't include the wire bonding equivalent inductance L_erc1 and L_erc2 given in section "Typical Assembly and Bias Configuration".



S21 of the proposed external resonator

freq	dB(S11)	phase(S11)	dB(S21)	phase(S21)	dB(S12)	phase(S12)	dB(S22)	phase(S22)
9.750E+09	-0.269	165.984	-19.639	75.748	-19.639	75.748	-0.269	165.984
10.05E+09	-0.282	148.566	-19.246	58.344	-19.246	58.344	-0.282	148.566
10.35E+09	-0.294	131.116	-18.849	40.900	-18.849	40.900	-0.294	131.116
10.65E+09	-0.306	113.629	-18.421	23.404	-18.421	23.404	-0.306	113.629
10.95E+09	-0.320	96.082	-17.921	5.819	-17.921	5.819	-0.320	96.082
11.25E+09	-0.337	78.416	-17.290	-11.932	-17.290	-11.932	-0.337	78.416
11.55E+09	-0.364	60.508	-16.428	-30.016	-16.428	-30.016	-0.364	60.508
11.85E+09	-0.415	42.062	-15.152	-48.824	-15.152	-48.824	-0.415	42.062
12.15E+09	-0.543	22.219	-13.061	-69.511	-13.061	-69.511	-0.543	22.219
12.45E+09	-1.135	-2.751	-9.044	-97.347	-9.044	-97.347	-1.135	-2.751
12.75E+09	-12.026	15.650	-2.717	176.749	-2.717	176.749	-12.026	15.650
13.05E+09	-0.736	-2.650	-13.295	95.005	-13.295	95.005	-0.736	-2.650
13.35E+09	-0.357	-27.461	-21.583	68.175	-21.583	68.175	-0.357	-27.461
13.65E+09	-0.294	-47.296	-29.127	49.027	-29.127	49.027	-0.294	-47.296
13.95E+09	-0.278	-65.784	-39.725	36.983	-39.725	36.983	-0.278	-65.784
14.25E+09	-0.275	-83.768	-45.375	169.387	-45.375	169.387	-0.275	-83.768
14.55E+09	-0.277	-101.542	-35.988	164.157	-35.988	164.157	-0.277	-101.542
14.85E+09	-0.282	-119.232	-32.348	148.414	-32.348	148.414	-0.282	-119.232
15.15E+09	-0.289	-136.894	-30.136	131.474	-30.136	131.474	-0.289	-136.894
15.45E+09	-0.297	-154.550	-28.526	114.171	-28.526	114.171	-0.297	-154.550
15.75E+09	-0.305	-172.202	-27.227	96.721	-27.227	96.721	-0.305	-172.202

S parameters of the proposed external resonator

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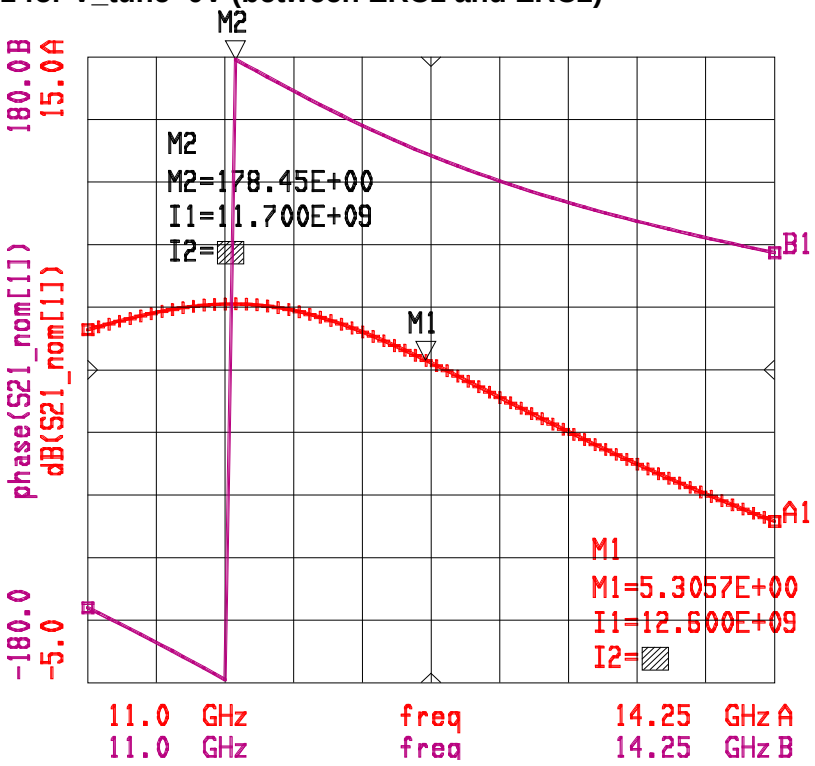
External Resonator Coupling Information

The external resonator has to be an equivalent band-pass filter with 180° insertion phase at resonance (oscillation) frequency. However, this filter must be compatible to the loop parameters of the oscillator (between ERC ports) in order to obtain the oscillation conditions and to avoid parasitic oscillations. The following information concerns the S parameters of the chip (plots for S21 and tables for the four parameters), reference ports are ERC1 and ERC2. These values don't include the wire bonding equivalent inductance L_erc1 and L_erc2 given in section "Typical Assembly and Bias Configuration". For more detail and for a wider band analysis a complete S parameter file is available on request.

MMIC S21 for V_tune=0V (between ERC1 and ERC2)



freq	dB(S11)	Phase(S11)	dB(S21)	Phase(S21)	dB(S12)	Phase(S12)	dB(S22)	Phase(S22)
11	-4.76	-120.8	6.28	-136.9	-24.28	135.4	-10.50	-39.2
11.25	-5.98	-143.0	6.73	-152.2	-23.66	120.9	-10.96	-36.4
11.5	-7.56	-172.9	7.035	-168.3	-23.17	105.6	-11.18	-31.7
11.75	-8.71	147.5	7.10	175.1	-22.94	89.7	-10.95	-26.5
12	-8.22	105.0	6.86	158.7	-23.01	74.0	-10.34	-23.1
12.25	-6.62	71.3	6.34	143.4	-23.36	59.3	-9.64	-22.4
12.5	-5.06	47.3	5.63	129.5	-23.91	46.1	-9.06	-23.7
12.75	-3.88	29.9	4.80	117.3	-24.58	34.4	-8.67	-25.8
13	-3.04	16.5	3.95	106.6	-25.23	24.2	-8.43	-28.2
13.25	-2.45	6.0	3.10	97.1	-25.97	15.3	-8.31	-30.7
13.5	-2.01	-2.6	2.30	88.6	-26.62	7.3	-8.28	-32.9
13.75	-1.67	-9.7	1.54	81.0	-27.23	0.2	-8.30	-35.0
14	-1.46	-15.9	0.82	73.9	-27.80	-6.4	-8.37	-36.8
14..25	-1.28	-21.2	0.16	67.4	-28.31	-12.6	-8.47	-38.5

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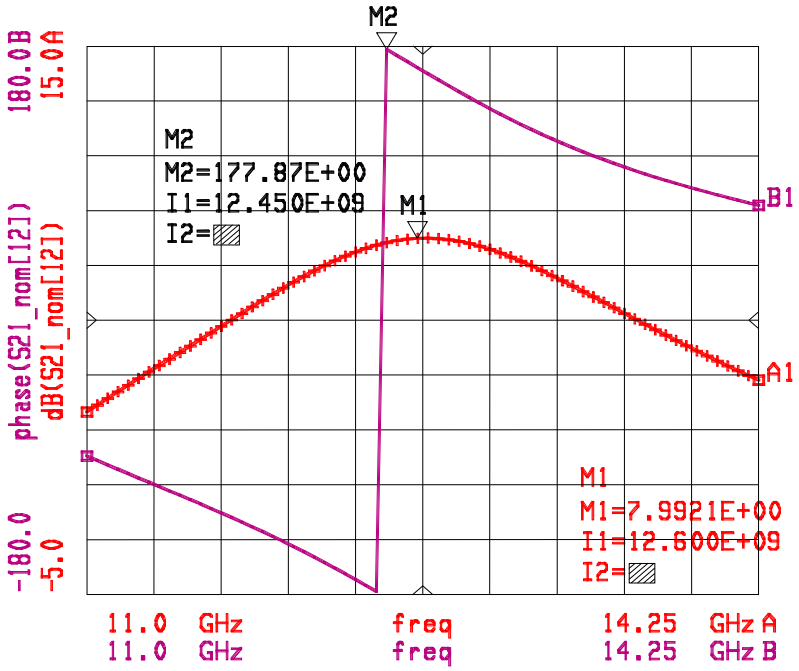
MMIC S21 for V_tune=2V (between ERC1 and ERC2)



freq	dB(S11)	Phase(S11)	dB(S21)	Phase(S21)	dB(S12)	Phase(S12)	dB(S22)	Phase(S22)
11	-6.2	-16.0	1.66	-89.1	-28.9	-176.9	-9.16	50.9
11.25	-5.2	-34.1	2.88	-103.6	-27.5	169.5	-9.86	-52.7
11.5	-5	-50.3	4.07	-117.8	-26.1	156.0	-10.82	-53.7
11.75	-5.5	-66.5	5.26	-132.6	-24.8	142.0	-12.14	-52.6
12	-7.1	-84.5	6.39	-148.6	-23.5	126.6	-13.76	-46.1
12.25	-10.4	-107.1	7.34	-166.6	-22.4	109.4	-14.75	-30.0
12.5	-18.4	-151.9	7.91	173.9	-21.6	90.4	-13.45	-12.4
12.75	-16.1	80.0	7.94	153.9	-21.4	71.1	-11.18	-6.7
13	-9.1	45.0	7.46	135.3	-21.8	53.0	-9.42	-9.6
13.25	-5.8	25.9	6.63	119.1	-22.4	37.3	-8.39	-15.0
13.5	-4.1	11.9	5.66	105.4	-23.3	24.1	-7.87	-20.6
13.75	-3.0	1.2	4.66	93.9	-24.1	13.1	-7.64	-25.5
14	-2.3	-7.5	3.7	84.1	-24.9	3.7	-7.59	-29.6
14..25	-1.9	-14.5	2.81	75.5	-25.7	-4.5	-7.64	-33

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Ordering Information

Chip form : CHV2242c98F/00

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