

31-40GHz Variable Gain Amplifier

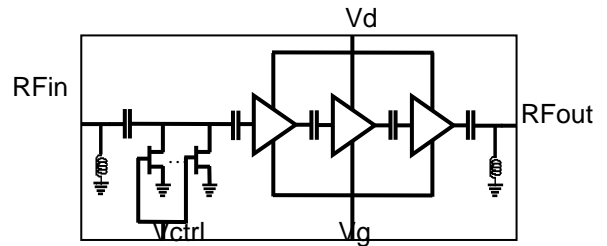
GaAs Monolithic Microwave IC

Description

The CHA3694 is a variable gain broadband three-stage monolithic amplifier. It is designed for a wide range of applications, typically commercial communication systems.

The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a power pHEMT process, 0.15 μ m gate length, via holes through the substrate and air bridges.

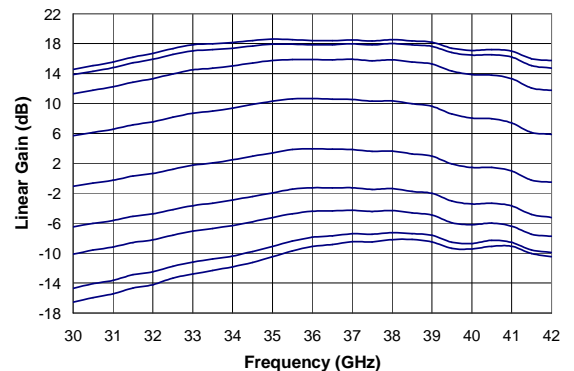


It is supplied in chip form.

Main Features

- Broadband performance 31-40GHz
- 17dB gain
- 25dBm output IP3
- 26dB gain control range
- ESD protected (see page 11)
- DC power consumption: 3.5V, 160mA
- Chip size: 2.41 x 2.08 x 0.07mm

On-Wafer Measurements



Main Characteristics

Tamb. = 25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	31		40	GHz
G	Small signal gain		17		dB
Gc	Gain control range		26		dB
OIP3	3 rd Output Intercept Point @ max. gain		25		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb. = 25°C. These values are representative of on-wafer measurements.

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	31		40	GHz
G	Nominal gain @ max. gain (31-37GHz)	12.5	14.5		dB
	Nominal gain @ max. gain (37-40GHz)	14	17		dB
NF	Noise Figure @ max. gain (31-37GHz)		10	12	dB
	Noise Figure @ max. gain (37-40GHz)		8	10	dB
RLin	Input Return Loss (any attenuation) (31-34GHz)		-4	-3	dB
	Input Return Loss (any attenuation) (34-39GHz)		-3	-2	dB
	Input Return Loss (any attenuation) (39-40GHz)		-4	-3	dB
RLout	Output Return Loss (any attenuation) (31-37GHz)		-11.5	-10	dB
	Output Return Loss (any attenuation) (37-40GHz)		-7	-6	dB
OIP3	3 rd Output Intercept Point @ max. gain	23	25		dBm
P1dB	Output Power at 1dB gain compression @ nominal gain	15	17		dBm
Gc	Gain control range (31-34GHz)	25	26		dB
	Gain control range (34-40GHz)	23	25		dB
Vd	Drain bias voltage		3.5		V
Id	Drain bias current (*)	120	160	200	mA
Idc	Drain current at 1dB gain compression		180		mA
Vg	Gate bias voltage		-0.8		V
Vctrl	Variable gain control voltage	-1.5		+0,6	V

(*) Id not affected by Vctrl.

Absolute Maximum Ratings (*)

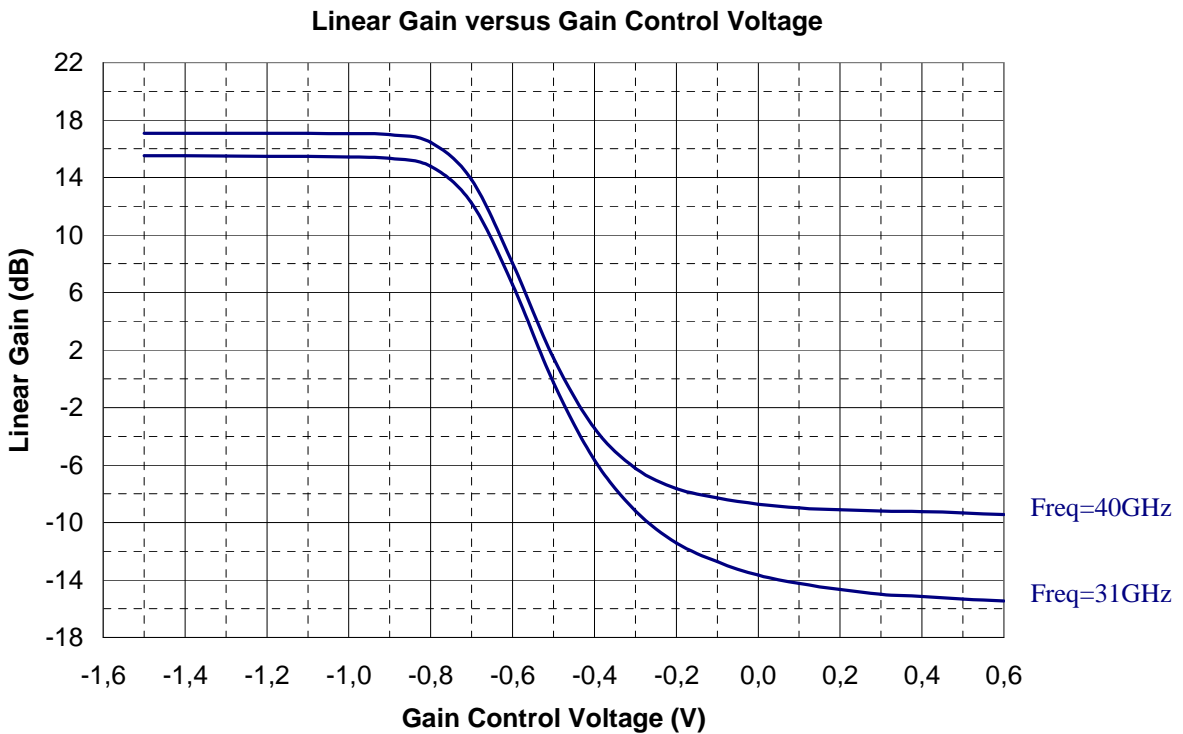
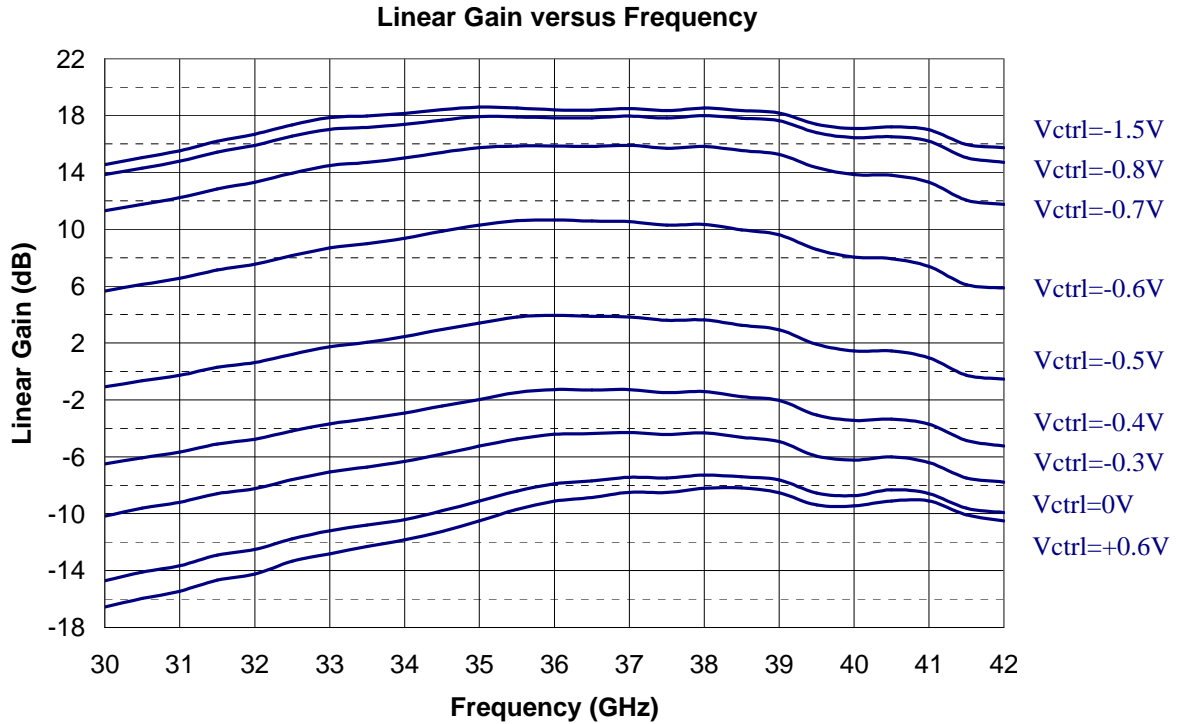
Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4	V
Id	Power supply quiescent current	200	mA
Vg	Gate bias voltage	-4.0 to +0.8	V
Vctrl	Variable gain control voltage	-2.5 to +0.8	V
Pin	RF input power overdrive @ 3.5V	5	dBm
Tch	Maximum channel temperature	+175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

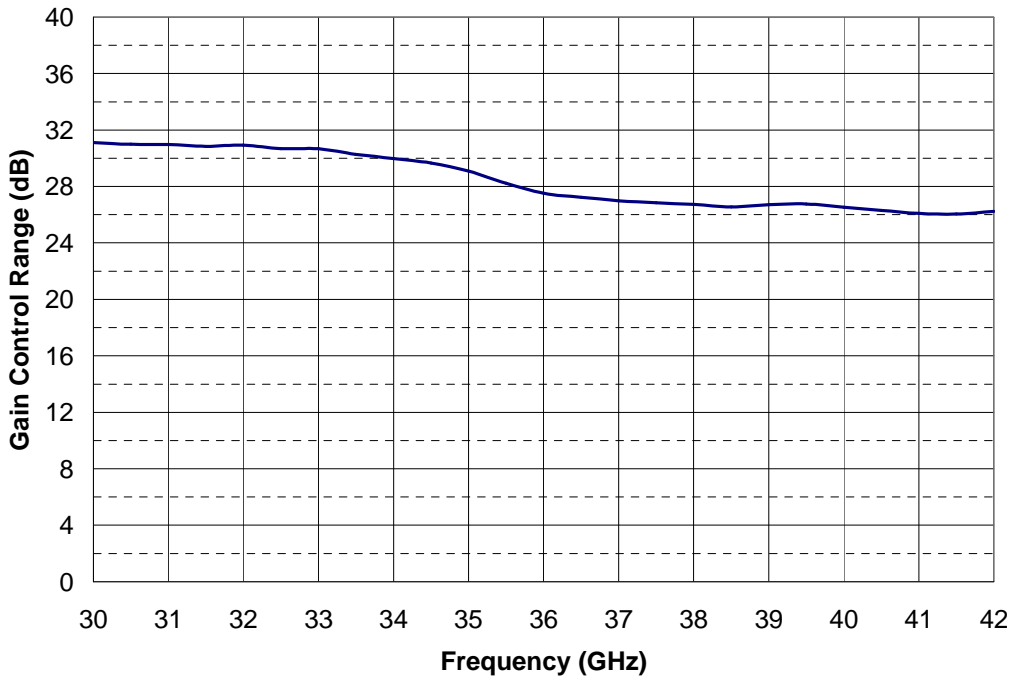
(*) Operation of this device above anyone of these parameters may cause permanent damage.

Typical On-Wafer Measured Performance

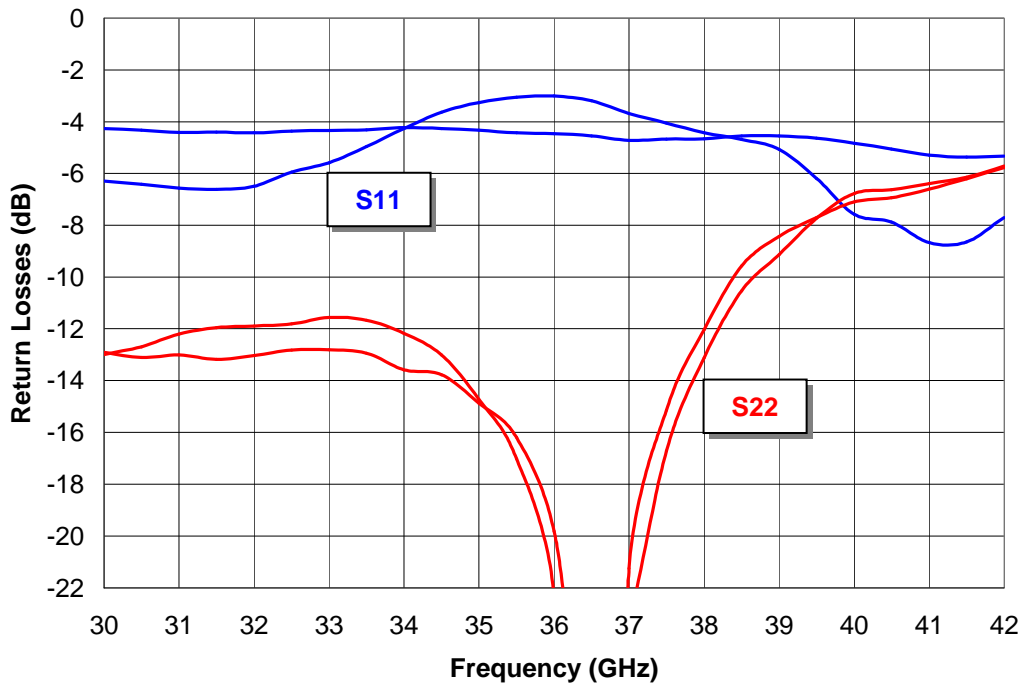
Tamb. = +25°C, Vd = +3.5V, Vg tuned for Id = 160mA



Gain Control Range versus Frequency



Return Losses versus Frequency and Gain Control Voltage (-1,5V & +0,6V)



Typical On-Wafer Sij parameters for Vctrl = -1.5V

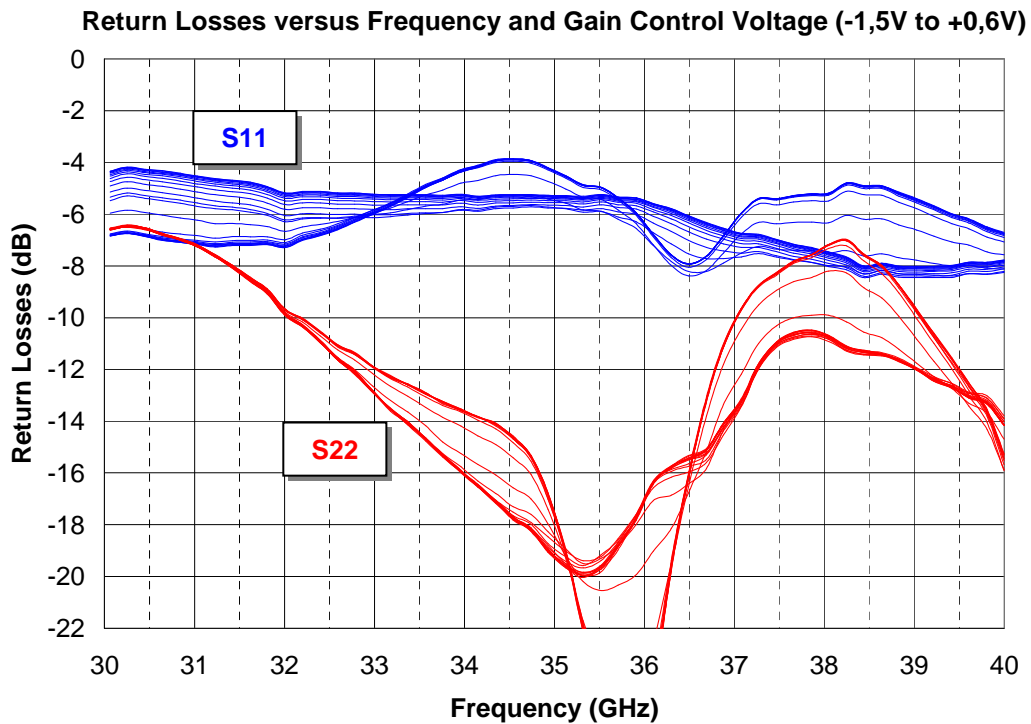
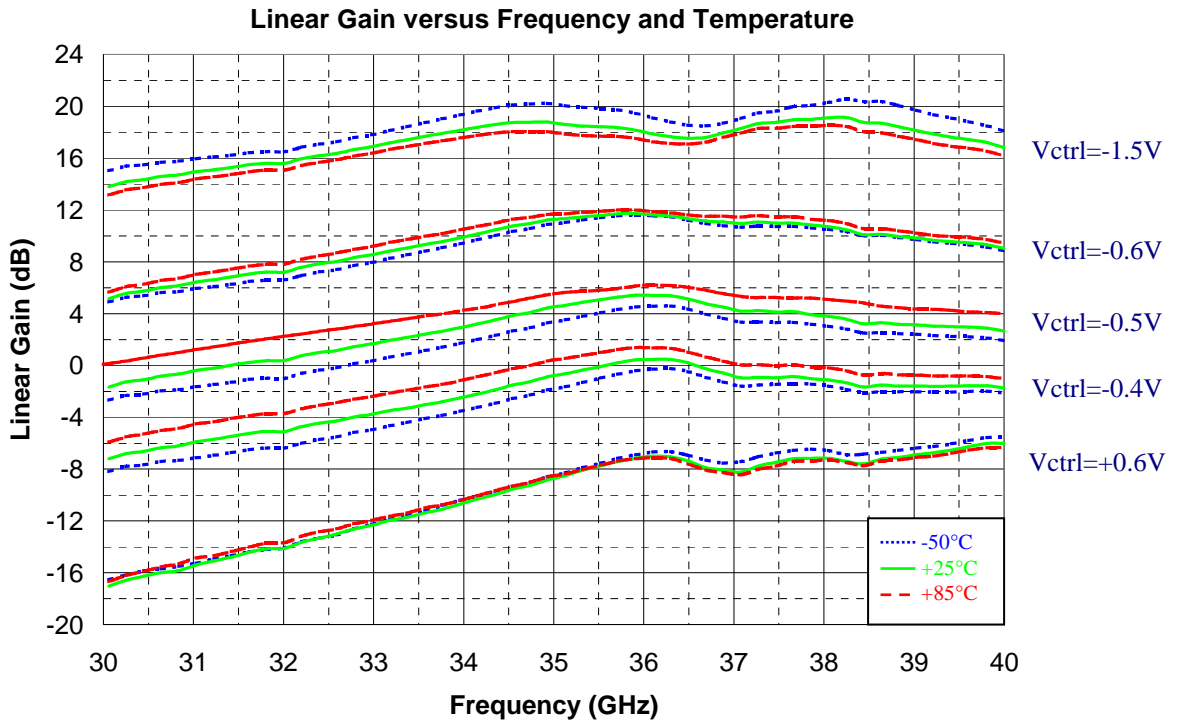
Tamb. = +25°C, Vd = +3.5V, Id = 160mA

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S2 1)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
1,0	0,0	174	-72,4	103	-48,9	-50	-0,8	163
2,0	-0,1	167	-70,1	91	-50,9	-173	-4,5	146
3,0	0,1	161	-69,9	-127	-45,2	38	-5,7	178
4,0	-0,1	154	-68,1	-164	-48,5	-41	-0,9	163
5,0	-0,3	146	-77,5	-160	-51,3	-178	-0,9	141
6,0	-1,5	134	-63,5	-162	-45,3	131	-2,0	127
7,0	-0,8	143	-68,2	102	-36,1	30	-3,2	118
8,0	-0,6	133	-69,1	15	-31,6	1	-4,3	110
9,0	-0,7	124	-68,1	107	-24,4	-32	-5,8	104
10,0	-0,7	116	-63,2	167	-17,2	-84	-7,4	106
11,0	-0,9	108	-55,7	152	-12,5	-140	-7,1	113
12,0	-1,1	98	-49,7	137	-9,0	166	-6,0	109
13,0	-1,4	87	-48,2	114	-6,5	117	-5,1	102
14,0	-1,9	74	-47,7	67	-4,3	70	-4,5	92
15,0	-3,0	57	-51,4	23	-2,9	24	-4,1	81
16,0	-4,9	36	-57,1	1	-1,5	-19	-3,7	68
17,0	-9,6	11	-61,5	-25	-0,5	-60	-3,3	54
18,0	-23,3	-24	-62,5	56	0,4	-98	-3,2	39
19,0	-16,3	151	-64,1	110	1,7	-132	-3,3	21
20,0	-10,5	129	-64,4	133	3,1	-168	-3,5	4
21,0	-8,0	113	-54,4	149	5,0	155	-4,0	-14
22,0	-7,0	99	-50,1	122	6,5	117	-4,7	-31
23,0	-6,6	87	-48,4	130	8,6	81	-5,7	-49
24,0	-6,8	76	-46,4	95	10,4	37	-6,7	-67
25,0	-7,0	70	-46,3	70	11,7	-8	-8,1	-85
26,0	-7,2	64	-47,0	63	12,4	-52	-9,9	-101
27,0	-7,2	59	-45,8	64	12,9	-93	-11,9	-118
28,0	-7,1	52	-47,6	55	13,5	-134	-14,4	-137
29,0	-6,8	47	-44,3	52	13,9	-176	-18,4	-172
30,0	-7,2	43	-47,1	39	14,6	145	-20,5	152
31,0	-7,2	39	-46,9	49	15,5	106	-21,5	88
31,5	-7,3	38	-45,9	44	16,2	85	-20,6	56
32,0	-7,2	38	-46,0	45	16,7	62	-19,6	49
32,5	-6,9	39	-43,8	37	17,3	40	-18,4	27
33,0	-6,1	39	-44,8	31	17,9	14	-17,9	24
33,5	-5,2	37	-44,3	21	18,0	-10	-16,2	8
34,0	-4,4	32	-46,2	19	18,1	-33	-15,6	-6
34,5	-3,9	26	-45,4	28	18,4	-57	-15,2	-18
35,0	-3,4	20	-44,7	26	18,6	-83	-16,4	-29
35,5	-3,0	13	-42,8	26	18,5	-108	-17,7	-28
36,0	-2,7	6	-42,0	14	18,4	-133	-17,7	-33
36,5	-2,8	-2	-41,1	0	18,4	-156	-19,8	-51
37,0	-3,0	-9	-41,2	-18	18,5	178	-23,6	-69
37,5	-3,5	-14	-42,5	-30	18,3	153	-50,8	-127
38,0	-3,7	-19	-44,6	-34	18,5	127	-26,4	96
38,5	-4,3	-24	-44,4	-40	18,4	99	-16,9	85
39,0	-4,9	-28	-45,0	-54	18,2	70	-12,7	66
39,5	-5,5	-31	-46,4	-64	17,4	42	-9,9	55
40,0	-6,4	-34	-48,0	-63	17,1	16	-8,3	38
41,0	-7,6	-29	-51,7	-118	17,0	-45	-6,9	18
42,0	-7,3	-16	-63,0	-162	15,7	-111	-6,3	5
43,0	-4,8	-17	-59,6	-73	13,2	180	-5,6	-8
44,0	-3,6	-28	-54,8	-89	11,2	100	-6,7	-17
45,0	-2,9	-40	-59,2	-179	2,5	-4	-4,3	-7
46,0	-3,0	-50	-53,9	146	-10,9	-70	-3,2	-26
47,0	-3,2	-61	-47,4	165	-24,5	-107	-3,5	-36
48,0	-3,9	-73	-41,4	111	-47,2	142	-3,4	-42
49,0	-4,6	-87	-39,6	89	-43,7	171	-3,0	-50
50,0	-6,8	-102	-37,2	53	-29,1	96	-3,7	-57

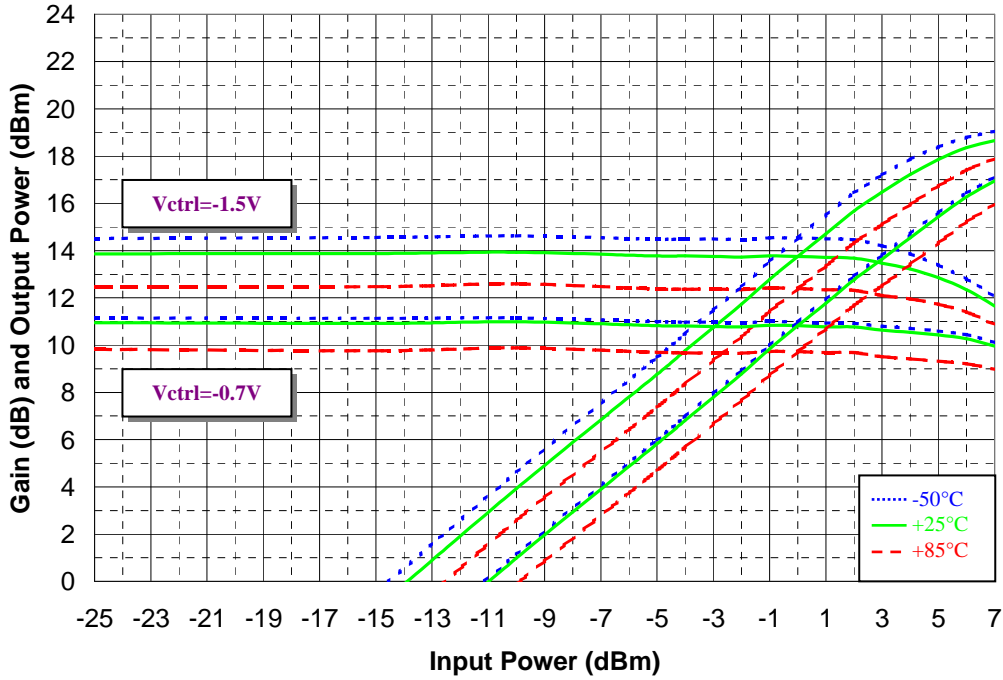
Typical Measured Performance in Test Fixture

Vd = +3.5V, Vg tuned for Id = 160mA

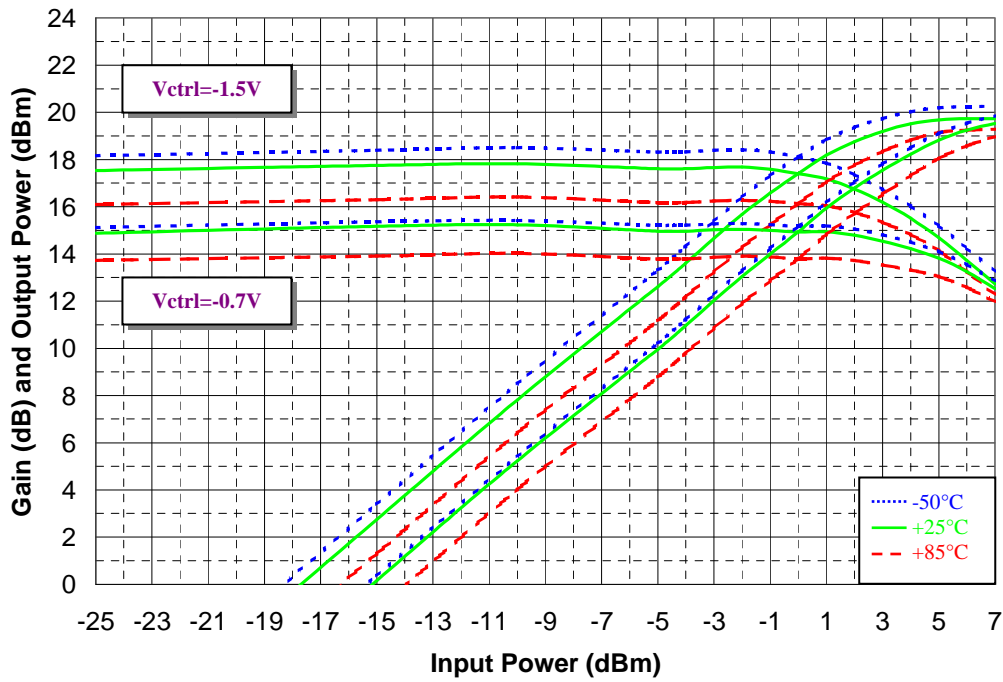
Measurements in test fixture, using the proposed chip assembly, as defined page 10.



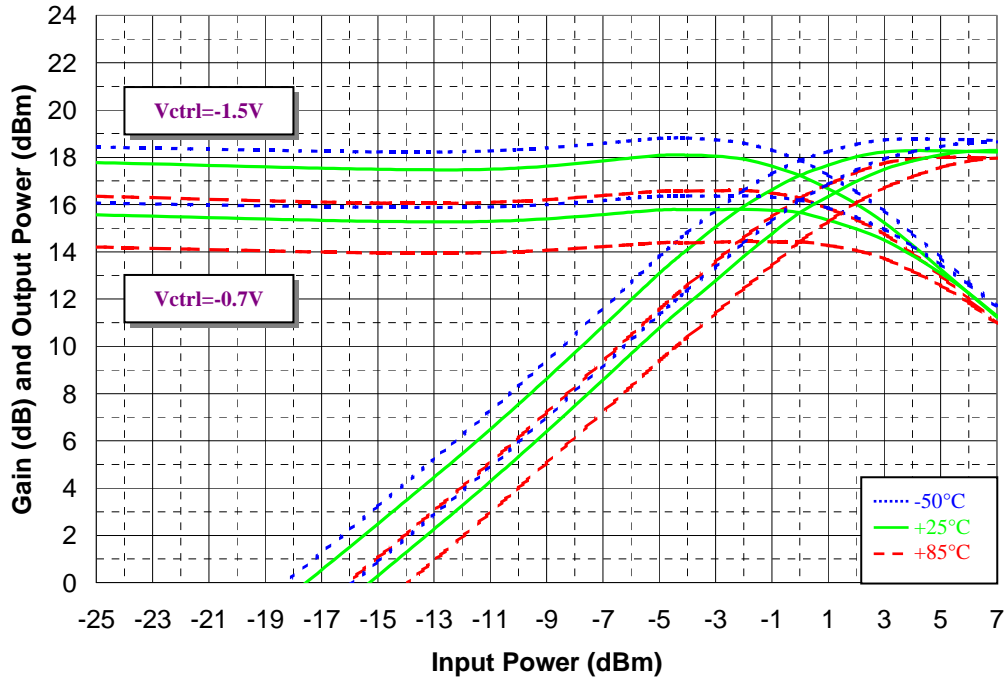
Gain and Output Power versus Input Power and Temperature @ 31GHz



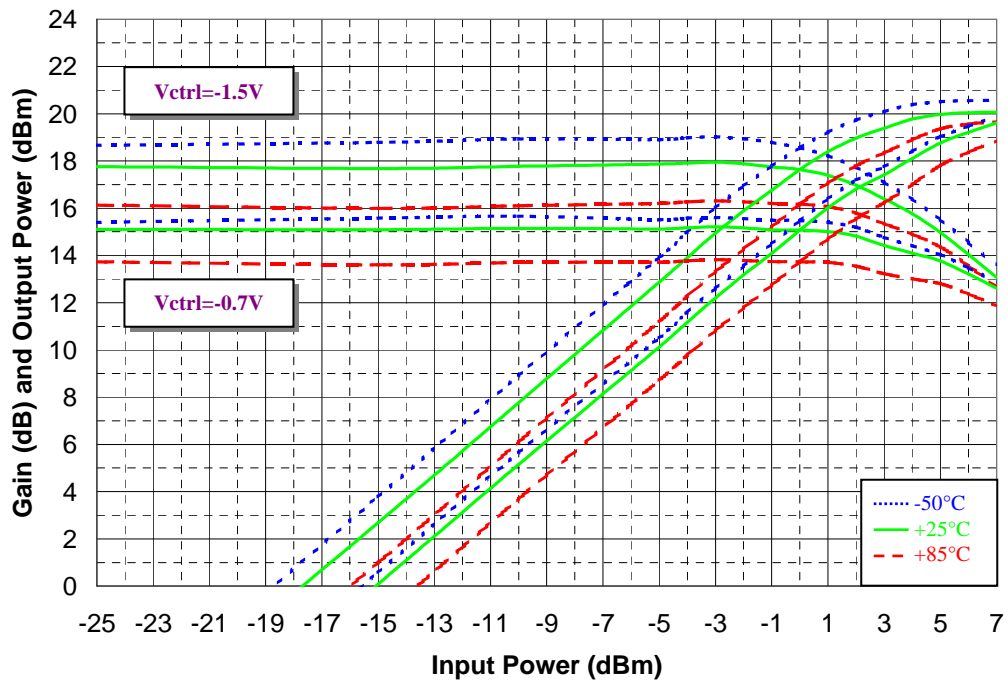
Gain and Output Power versus Input Power and Temperature @ 34GHz



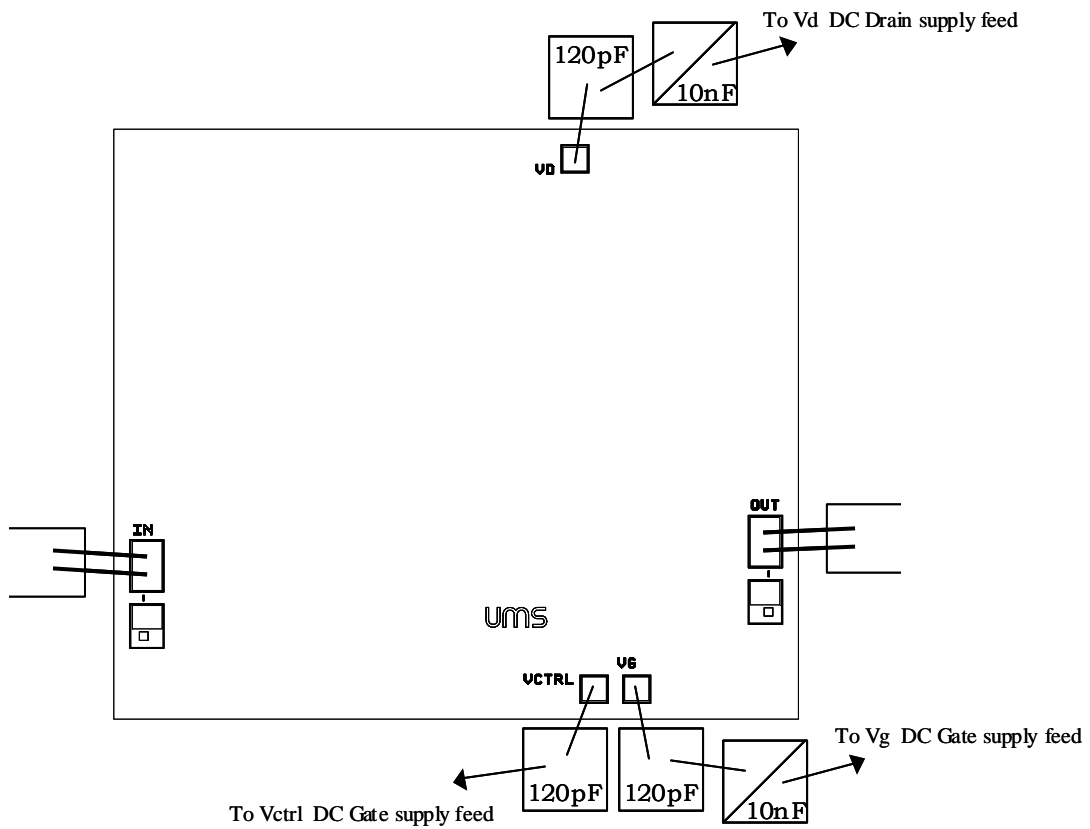
Gain and Output Power versus Input Power and Temperature @ 37GHz



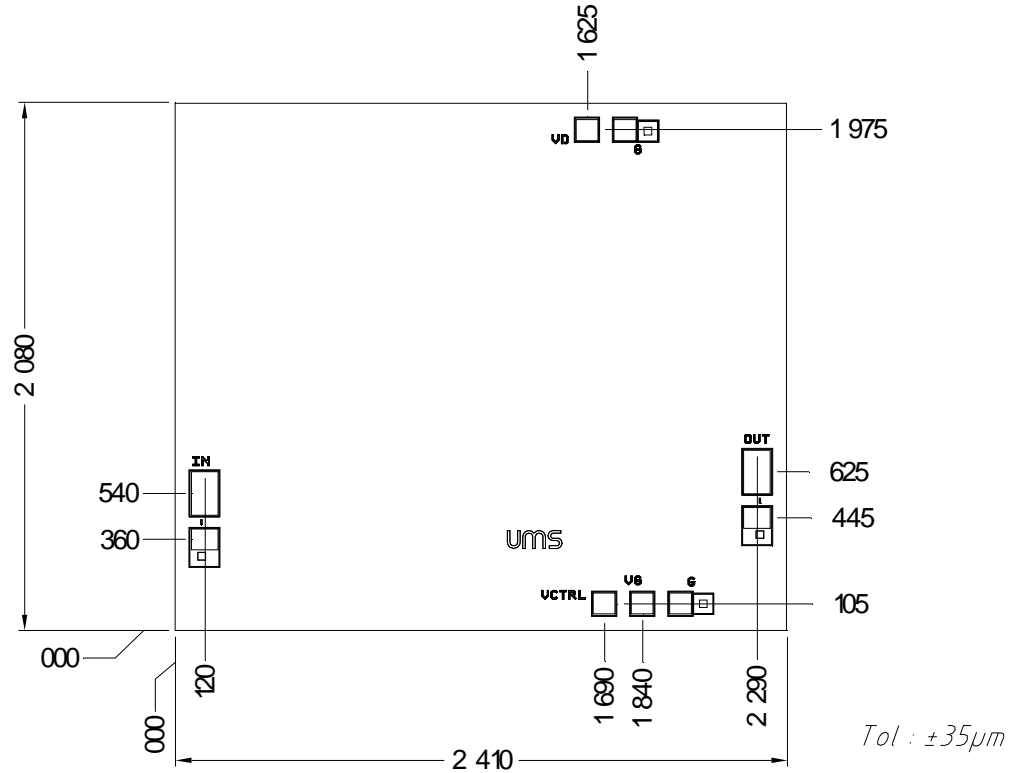
Gain and Output Power versus Input Power and Temperature @ 40GHz



Chip Assembly and Mechanical Data



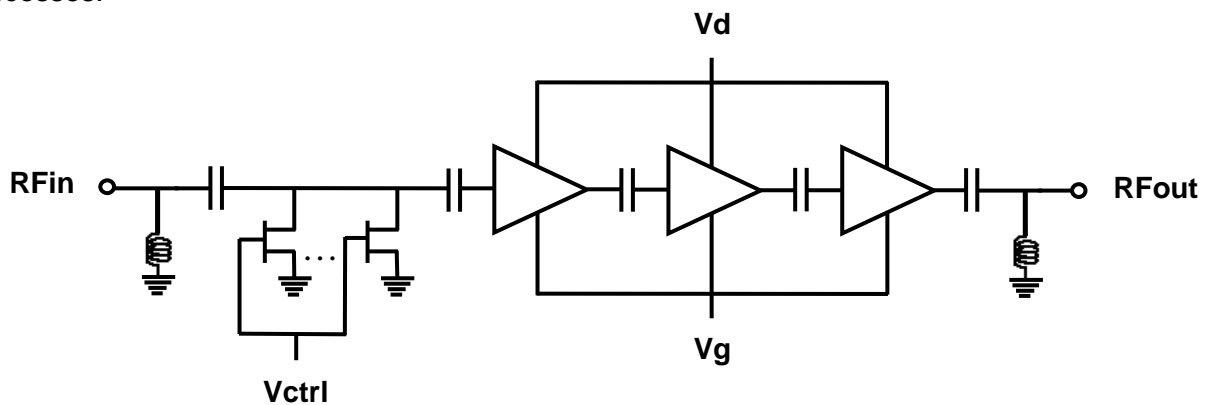
Note : Supply feed should be capacitively bypassed.
 25 μ m diameter gold wire is recommended.
 RF wire bondings should be as short as possible, lower than 0.35mm.
 RF Pad size: 105/172 μ m
 DC Pad size : 86/83 μ m



Bonding pad positions
 (Chip thickness : 70µm. All dimensions are in micrometers)

Notes

- Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections are also implemented on gate and control accesses.

- Due to BCB coating on the chip, qualification domain implies the chip must be glued.

Ordering Information

Chip form: CHA3694-98F/00

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